LH52256C/CH

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time: 70 ns (MAX.)
- Supply current:
  Operating: 45 mA (MAX.)
  10 mA (MAX.) (t_{RC}, t_{WC} = 1 µs)
  Standby: 40 µA (MAX.)
- Data retention current: 1.0 µA (MAX.)
  (V_{CCDR} = 3 V, T_A = 25°C)
- Wide operating voltage range:
  4.5 V ± 5.5 V
- Operating temperature:
  Commerical temperature 0°C to +70°C
  Industrial temperature -40° to +85°C
- Fully-static operation
- Three-state outputs
- Not designed or rated as radiation hardened
- Package:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  28-pin, 300-mil SK-DIP
  28-pin, 8 × 3 mm^2 TSOP (Type I)
- N-type bulk silicon

DESCRIPTION

The LH52256C is a Static RAM organized as 32,768 × 8 bits which provides low-power standby mode. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

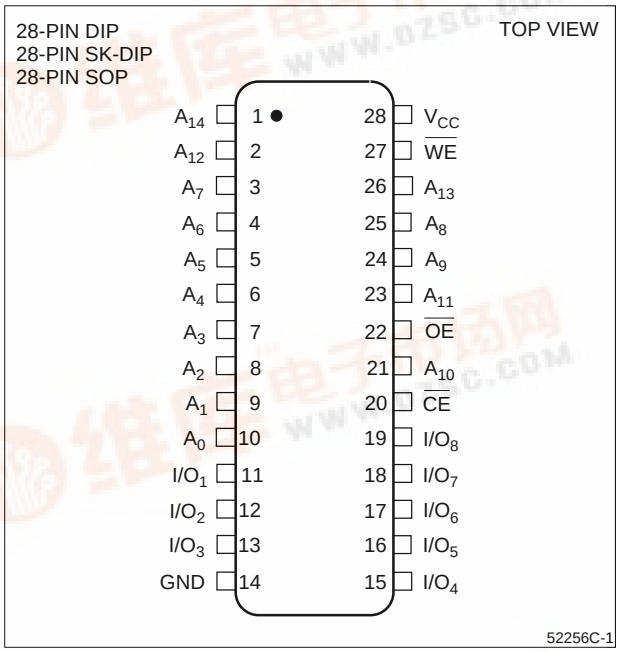


Figure 1. Pin Connections

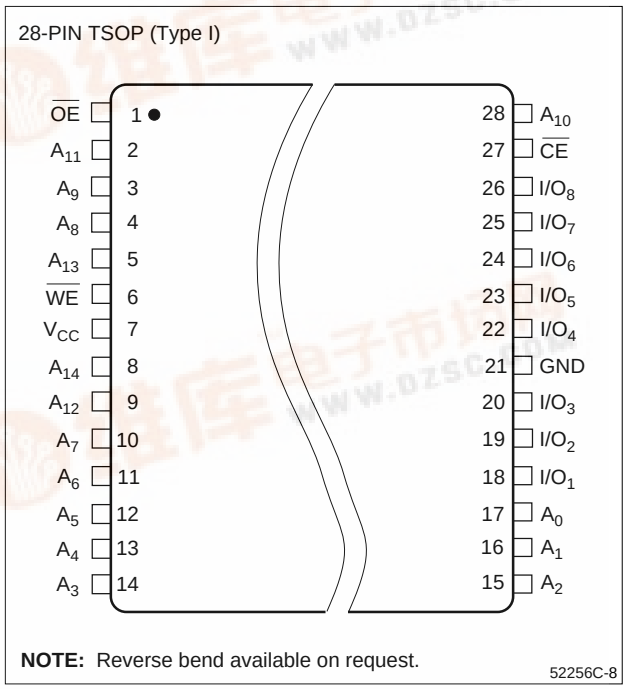


Figure 2. TSOP (Type I) Pin Connections

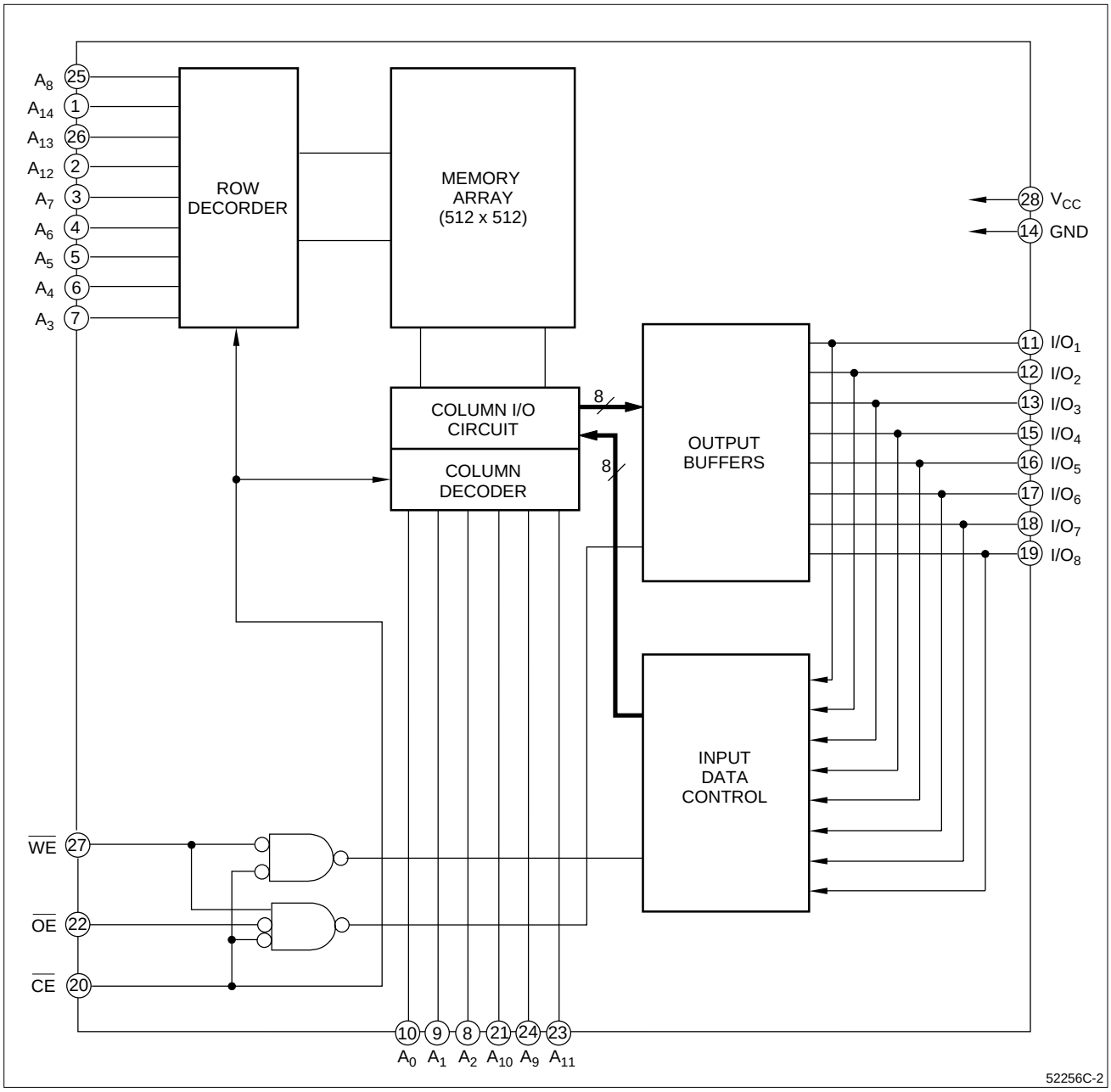


Figure 3. LH52256C Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address inputs
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Standby	High impedance	Standby (I_{SB})	1
L	H	L	Read	Data output	Active (I_{CC})	1
L	H	H	Output disable	High impedance	Active (I_{CC})	1
L	L	X	Write	Data input	Active (I_{CC})	1

NOTE:
1. X = Don't care, L = Low, H = High

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	–0.5 to +7.0	V	1
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V	1, 2
Operating temperature	T_{OPR}	0 to +70	°C	—
Storage temperature	T_{STG}	–65 to +150	°C	—

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Undershoot of -3.0 V is allowed width of pulse below 50 ns.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	—
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V	—
	V_{IL}	–0.5	—	0.8	V	1

NOTE:
1. Undershoot of -3.0 V is allowed width of pulse below 50 ns.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 4.5 V to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0	—	1.0	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 V to V_{CC}	–1.0	—	1.0	µA
Operating supply current	I_{CC}	Minimum cycle, V_{IN} = V_{IL} or V_{IH} $I_{I/O}$ = 0 mA, $\overline{CE}$ = V_{IL}	—	25	45.0	mA
	I_{CC1}	t_{RC}, t_{WC} = 1 µs, V_{IN} = V_{IL} or V_{IH}, $I_{I/O}$ = 0 mA, $\overline{CE}$ = V_{IL}	—	—	10.0	
Standby current	I_{SB}	$\overline{CE}$ ≥ V_{CC} – 0.2 V	—	0.6	40.0	µA
	I_{SB1}	$\overline{CE}$ = V_{IH}	—	—	3.0	mA
Output voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4	—	—	

NOTE:

Typical values at V_{CC} = 5.0 V, T_A = 25°C

AC ELECTRICAL CHARACTERISTICS
AC Test Conditions

PARAMETER	MODE	NOTE
Input pulse level	0.6 V to 2.4 V	—
Input rise and fall time	10 ns	—
Input and output timing Ref. level	1.5 V	—
Output load	1 TTL + C_L (100 pF)	1

NOTE:

1. Including scope and jig capacitance.

READ CYCLE (T_A = 0°C to +70°C, V_{CC} = 4.5 V to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	70	—	ns	—
Address access time	t_{AA}	—	70	ns	—
$\overline{CE}$ access time	t_{ACE}	—	70	ns	—
Output enable to output valid	t_{OE}	—	35	ns	—
Output hold from address change	t_{OH}	10	—	ns	—
$\overline{CE}$ Low to output active	t_{LZ}	10	—	ns	1
$\overline{OE}$ Low to output active	t_{OLZ}	5	—	ns	1
$\overline{CE}$ High to output in High impedance	t_{HZ}	0	30	ns	1
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	30	ns	1

NOTES:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

WRITE CYCLE (T_A = 0°C to +70°C, V_{CC} = 4.5 V to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	70	—	ns	—
$\overline{CE}$ Low to end of write	t_{CW}	45	—	ns	—
Address valid to end of write	t_{AW}	45	—	ns	—
Address setup time	t_{AS}	0	—	ns	—
Write pulse width	t_{WP}	35	—	ns	—
Write recovery time	t_{WR}	0	—	ns	—
Input data setup time	t_{DW}	30	—	ns	—
Input data hold time	t_{DH}	0	—	ns	—
$\overline{WE}$ High to output active	t_{OW}	5	—	ns	1
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	30	ns	1
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	30	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	V_{IN} = 0 V	—	—	7	pF	1
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	—	10	pF	1

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Data retention supply voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ – 0.2 V		2.0	—	5.5	V	—
Data retention supply current	I_{CCDR}	V_{CCDR} = 3.0 V	T_A = 25°C	—	0.3	1.0	µA	—
			TA = 40°C	—	—	3.0		—
		$\overline{CE} \geq V_{CCDR}$ – 0.2 V				15		
Chip enable setup time	t_{CDR}	—		0	—	—	ns	—
Chip enable hold time	t_R	—		t_{RC}	—	—	ns	1

NOTE:
1. t_{RC} = Read cycle time.
2. Typical values at T_A = 25°C

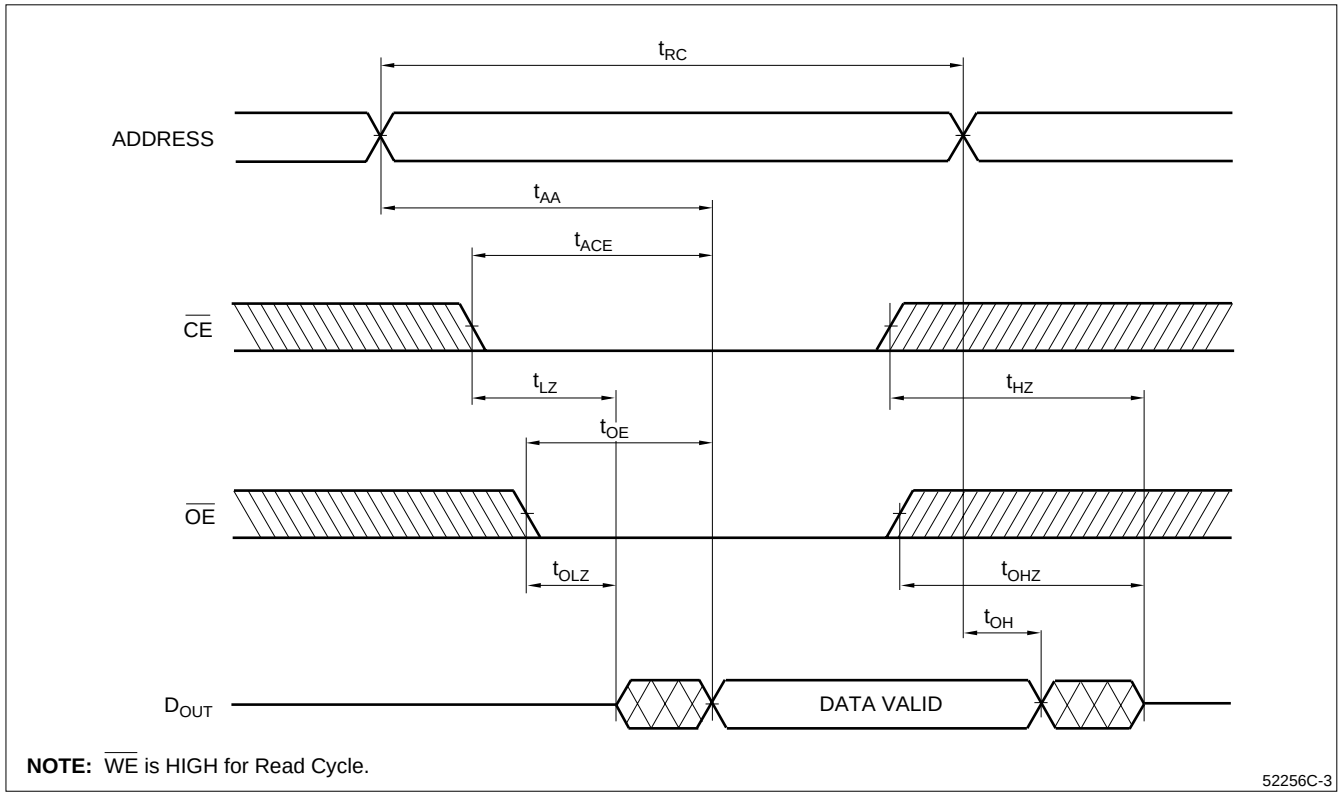
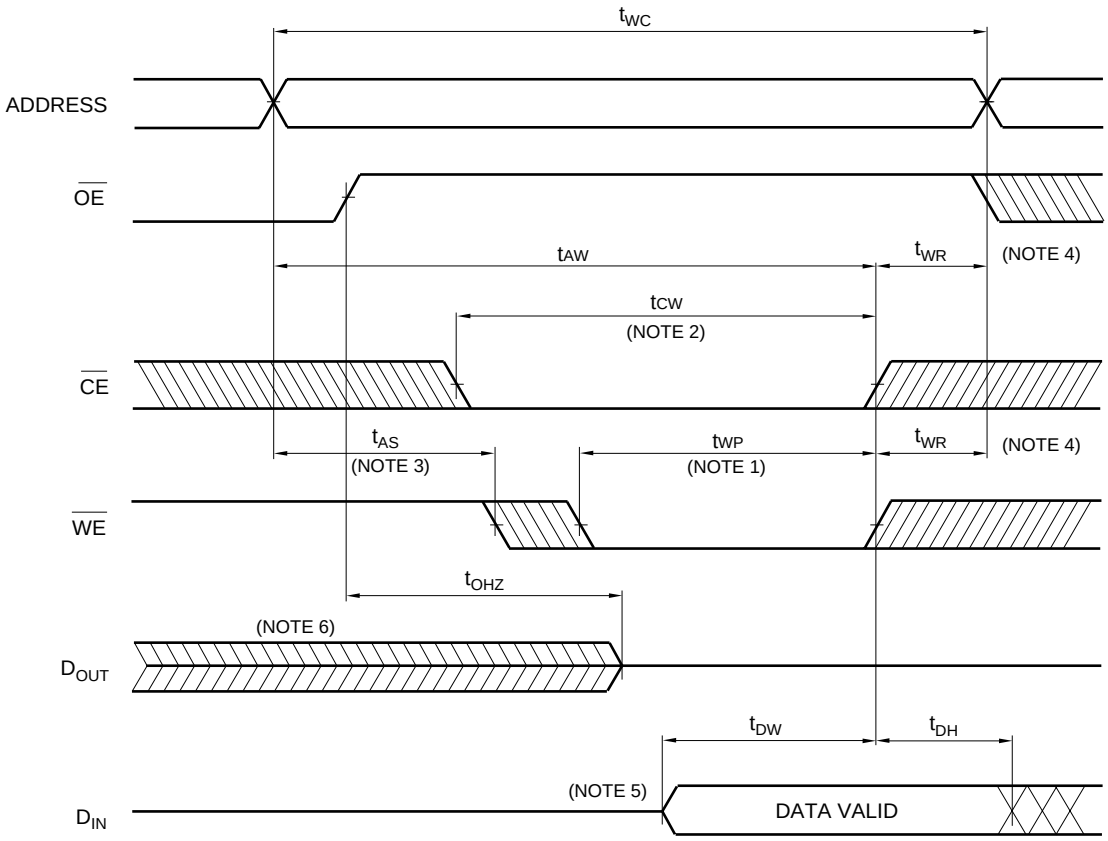


Figure 4. Read Cycle



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CE}$, and a LOW $\overline{WE}$. A write begins at the latest transition among $\overline{CE}$ going LOW, and $\overline{WE}$ going LOW. A write ends at the earliest transition among $\overline{CE}$ going HIGH, and $\overline{WE}$ going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CE}$ going LOW to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CE}$ goes LOW simultaneously with $\overline{WE}$ going LOW or after $\overline{WE}$ going LOW, the outputs remain in high impedance state.
7. If $\overline{CE}$ goes HIGH simulaneously with $\overline{WE}$ going HIGH or before $\overline{WE}$ going HIGH, the outputs remain in high impedance state.

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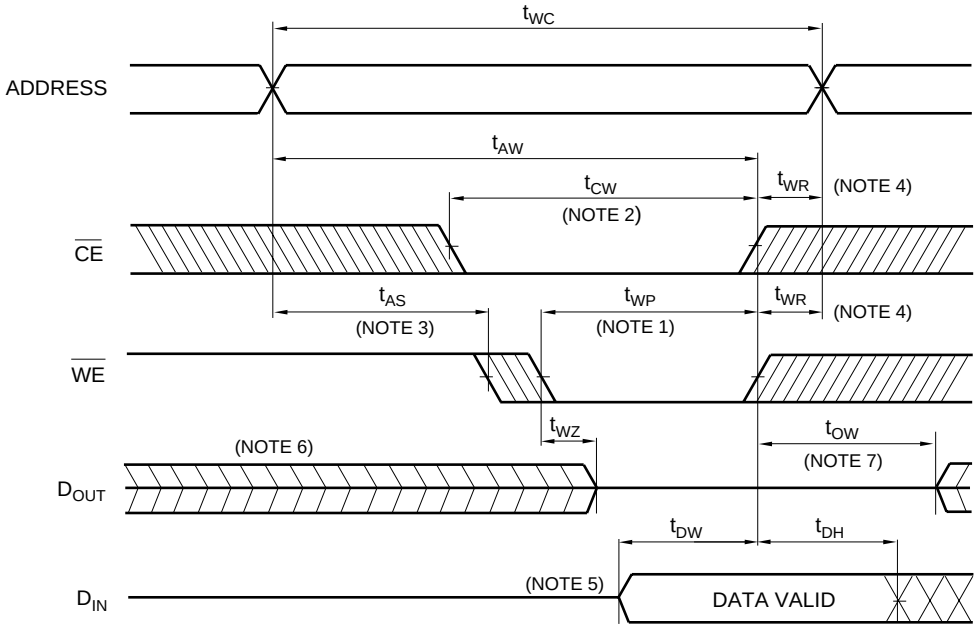
Figure 5. Write Cycle ($\overline{OE}$ Controlled)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CE}$, and a LOW $\overline{WE}$. A write begins at the latest transition among $\overline{CE}$ going LOW, and $\overline{WE}$ going LOW. A write ends at the earliest transition among $\overline{CE}$ going HIGH, and $\overline{WE}$ going HIGH. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CE}$ going LOW to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CE}$ goes LOW simultaneously with $\overline{WE}$ going LOW or after $\overline{WE}$ going LOW, the outputs remain in high impedance state.
7. If $\overline{CE}$ goes HIGH simulaneously with $\overline{WE}$ going HIGH or before $\overline{WE}$ going HIGH, the outputs remain in high impedance state.

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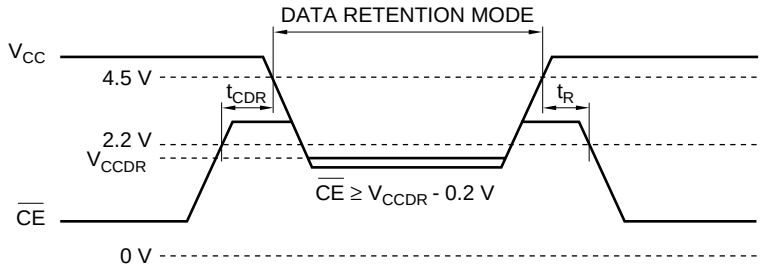
Figure 6. Write Cycle ($\overline{OE}$ Low Fixed)

$\overline{CE}$ CONTROL



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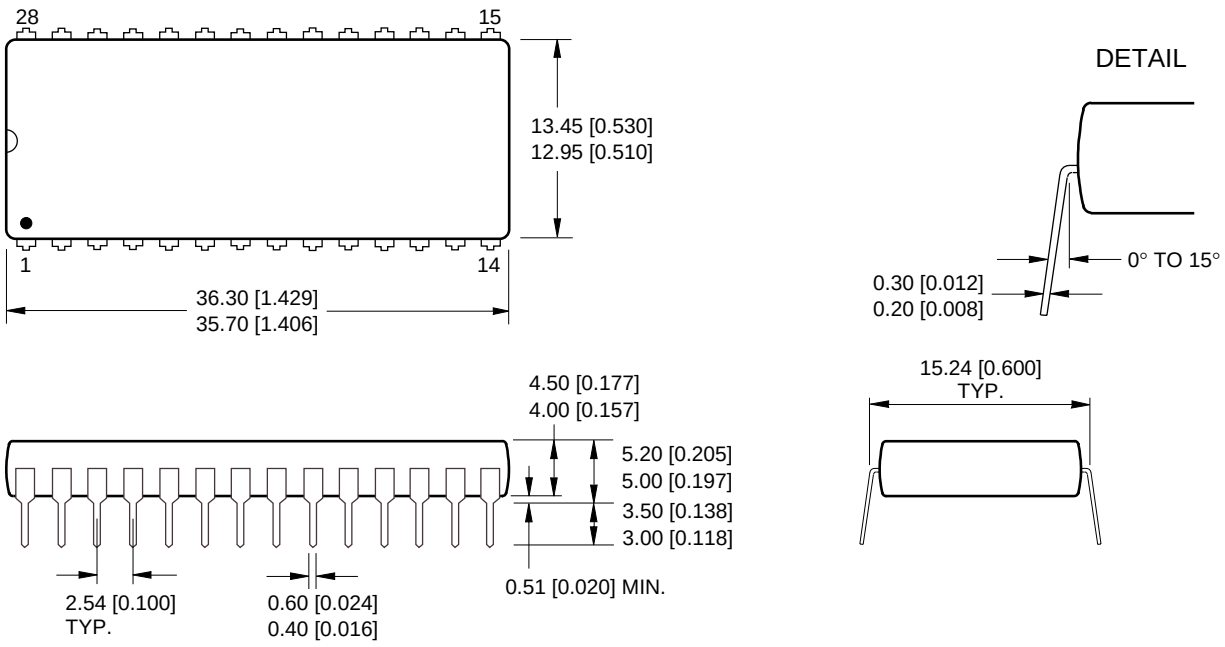
Data Retention Timing Chart
$\overline{CE}$ Controlled

PACKAGE DIAGRAMS

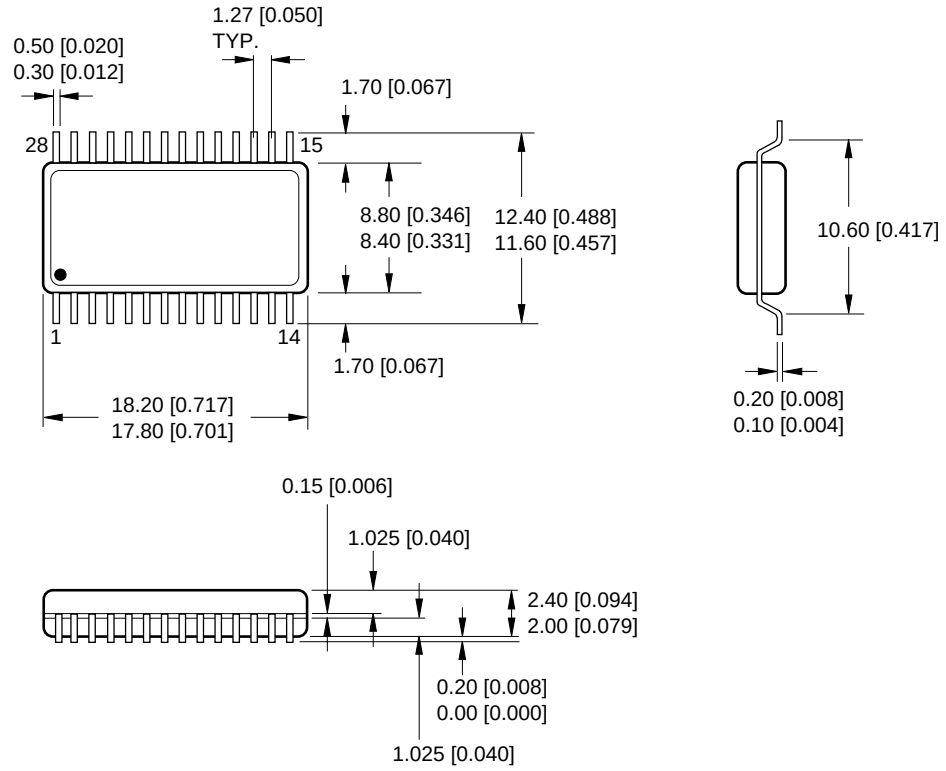
28DIP (DIP028-P-0600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-2

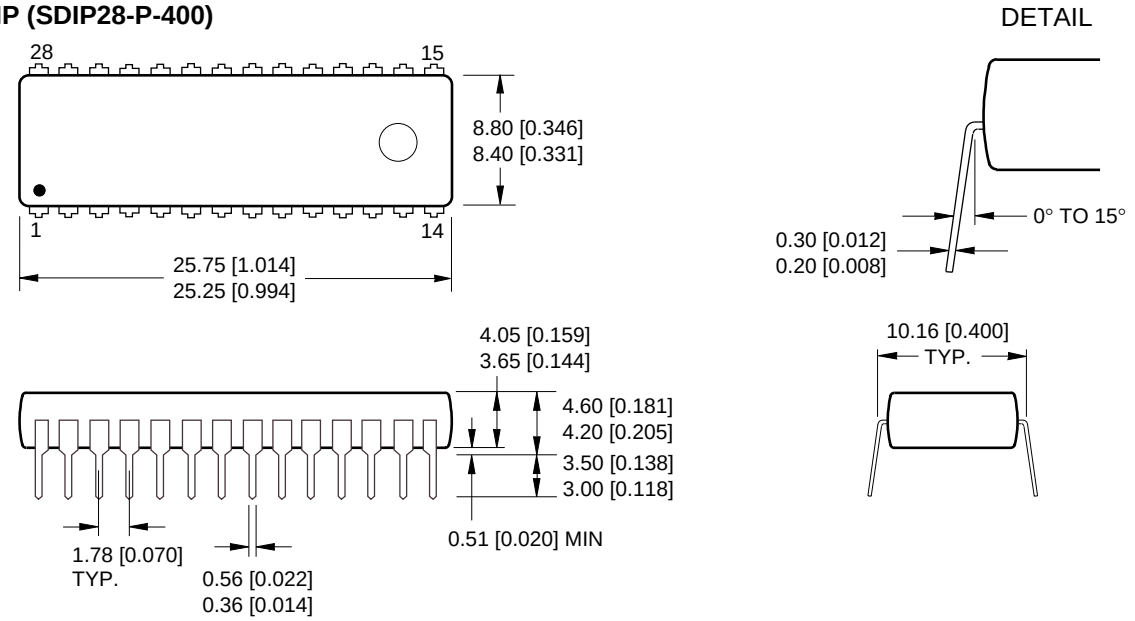
28SOP (SOP028-P-0450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOP

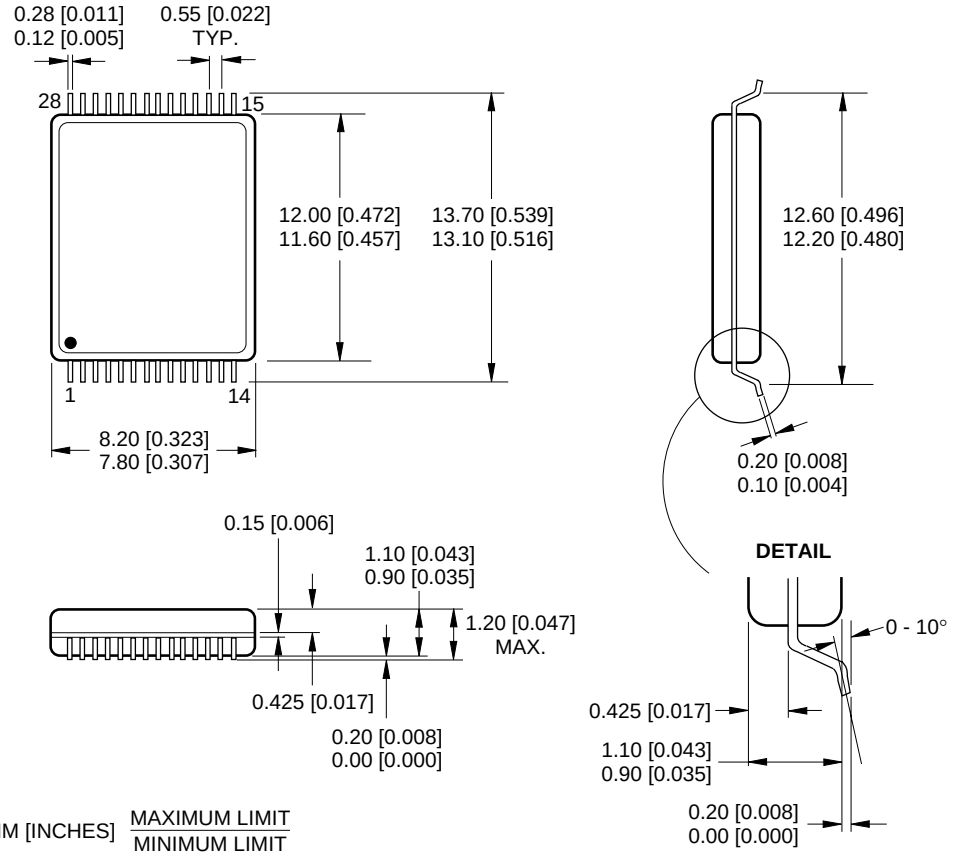
28SDIP (SDIP28-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SDIP

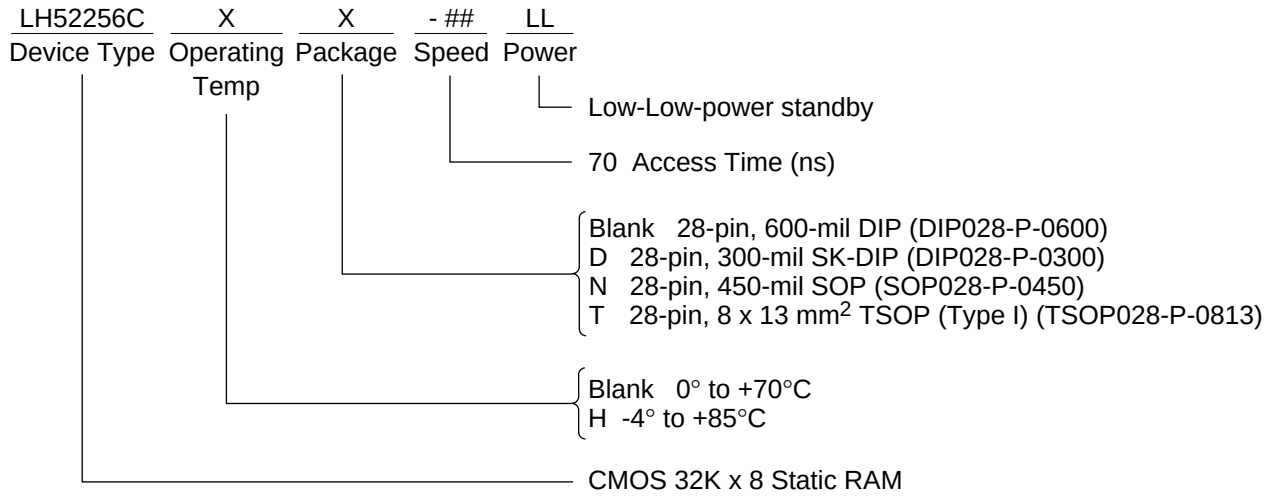
28TSOP (TSOP028-P-0813)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28TSOP

ORDERING INFORMATION



Example: LH52256C-70LL (CMOS 32K x 8 Static RAM, Low-Low-power standby, 70 ns, 28-pin, 600-mil DIP)

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