PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH52256CHT-85LL

256K SRAM

(Model No.: LH525C2T)

Spec No.: EL087111

Issue Date: July 18, 1996

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● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-sale operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Decription

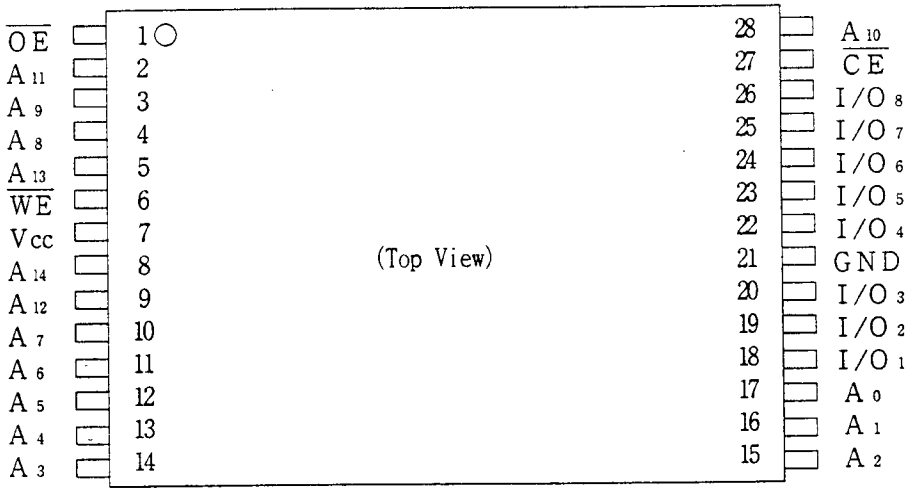
The LH52256CHT-85LL is a static RAM organized as 32,768×8 bit with provides low-power standby mode.
It is fabricated using silicon-gate CMOS process technology.

Features

○Access Time	· · · ·	85 ns (Max.)
○Operating current	· · · ·	40 mA (Max.)
	· · · ·	10 mA (Max. t_{RC}, t_{WC}=1 μs)
○Standby current	· · · ·	40 μA (Max.)
○Data retention current	· · · ·	1.0 μA (Max. V_{CCDR}=3V, Ta=25℃)
○Wide operating voltage range	· · · ·	4.5V to 5.5V
○Operating temperature	· · · ·	−40℃ to +85℃

○Fully static operation
○Three-state output
○Not designed or rated as radiation hardened
○28 pin TSOP (TSOP28-P-0813) plastic package
○N-type bulk silicon

2. Pin Configuration



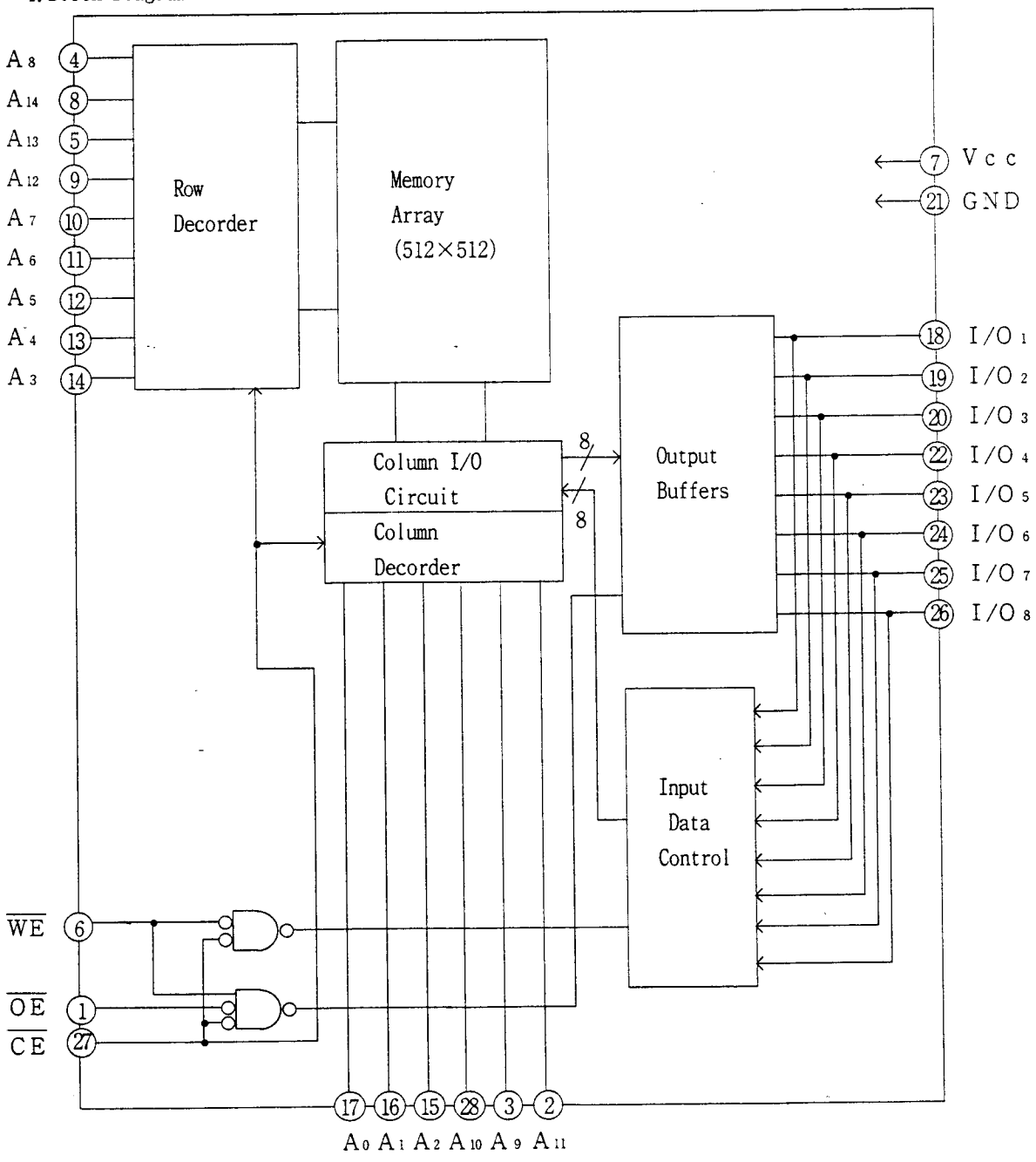
Pin Name	Function
A_0 to A_{14}	Address inputs
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
I/O_1 to I/O_8	Data inputs/outputs
V_{CC}	Power supply
GND	Ground

3. Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1 to I/O8	Supply current
H	*	*	Standby	High impedance	Standby (I_{SB})
L	H	L	Read	Data output	Active (I_{CC})
L	H	H	Output disable	High impedance	Active (I_{CC})
L	L	*	Write	Data Input	Active (I_{CC})

(*=Don't Care, L=Low, H=High)

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1)	V_{CC}	−0.5 to +7.0	V
Input voltage (*1)	V_{IN}	−0.5 (*2) to Vcc+0.5	V
Operating temperature	T_{opr}	−40 to +85	℃
Storage temperature	T_{stg}	−65 to +150	℃

Note) *1. The maximum applicable voltage on any pin with respect to GND.
*2. Undershoot of −3.0V is allowed width of pluse bellow 50ns.

6. Recommended DC Operating Conditions

(Ta=−40℃ to +85)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		Vcc+0.5	V
	V_{IL}	−0.5 (*3)		0.8	V

Note) *3. Undershoot of −3.0V is allowed width of pluse below 50ns.

7. DC Electrical Characteristics

(Ta=−40℃ to +85, Vcc=4.5V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ. (*4)	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=0V to V_{CC}	−1.0		1.0	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=0V to V_{CC}	−1.0		1.0	μA
Operating supply current	I_{CC}	Minimum cycle V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA, $\overline{CE}$=V_{IL}		25	40	mA
	I_{CC1}	t_{RC}, t_{WC}=1μs V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA, $\overline{CE}$=V_{IL}			10	mA
Standby current	I_{SB}	$\overline{CE}$ ≧ V_{CC}−0.2V		0.6	40	μA
	I_{SB1}	$\overline{CE}$=V_{IH}			3	mA
Output voltage	V_{OL}	I_{OL}= 2.1mA			0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4			V

Note) *4. Typical values at Vcc=5.0V, Ta=25℃.

8. AC Electrical Characteristics

AC Test Conditions

Input pulse level	0.6V to 2.4V
Input rise and fall time	10ns
Input and Output timing Ref. level	1.5V
Output load	1TTL+C_L (100pF) (*5)

Note) *5. Including scope and jig capacitance.

Read cycle

(Ta= −40℃ to +85, Vcc= 4.5V to 5.5V)

Parameter	Symbol	Min.	Max.	Unit	
Read cycle time	t_{RC}	85		ns	
Address access time	t_{AA}		85	ns	
$\overline{CE}$ access time	t_{ACE}		85	ns	
Output enable to output valid	t_{OE}		35	ns	
Output hold from address change	t_{OH}	10		ns	
$\overline{CE}$ Low to output active	t_{LZ}	10		ns	*6
$\overline{OE}$ Low to output active	t_{OLZ}	5		ns	*6
$\overline{CE}$ High to output in High impedance	t_{HZ}	0	30	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	30	ns	*6

Write cycle

(Ta= −40℃ to +85, Vcc= 4.5V to 5.5V)

Parameter	Symbol	Min.	Max.	Unit	
Write cycle time	t_{WC}	85		ns	
$\overline{CE}$ Low to end of write	t_{CW}	55		ns	
Address valid to end of write	t_{AW}	55		ns	
Address setup time	t_{AS}	0		ns	
Write pluse width	t_{WP}	40		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	30		ns	
Input data hold time	t_{DH}	0		ns	
$\overline{WE}$ High to output active	t_{OW}	5		ns	*6
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	30	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	30	ns	*6

Note) *6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

9. Data Retention Characteristics

(Ta= −40℃ to +85)

Paramenter	Symbol	Conditions		Min.	Typ. (*7)	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$\overline{CE} \geqq V_{CCDR} - 0.2$ V		2.0		5.5	V
Data Retention supply current	I_{CCDR}	V_{CCDR} = 3 V	Ta = 25℃		0.3	1.0	μA
			Ta = 70℃			15	μA
		$\overline{CE} \geqq V_{CCDR} - 0.2$ V (*5)				20	μA
Chip enable setup time	t_{CDR}			0			ns
Chip enable hold time	t_R			(*8) t_{RC}			ns

Note) * 7. Typical values at Ta=25℃

* 8. Read Cycle

10. Pin Capacitance

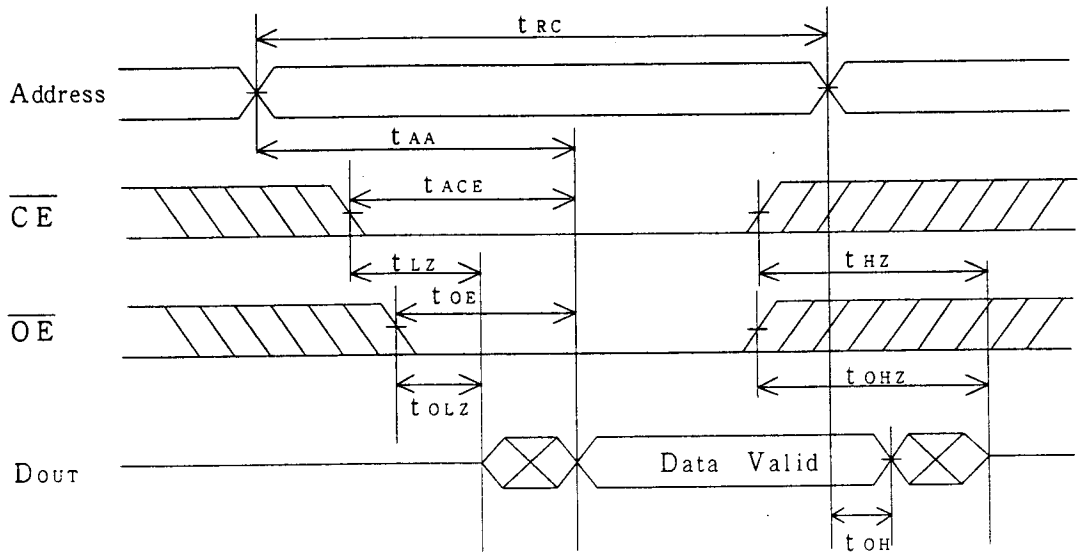
(Ta= 25℃, f = 1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF	* 9
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF	* 9

Note) * 9. This parameter is sampled and not production tested.

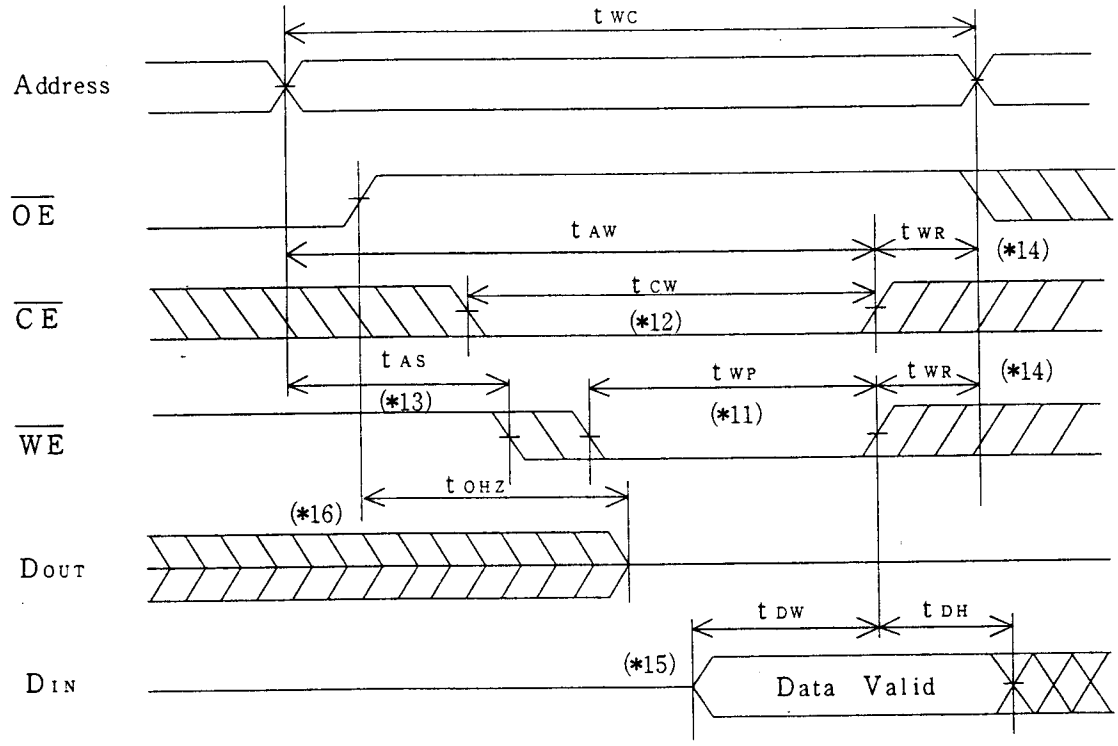
11. Timing Chart

Read cycle timing chart— (*10)

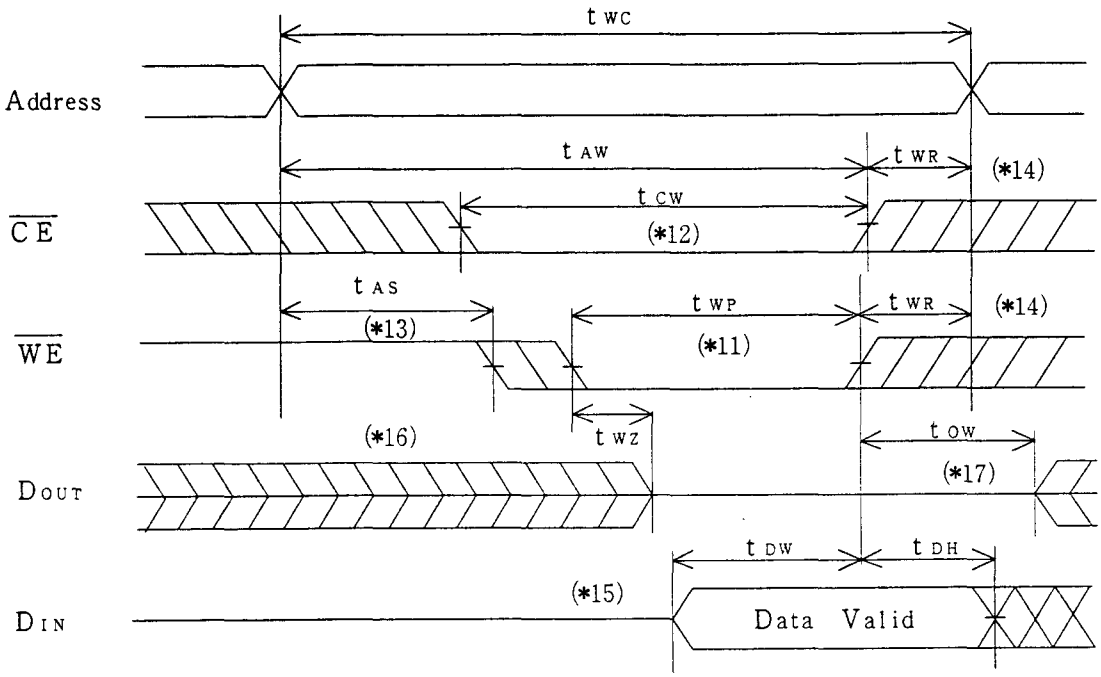


Note) *10. $\overline{WE}$ is high for Read cycle.

Write cycle timing chart— ($\overline{OE}$ Controlled)



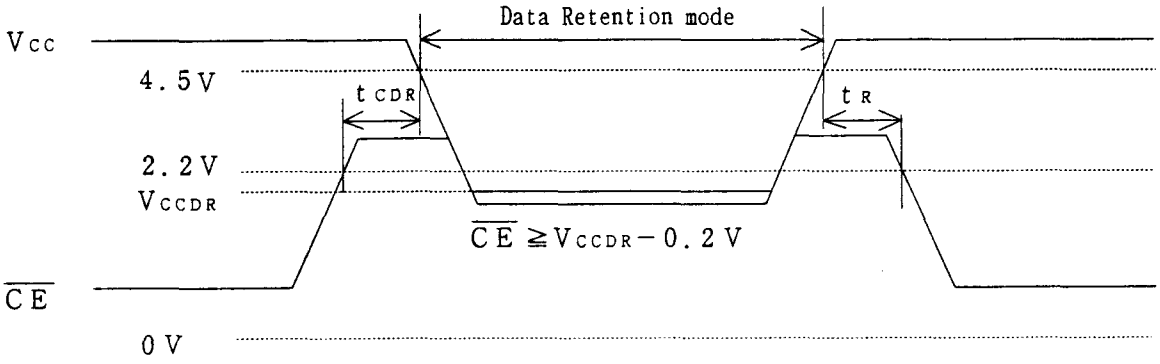
Write cycle timing chart— ($\overline{OE}$ Low fixed)



Note) * 11. A write occurs during the overlap of a low $\overline{CE}$, and a low $\overline{WE}$,
A write begins at the latest transition among $\overline{CE}$ going low, and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE}$ going high, and $\overline{WE}$ going high.
t_{WP} is measured from the beginning of write to the end of write.

* 12. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.
* 13. t_{AS} is measured from the address valid to the beginning of write.
* 14. t_{WR} is measured from the end of write to the address change.
* 15. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
* 16. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
* 17. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.

Data Retention timing chart— $\overline{CE}$ Controlled)



12 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1068

2. Markings

2−1. Marking contents

(1) Product name : LH52256CHT−85LL

(2) Company name : SHARP

(3) Date code

(Example) YY WW ××× Indicates the product was manufactured in the WWth week of 19YY.

→ Denotes the production ref.code (1~3)

→ Denotes the production week. (01,02,03, · · · · · 52,53)

→ Denotes the production year. (Lower two digits of the year.)

(4) The marking of "JAPAN" indicates the country of origin.

2−2. Marking layout

Refer drawing No.AA1068

(This layout do not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3−1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (80devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (800devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

3－2. Outline dimension of tray
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 3 days after opening dry packing.

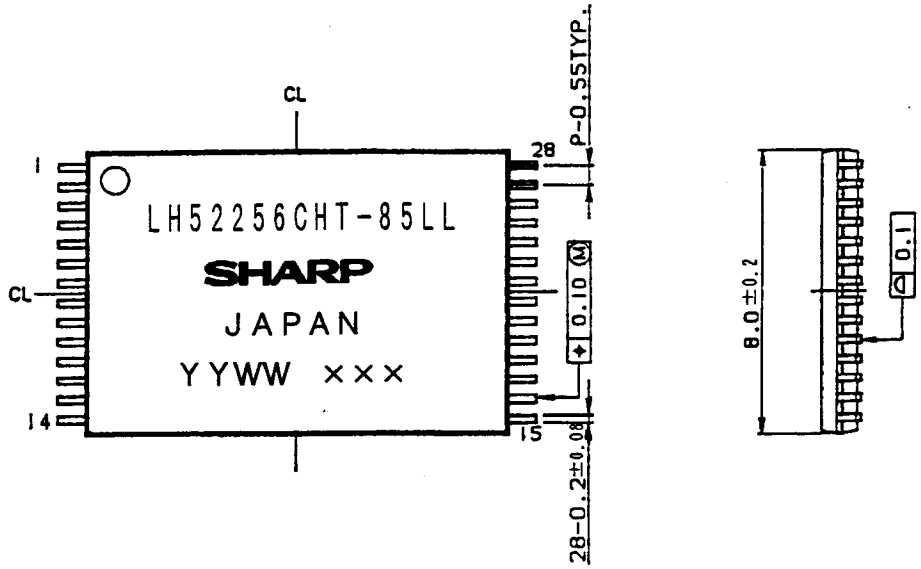
4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16~24 hours at 120℃.
Heat resistance tray is used for shipping tray.

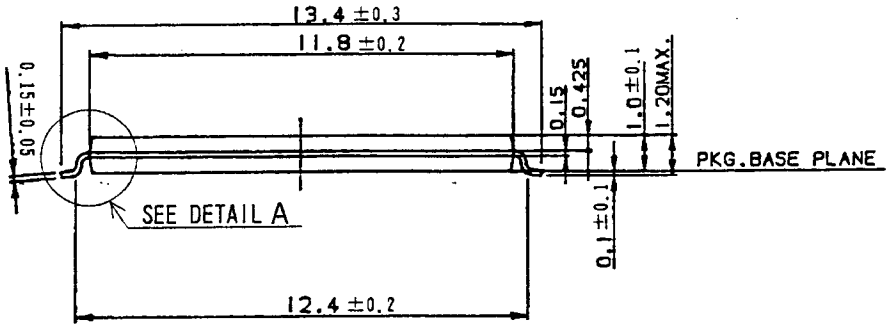
5. Surface Mount Conditions
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

5－1. Soldering conditions (The following conditions are valid only for one time soldering.)

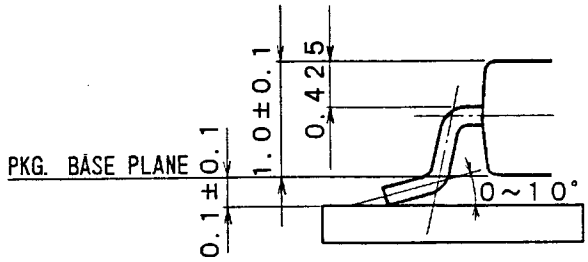
Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 230℃ or less, duration less than 15 seconds. 200℃ or over, duration less than 40 seconds. Temperature increase rate of 1～4℃/second	IC surface
Manual soldering (soldering iron)	260℃ or less, duration less than 10 seconds	IC outer lead surface

5－2. Conditions for removal of residual flux
(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃

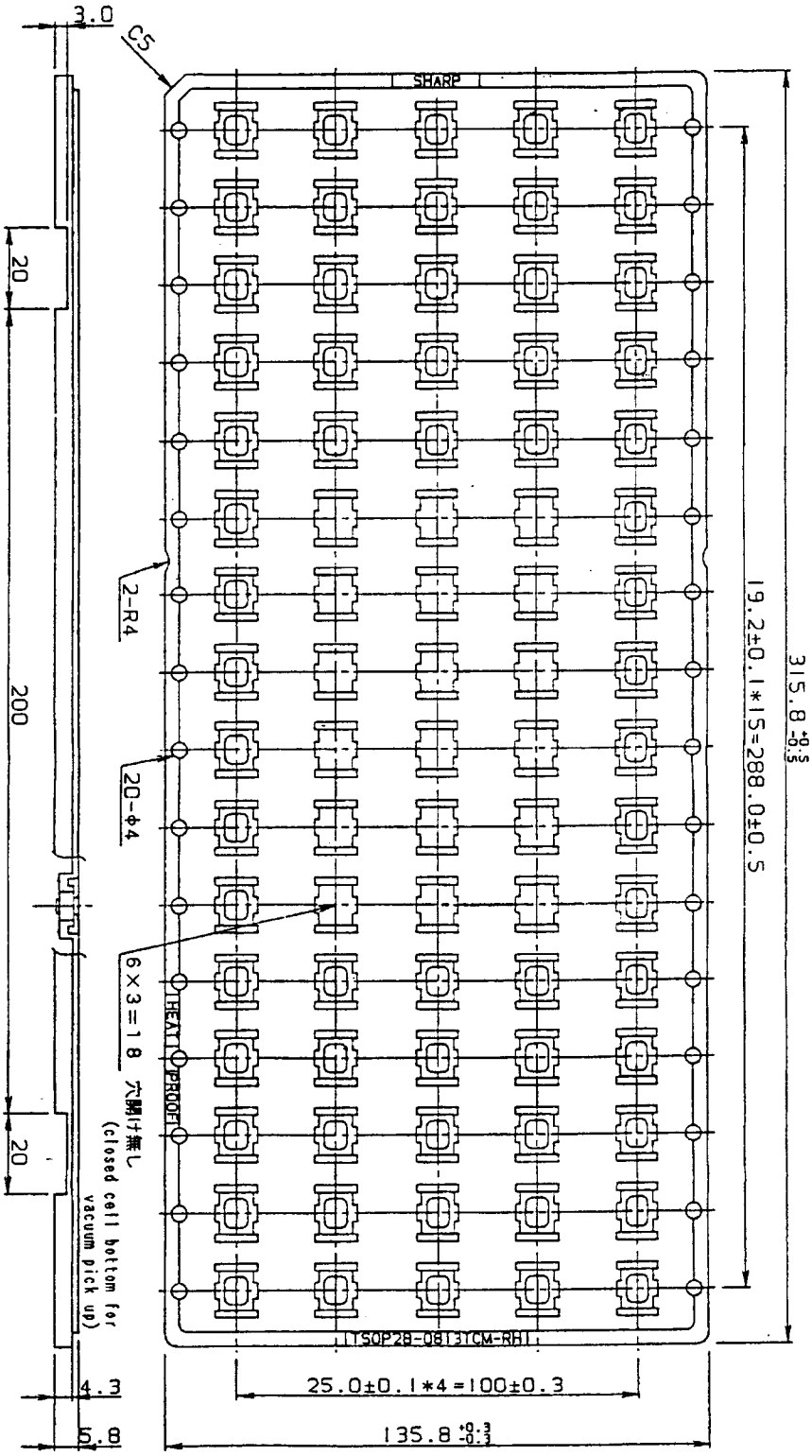




DETAIL A



名称 NAME	TSOP28-P-0813	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。 NOTE Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1068	単位 UNIT	mm	



名称 NAME	TSOP28−0813TCM−RH			備考 NOTE
DRAWING NO.	CV597	単位 UNIT	mm	

STATIC SRAM RAM Random Access Memory Low Power Industrial Temp TSOP LH52256CHT-85LL 256K (32K x 8)