LH543620

1024 × 36 Synchronous FIFO

FEATURES

- Fast Cycle Times: 20/25/30 ns
- Selectable 36/18/9-Bit Word Width for Both Input Port and Output Port
- Byte-Order-Reversal Function (i.e., 'Big-Endian' ↔ 'Little-Endian' Conversion)
- 16-mA-I_{OL} Three-State Outputs
- Automatic Byte Parity Checking
- Selectable Byte Parity Generation
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- All FIFO Status Flags are Synchronous ($\overline{AE}$, $\overline{HF}$, $\overline{AF}$ Through Programming of Control Register)
- Programmed Values may be entered from either Port
- Two Enable Control Signals for each Port
- Mailbox Register with Synchronized Flags
- Asynchronous Data-Bypass Function
- 'Smart' Data-Retransmit Function
- Configurable for Paralleled FIFO Operation (72-Bit Data Width)
- Space-Saving PQFP and TQFP [1] Packages
- PQFP-to-PGA Package Conversion [2]

FUNCTIONAL DESCRIPTION

The LH543620 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 1024 36-bit words. It can replace four or more nine-bit-wide FIFOs in many applications.

The input port and the output port operate independently of each other. Write operations are performed on the rising edge of the input clock CKI, and enabled by two enabled signals ENI_1, ENI_2. Read operations are performed on the rising edge of the output clock CKO and enabled by two enabled signals ENO_1, ENO_2.

Five status flags are available to monitor the memory array status: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flags are initialized to a default offset of eight locations from their respective boundaries, but they are each programmable over the entire FIFO depth.

Both the input port and the output port may be set independently to operate at three data-word widths: 36 bits, 18 bits, or 9 bits. This setting may be changed during system operation. The LH543620 can perform Byte-Order-Reversal on the four nine-bit bytes of each 36-bit data word passing through it, thus accomplishing 'Big Endian' ↔ 'Little Endian' conversion.

When data is read out of the FIFO a byte-parity check is performed. The parity flag is used to indicate that a parity error was detected in one of the 9-bit bytes of the output word.

Parity generation, when selected, creates the parity bit of each 8-bit byte of the input word. The result is written into the MSB-bit of each 9-bit byte, overwriting the previous contents of the bit. The default is odd parity. However, the FIFO may be programmed to use even parity.

The LH543620 has a data-bypass mode that connects the output port to the input port asynchronously. A mailbox facility with Synchronized Flags is provided from the input port to the output port.

The LH543620's 'Smart-Retransmit' capability sets the internal-memory read pointer to any arbitrary memory location. The 'Smart-Retransmit' capability includes a Marking Function and a Programmable Offset to support data communication and digital signal processing applications.

1. This is a final data sheet; except that all references to the TQFP package have Preliminary status.
2. For PQFP-to-PGA conversion for thru-hole board designs, Sharp recommends ITT Pomona Electronics' SMT/PGA Generic Converter model #5853®. This converter maps the LH543620 132-pin PQFP to a generic 13 × 13, 132-pin PGA (100-mil pitch). For more information, contact Sharp or ITT Pomona Electronics at 1500 East Ninth Street, Pomona, CA 91766, (909) 469-2900.

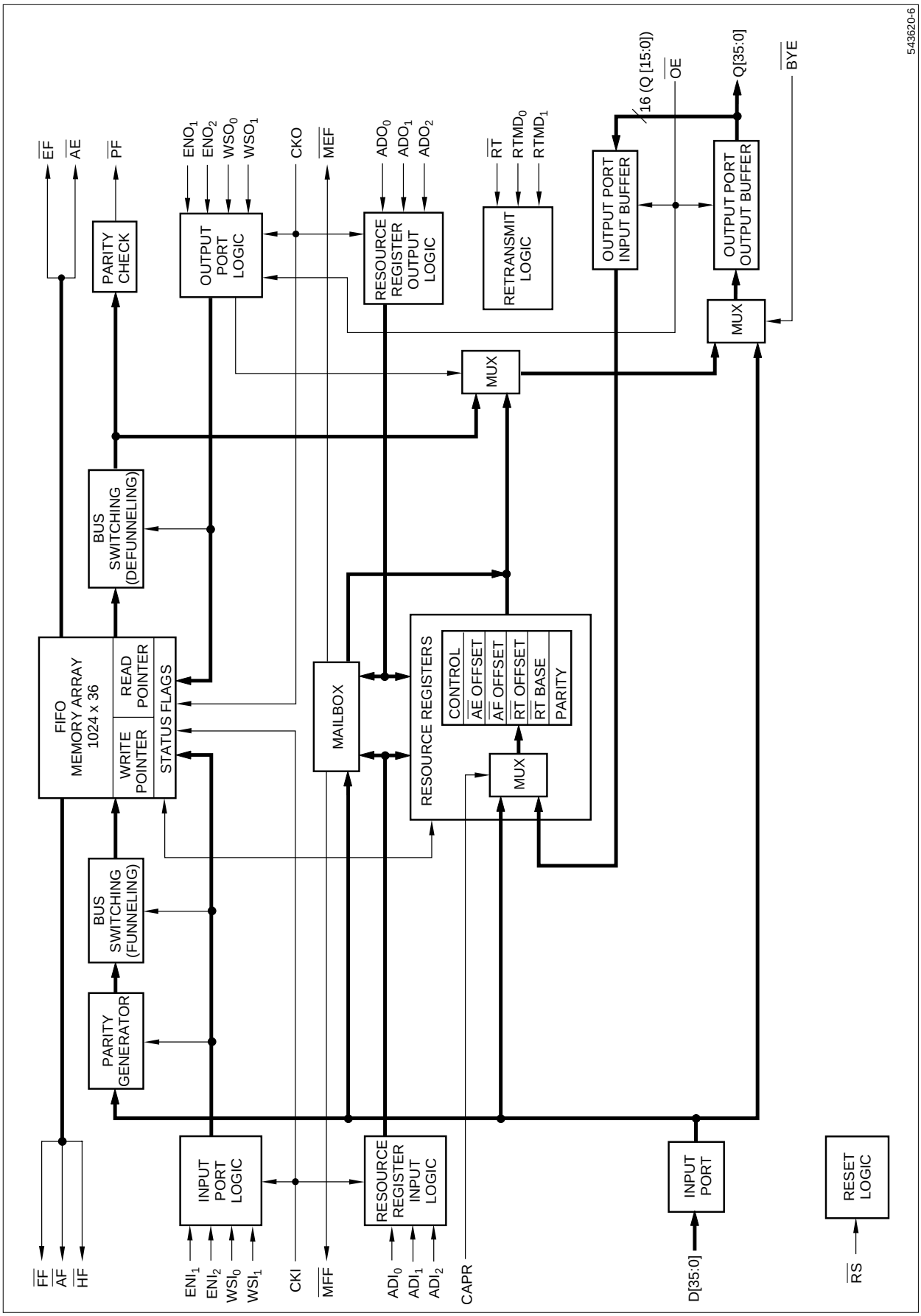


Figure 1. LH543620 Block Diagram

PIN DESCRIPTIONS (SUMMARY)

PIN NAME	PIN TYPE *	DESCRIPTION
DATABUS		
D[35:0]	I	36-Bit Input-Port Databus
Q[15:0]	I/O/Z	Three-State 36-Bit Output-Port Databus
Q[35:16]	O/Z	
CLOCKS		
CKI	I	Input-Port Clock
CKO	I	Output-Port Clock
ASYNCHRONOUS CONTROL		
$\overline{RS}$	I	Master Reset
$\overline{OE}$	I	Output Enable
$\overline{BYE}$	I	Data-Bypass Enable
CAPR	I	Command-Address Port Reference
CONTROL SIGNALS SYNCHRONOUS TO THE INPUT CLOCK		
ENI_1,ENI_2	I	Input-Port Enables
ADI[2:0]	I	Input-Port Address
WSI[1:0]	I	Input-Port Word-Width Selection
STATUS FLAGS SYNCHRONOUS TO THE INPUT CLOCK		
$\overline{FF}$	O	Full Flag
$\overline{AF}$	O	Almost-Full Flag
$\overline{HF}$ [1]	O	Half-Full Flag
$\overline{MFF}$	O	Mailbox-Full Flag

PIN NAME	PIN TYPE *	DESCRIPTION
CONTROL SIGNALS SYNCHRONOUS TO THE OUTPUT CLOCK		
ENO_1,ENO_2	I	Output-Port Enables
ADO[2:0]	I	Output-Port Address
WSO[1:0]	I	Output-Port Word-Width Selection
RTMD[1:0]	I	Retransmit Mode Control
$\overline{RT}$	I	Retransmit
STATUS FLAGS SYNCHRONOUS TO THE OUTPUT CLOCK		
$\overline{AE}$	O	Almost-Empty Flag
$\overline{EF}$	O	Empty Flag
$\overline{PF}$	O	Parity-Error Flag
$\overline{MEF}$	O	Mailbox-Empty Flag
VOLTAGES AND GROUNDS		
V_{CC}	V	Positive Power
V_{SS}	V	Ground

* I = Input, O = Output, V = Voltage, Z = High-Impedance

1. The half-full flag is user-selectable to be synchronized to either CKI or CKO.

PIN CONNECTIONS

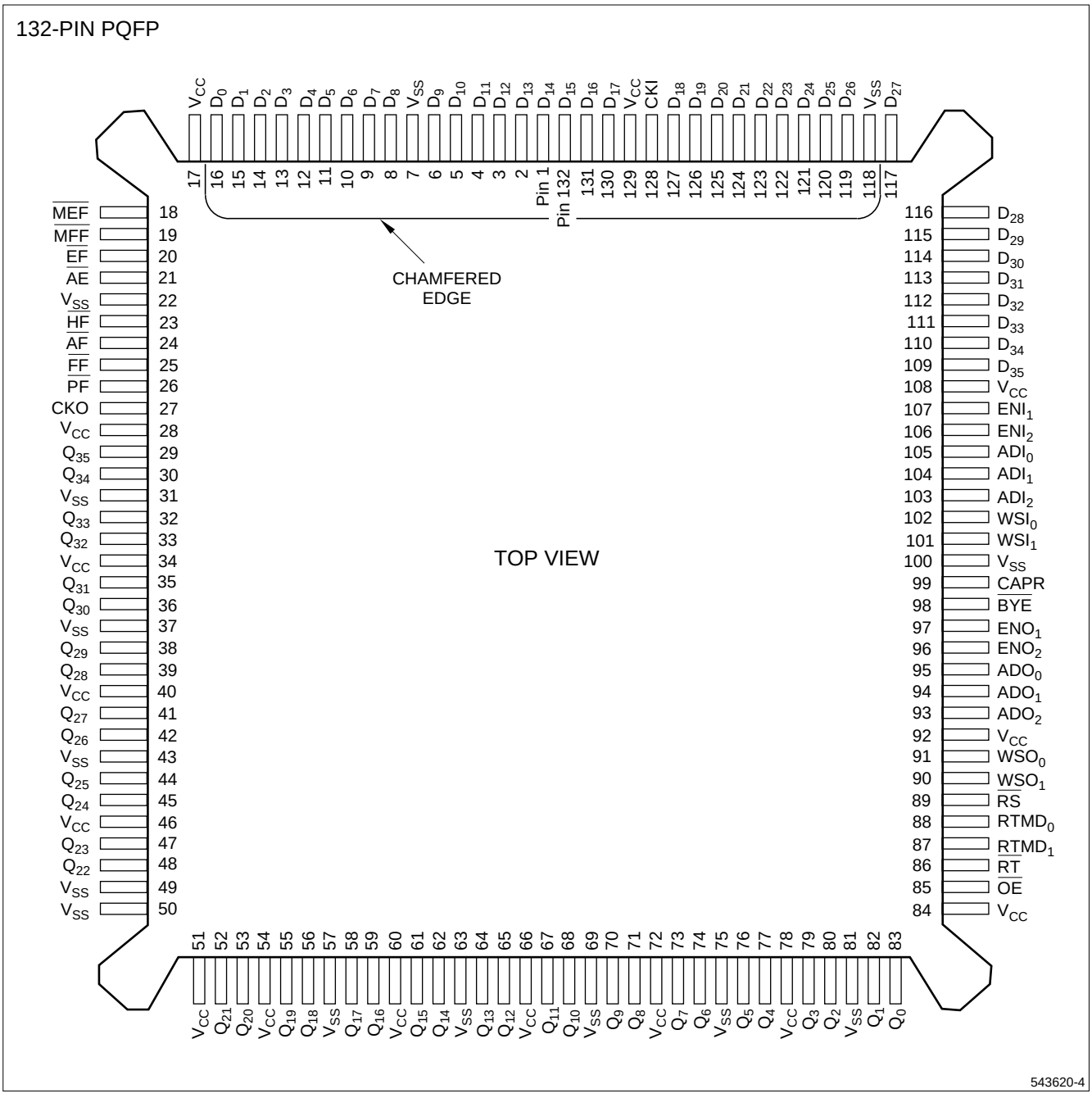


Figure 2. Pin Connections for 132-Pin PQFP Package (Top View)

PIN LIST

PIN NAME	PIN NO.
D_{14}	1
D_{13}	2
D_{12}	3
D_{11}	4
D_{10}	5
D_9	6
D_8	8
D_7	9
D_6	10
D_5	11
D_4	12
D_3	13
D_2	14
D_1	15
D_0	16
$\overline{MEF}$	18
$\overline{MFF}$	19
$\overline{EF}$	20
$\overline{AE}$	21
$\overline{HF}$	23
$\overline{AF}$	24
$\overline{FF}$	25
$\overline{PF}$	26
CKO	27
Q_{35}	29
Q_{34}	30
Q_{33}	32
Q_{32}	33
Q_{31}	35
Q_{30}	36
Q_{29}	38
Q_{28}	39
Q_{27}	41
Q_{26}	42
Q_{25}	44
Q_{24}	45
Q_{23}	47
Q_{22}	48
Q_{21}	52
Q_{20}	53
Q_{19}	55
Q_{18}	56
Q_{17}	58
Q_{16}	59

PIN NAME	PIN NO.
Q_{15}	61
Q_{14}	62
Q_{13}	64
Q_{12}	65
Q_{11}	67
Q_{10}	68
Q_9	70
Q_8	71
Q_7	73
Q_6	74
Q_5	76
Q_4	77
Q_3	79
Q_2	80
Q_1	82
Q_0	83
$\overline{OE}$	85
$\overline{RT}$	86
$RTMD_1$	87
$RTMD_0$	88
$\overline{RS}$	89
WSO_1	90
WSO_0	91
ADO_2	93
ADO_1	94
ADO_0	95
ENO_2	96
$EN0_1$	97
$\overline{BYE}$	98
CAPR	99
WSI_1	101
WSI_0	102
ADI_2	103
ADI_1	104
ADI_0	105
ENI_2	106
ENI_1	107
D_{35}	109
D_{34}	110
D_{33}	111
D_{32}	112
D_{31}	113
D_{30}	114
D_{29}	115

PIN NAME	PIN NO.
D_{28}	116
D_{27}	117
D_{26}	119
D_{25}	120
D_{24}	121
D_{23}	122
D_{22}	123
D_{21}	124
D_{20}	125
D_{19}	126
D_{18}	127
CKI	128
D_{17}	130
D_{16}	131
D_{15}	132
V_{SS}	7
V_{CC}	17
V_{SS}	22
V_{CC}	28
V_{SS}	31
V_{CC}	34
V_{SS}	37
V_{CC}	40
V_{SS}	43
V_{CC}	46
V_{SS}	49
V_{SS}	50
V_{CC}	51
V_{CC}	54
V_{SS}	57
V_{CC}	60
V_{SS}	63
V_{CC}	66
V_{SS}	69
V_{CC}	72
V_{SS}	75
V_{CC}	78
V_{SS}	81
V_{CC}	84
V_{CC}	92
V_{SS}	100
V_{CC}	108
V_{SS}	118
V_{CC}	129

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	–0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	–0.5 V to V_{CC} + 0.5 V
DC Output Current [3]	± 75 mA
Storage Temperature Range	–65°C to 150°C
Power Dissipation (Package Limit)	2.5 Watts (Quad Flat Pack)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	–0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	Vcc + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V To V_{CC}	–10		10	µA
I_{LO}	I/O Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	–10		10	µA
V_{OL}	Logic LOW Output Voltage	I_{OL} = 16.0 mA			0.4	V
V_{OH}	Logic HIGH Output Voltage	I_{OH} = –8.0 mA	2.4			V
I_{CC}	Average Supply Current [1,2]	Measured at f_C = maximum		205	380	mA
I_{CC2}	Average Standby Supply Current [1,3]	All Inputs = V_{IHMIN} (Clock idle)		40	85	mA
I_{CC3}	Power-Down Supply Current [1]	All Inputs = V_{CC}, Outputs – open, Control – deasserted, Clocks = V_{CC}		0.01	1.0	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading, and I_{CC} is also dependent on cycle times. Specified values are with outputs open (for I_{CC}: C_L = 0 pF); and, for I_{CC}, operating at minimum cycle times.
2. I_{CC} (MAX): Using worst case conditions and data pattern. I_{CC} (TYP): Using V_{CC} = 5 V and average data pattern.
3. I_{CC2} (TYP): Using V_{CC} = 5 V and T_A = 25°C.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	3 ns
Output Reference Levels	1.5 V
Input Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX. (Input Capacitance)	8 pF
C_{OUT} MAX. (Output Capacitance)	10 pF

NOTES:
1. Sample tested only.
2. Capacitances are maximum values at 25^0C, measured at 1.0 MHz, with V_{IN} = 0 V.

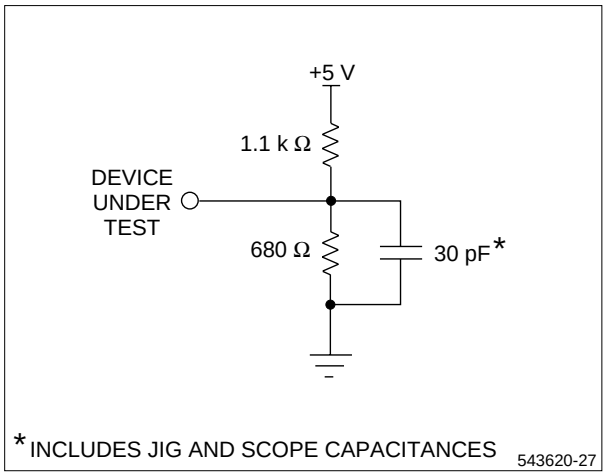


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (See Timing Diagrams Pages 21-35)

SYMBOL	DESCRIPTION	–20		–25		–30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Clock Cycle Frequency		50		40		33	MHz
t_C	Clock Cycle Time	20		25		30		ns
t_{CH}	Clock HIGH Time	8		10		12		ns
t_{CL}	Clock LOW Time	9		12		14		ns
t_{DS}	Data In Setup Time	5		6		7		ns
t_{DSO}	Data Setup Time When Writing to Resource Register From Output Port	10		12		14		ns
t_{DH}	Data In Hold Time	2		2		2		ns
t_{DHO}	Data Hold Time When Writing to Resource Register From Output Port	2		2		2		ns
t_A	Data Out Access Time		14		16		18	ns
t_{OH}	Data Out Hold Time	4		4		4		ns
t_{ES}	Enable Setup Time	5		6		7		ns
t_{EH}	Enable Hold Time	2		2		2		ns
t_{OES}	Output Enable Setup Time	6		7		8		ns
t_{OEH}	Output Enable Hold Time	2		2		2		ns
t_{OL}	$\overline{OE}$ to Data Out Low-Z [2]	1		1		1		ns
t_{OZ}	$\overline{OE}$ to Data Out High-Z [2]		12		15		19	ns
t_{OE}	$\overline{OE}$ to Data Valid		10		12		14	ns
t_{EF}	Empty Flag Access Time		14		16		18	ns
t_{FF}	Full Flag Access Time		14		16		18	ns
t_{AE}	$\overline{AE}$ Flag Access Time		14		16		18	ns
t_{AF}	$\overline{AF}$ Flag Access Time		14		16		18	ns
t_{HF}	$\overline{HF}$ Flag Access Time		14		16		18	ns
t_{PF}	Parity Flag Access Time		14		16		18	ns
t_{MFF}	Mailbox $\overline{FF}$ Access Time		14		16		18	ns
t_{MEF}	Mailbox $\overline{EF}$ Access Time		14		16		18	ns
t_{AS}	Address Setup Time	10		12		14		ns
t_{AH}	Address Hold Time	2		2		2		ns
t_{WSS}	WSI and WSO Setup Time	10		12		14		ns
t_{WSH}	WSI and WSO Hold Time	2		2		2		ns
t_{RTMS}	Retransmit Mode Setup Time	5		6		7		ns
t_{RTMH}	Retransmit Mode Hold Time	2		2		2		ns
t_{RTS}	Retransmit Setup Time	5		6		7		ns
t_{RTH}	Retransmit Hold Time	2		2		2		ns
t_{RS}	Reset Pulse Width	20		25		30		ns
t_{RSR}	Reset Recovery Time [2]	10		12		15		ns
t_{RF}	Reset LOW to Flag Valid		30		35		40	ns
t_{RO}	Reset to Data Out LOW		18		20		22	ns
t_{BA}	Bypass LOW to Data Valid		12		16		18	ns
t_{BD}	Bypass Propagation Delay		12		16		18	ns
t_{SKEW1}	Skew Time Between CKO and CKI for $\overline{FF}$ [3]	7		9		11		ns
t_{SKEW2}	Skew Time Between CKI and CKO for $\overline{EF}$ [4]	7		9		11		ns
t_{SKEWM}	Skew Time Between Clock for Mailbox Flags	7		9		11		ns

NOTES:

PIN DESCRIPTIONS (FUNCTIONAL)

PIN NAME	DESCRIPTION
	DATABUS
D[35:0]	**36-bit Input-Port Databus.** The D port is the input port for the FIFO memory array, the resource registers, and the mailbox, or it may be directly connected to the output port. See Figure 4. D[35:0] is synchronous to the rising edge of CKI.
Q[35:0]	**Three-State 36-Bit Output-Port Databus.** The Q port is the output port for the FIFO memory array, the resource registers, and the mailbox, or it may be directly connected to the input port. See Figure 4. Q[35:0] is synchronous to the rising edge of CKO. The lower 16 bits of the Q port (Q[15:0]) may also be used as the input port for the resource register.
	CLOCKS
CKI	**Input-Port Clock.** CKI is a free-running waveform controlled by an oscillator. It may be irregular or asynchronous if minimum clock-HIGH times and clock-LOW times are met.
CKO	**Output-Port Clock.** CKO is a free-running waveform controlled by an oscillator. It may be irregular or asynchronous if minimum clock-HIGH times and clock-LOW times are met.

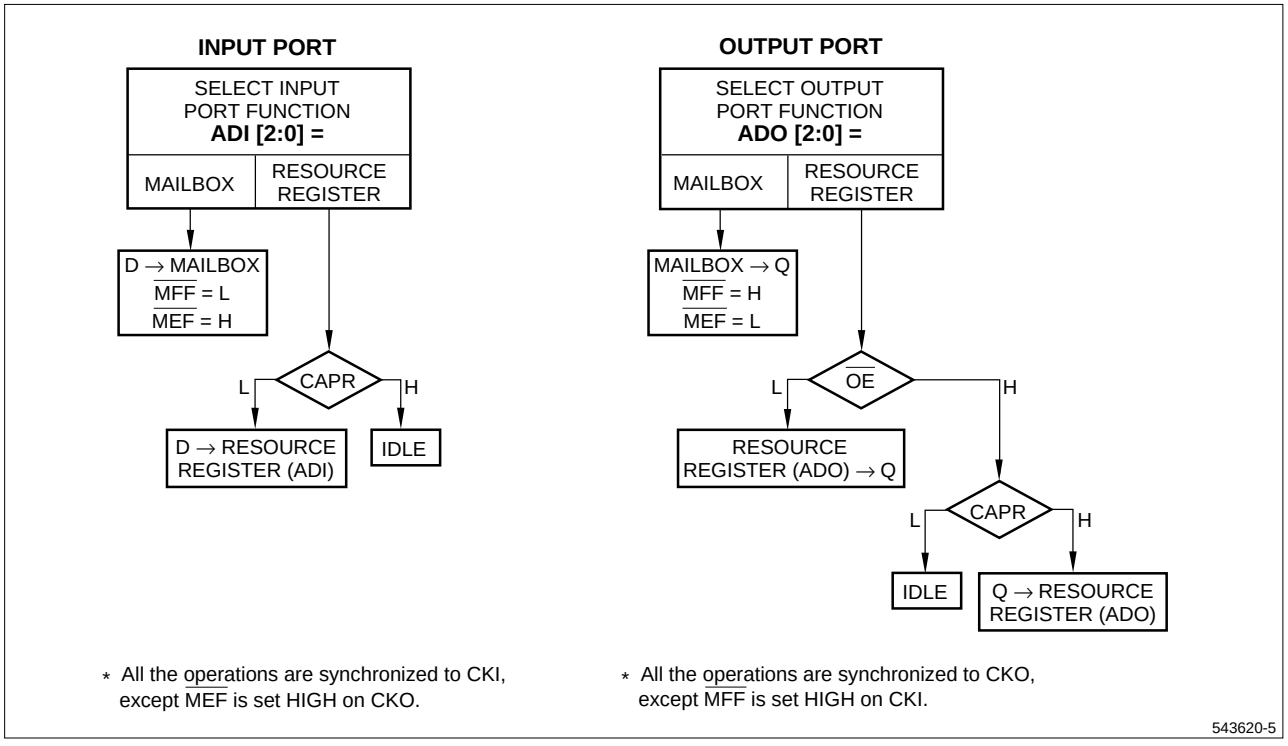


Figure 4. Resource Registers, Read and Write

PIN NAME	DESCRIPTION
	ASYNCHRONOUS CONTROL
$\overline{RS}$	**Master Reset.** When asserted LOW, the LH543620 internal resource registers are set to their default value. See Table 1. The status flags indicate Empty FIFO.
$\overline{OE}$	**Output Enable.** When asserted LOW, $\overline{OE}$ forces Q[35:0] to be active. When deasserted HIGH, $\overline{OE}$ forces Q[35:0] into a Hi-Z state. Bit 6 of the control register governs whether $\overline{OE}$ suppresses the advancement of the Read Pointer (RP). In this case, $\overline{OE}$ must obey setup time and hold time relative to CKO.
$\overline{BYE}$	**Data-Bypass Enable.** When asserted LOW, $\overline{BYE}$ connects Q[35:0] directly to D[35:0].
CAPR	**Command-Address Port Reference.** CAPR determines the source of the 16-bit word to be loaded into the resource register. Whenever CAPR is LOW, the word comes from the Input Port. Whenever CAPR is HIGH ($\overline{OE}$ is HIGH), the word comes from the Output Port. **NOTES**: 1. The destination of the resource register is always the Output Port. 2. CAPR is assumed to be a steady signal. It is not allowed to change 'on-the-fly' during operation.
	CONTROL SIGNALS SYNCHRONOUS TO THE INPUT CLOCK
ENI_1, ENI_2	**Input-Port Enables.** ENI_1 and ENI_2 are active HIGH and synchronous to the rising edge of CKI. Data is written into the FIFO memory array when both ENI_1 and ENI_2 are asserted HIGH. **NOTE:** ENI_1, ENI_2 DO NOT ENABLE writing data into the Resource Registers or the Mailbox.
ADI[2:0]	**Input-Port Address.** ADI[2:0] specifies the Input-Port destination. See Table 1. ADI[2:0] is synchronized to the rising edge of CKI.
WSI[1:0]	**Input-Port Word-Width Selection.** WSI[1:0] selects the Input-Port Word-Width. See Table 2. WSI[1:0] is synchronous to the rising edge of CKI.

Table 1. Input-Port Address

ADI_2	ADI_1	ADI_0	SELECTION	DEFAULT VALUE (of the selected REGISTER)
L	L	L	RBASE register	0
L	L	H	ROFFSET register	0
L	H	L	$\overline{AF}$ offset value	8
L	H	H	Parity register	0
H	L	L	$\overline{AE}$ offset value	8
H	L	H	Control register	1
H	H	L	Mailbox	0
H	H	H	Resource registers write disabled	

Table 2. Input-Port Word-Width Selection

WSI_1	WSI_0	FUNCTION	
L	L	9-Bit Data-Path Width	Input data D[8:0]
L	H	18-Bit Data-Path Width	Input data D[17:0]
H	L	Reserved	
H	H	36-Bit Data-Path Width	Input data D[35:0]

PIN NAME	DESCRIPTION
	STATUS FLAGS SYNCHRONOUS TO THE INPUT CLOCK
$\overline{FF}$	**Full Flag.** $\overline{FF}$ is synchronous to the rising edge of CKI. When asserted LOW, 1024 36-bit words of the FIFO memory array contain meaningful data. When $\overline{FF}$ is asserted, writing data to the FIFO is disabled.
$\overline{AF}$	**Almost-Full Flag.** When asserted LOW, $\overline{AF}$ indicates that there are at most 'p' vacant 36-bit words remaining in the FIFO memory array, where 'p' is the value of the Almost-Full-Offset-Value. $\overline{AF}$ has two synchronization modes depending on Bit 5 of the control register. *Bit 5 = 0* (Default) Asynchronous Mode *Bit 5 = 1*: $\overline{AF}$ is synchronous to the rising edge of CKI.
$\overline{HF}$	**Half-Full Flag.** When asserted LOW, there are at least 513 36-bit words in the FIFO memory array. $\overline{HF}$ has three synchronization modes depending on Bits 3 and 4 of the control register. See Table 3.
$\overline{MFF}$	**Mailbox-Full Flag.** $\overline{MFF}$ is synchronized to the rising edge of CKI. When asserted LOW, it indicates that a new mail word has been placed in the mailbox.
	CONTROL SIGNALS SYNCHRONOUS TO THE OUTPUT CLOCK
ENO_1, ENO_2	**Output-Port Enables.** ENO_1 and ENO_2 are active HIGH, synchronous to the rising edge of CKO. Data is read from the FIFO memory array when both ENO_1, ENO_2 are asserted. **NOTE:** ENO_1, ENO_2 DO NOT ENABLE reading data from the Resource Register or the Mailbox.
ADO[2:0]	**Output-Port Address.** ADO[2:0] specifies the Output-Port source/destination. See Table 4. ADO[2:0] is synchronous to the rising edge of CKO. **NOTE:** In order to read the resource register at the output bus, $\overline{BYE}$ should be deasserted and the FIFO memory array should be disabled.

Table 3. $\overline{HF}$ Synchronization Modes

CONTROL REGISTER		FUNCTION
BIT 4	BIT 3	
L *	L *	Asynchronous Mode: $\overline{HF}$
L	H	Synchronous Mode I: $\overline{HF}$ is synchronous to the rising edge of CKO
H	L	Synchronous Mode II: $\overline{HF}$ is synchronous to the rising edge of CKI
H	H	

* Default Mode

Table 4. Output-Port Address

ADO_2	ADO_1	ADO_0	SELECTION	DEFAULT VALUE (of the selected REGISTER)
L	L	L	RBASE register	0
L	L	H	ROFFSET register	0
L	H	L	$\overline{AF}$ offset value	8
L	H	H	Parity register	0
H	L	L	$\overline{AE}$ offset value	8
H	L	H	Control register	1
H	H	L	Mailbox	0
H	H	H	Resource registers read disabled	Not applicable

PIN NAME	DESCRIPTION
CONTROL SIGNALS SYNCHRONOUS TO THE OUTPUT CLOCK (cont'd)	
WSO[1:0]	**Output-Port Word-Width Selection.** WSO[1:0] is synchronous to the rising edge of CKO. WSO[1:0] selects the Output-Port Word-Width and controls byte-order-reversal according to Table 5.
RTMD[1:0]	**Retransmit Mode Control.** RTMD[1:0] is synchronized to the rising edge of CKO. RTMD[1:0] controls the placement of new contents into the Read Pointer (RP) and/or the Retransmit Base (RBASE) registers. Whenever Retransmit ($\overline{RT}$) is asserted, one of three operations is performed according to the setting of RTMD[1:0]. See Table 6. **NOTES:** 1. When RTMD[1:0] is set to 0, the FIFO is in depth cascade mode, and the Retransmit mechanism can not be used. In cascade mode, the Almost-Empty Flag is a handshake signal for cascading. The Almost-Empty Flag is used as an input to the ENI of the next FIFO in the chain. 2. In standard FIFO operation RTMD[1:0] must not be set to 0 and the Retransmit signal must be HIGH.
$\overline{RT}$	**Retransmit.** $\overline{RT}$ is synchronized to the rising edge of CKO. When asserted LOW, $\overline{RT}$ causes one of the Retransmit Mode operations to be performed, according to the encoding of RTMD[1:0]. See Table 6. **NOTE**: When RTMD[1:0] = 0 (FIFO is in cascade mode) $\overline{RT}$ is ignored.

Table 5. Output-Port Word-Width Selection

WSO_1	WSO_0	FUNCTION	
L	L	9-Bit Data-Path Width	Output data Q[8:0]
L	H	18-Bit Data-Path Width	Output data Q[17:0]
H	L	36-Bit Data-Path Width With Byte-Order-Reversal	Output data Q[35:0]
H	H	36-Bit Data-Path Width	Output data Q[35:0]

Table 6. Retransmit Operation Modes

$RTMD_1$	$RTMD_0$	OPERATION	ACTION TAKEN
L	L	Depth Cascade Mode	The Almost-Empty Flag is a handshake signal for cascading
L	H	Retransmit	(RBASE) + (ROFFSET) → RP
H	L	Retransmit and Mark	(RBASE) + (ROFFSET) → RP and (RBASE) + (ROFFSET) → RBASE
H	H	Mark	(RP) → RBASE

PIN NAME	DESCRIPTION
	STATUS FLAGS SYNCHRONOUS TO THE OUTPUT CLOCK
$\overline{AE}$	**Almost-Empty Flag.** The $\overline{AE}$ flag has two modes of operation depending on the RTMD[1:0] setting. **1. RTMD[1:0] ≠ 0:** $\overline{AE}$ is a standard Almost-Empty Flag. When asserted LOW, $\overline{AE}$ implies that there are at most 'q' 36-bit words in the FIFO memory array, where 'q' is Almost-Empty-Offset-Value register value. In this mode $\overline{AE}$ has two synchronization options depending on the setting of Bit 2 of the control register. *Bit 2 = 0* (Default) Asynchronous Mode *Bit 2 = 1* Synchronous Mode: $\overline{AE}$ is synchronous to the rising edge of CKO. **2. RTMD[1:0] = 0:** $\overline{AE}$ is a handshake signal for cascading.
$\overline{EF}$	**Empty Flag.** $\overline{EF}$ is synchronous to the rising edge of CKO. When asserted LOW, all 1024 36-bit words are vacant. When asserted, $\overline{EF}$ disables the FIFO Read operation.
$\overline{PF}$	**Parity-Error Flag.** $\overline{PF}$ is synchronized to the rising edge of CKO. When asserted LOW, $\overline{PF}$ implies that a parity error has occurred in at least one 9-bit byte within a 36-bit word read from the FIFO memory array. If there are no errors, it is deasserted HIGH. When an error is detected, the parity check result of each 9-bit byte of the 36-bit output word is written to the parity register. The content of the parity register is frozen until read. The $\overline{PF}$ signal is delayed by one CKO cycle compared to the output data (i.e., if the $\overline{PF}$ is asserted, there was an error in the previous word).
$\overline{MEF}$	**Mailbox-Empty Flag.** $\overline{MEF}$ is synchronous to the rising edge of CKO. When asserted LOW, $\overline{MEF}$ indicates that there is no new mail word in the mailbox.
	VOLTAGES AND GROUNDS
V_{CC}	**Positive Power.**
V_{SS}	**Ground.**

OPERATIONAL DESCRIPTION

The LH543620 has four operating modes: Normal Mode, Programmable Resource Registers, Mailbox, and Data Bypass.

NORMAL MODE

Normal FIFO operation refers to Read and Write operations to the FIFO memory array. Data Write operations into the FIFO memory array occur at the rising edge of CKI. The operation is enabled if both ENI_1 and ENI_2 are asserted HIGH. Data Read operations from the FIFO memory occur at the rising edge of CKO. The operation is enabled if both ENO_1 and ENO_2 are asserted HIGH.

The FIFO write and read operations are supported by the following mechanisms: Byte-Order-Reversal and Bus Funneling/Defunneling Functions, Status Flags, Retransmit Mechanism, Parity Checking, and Parity Generation.

Byte-Order-Reversal and Bus Funneling/ Defunneling Functions

Word width can be selected at the Input Port and/or the Output Port to be 36, 18 or 9 bits wide. When the Output Port width is selected to be 36 bits, it is possible to select Byte-Order-Reversal.

The funneling mechanism is controlled by the inputs WSI[1:0] and WSO[1:0] according to Tables 2 and 5. Data is packed and unpacked from a 36-bit word memory array. Table 7 describes all combinations of funneling/defunneling.

Changes to the funneling/defunneling settings during system operation should be made one clock before a word boundary, as shown in Example 3.

Example 1: 36-to-9 Funneling

CONDITIONS		RESULTS
WSI[1:0]	WSO[1:0]	
3	–	Input 36 bits wide.
–	0	Output 9 bits wide. Pins used are Q[8:0].

The dataflow structure is illustrated by Figure 5.

Example 2: 18-to-36 Defunneling With Byte Reversal

This example performs two functions:

1. Bus width change
2. Big Endian to Little Endian conversion

This configuration can be used for connecting the Intel 80286 to the Motorola 68040.

CONDITIONS		RESULTS
WSI[1:0]	WSO[1:0]	
1	–	Input 18 bits wide. Pins used are D[17:0].
–	2	Output 36 bits wide with byte order reversal.

The dataflow structure is illustrated by Figure 6.

Example 3: Changing Input Bus Width From 9 to 36 During Operation

CKI	WSI	ACTION
0	0	Write 1st 9-bit byte
1	0	Write 2nd 9-bit byte
2	0	Write 3rd 9-bit byte
3	3	Write 4th 9-bit byte
4	3	Write 1st 36-bit word

Table 7. Bus Funneling/Defunneling *

INPUT					OUTPUT																
CKI	WSI = 0				CKO	WSO = 3				WSO = 2				WSO = 1				WSO = 0			
cycles	D[35:9]			D[8:0]	cycles	Q[35:0]				Q[35:0]				Q[35:18]		Q[17:0]		Q[35:9]			Q[8:0]
0	xxx			**B0**	0	**B3**	**B2**	**B1**	**B0**	**B0**	**B1**	**B2**	**B3**	B3	B2	**B1**	**B0**	B3	B2	B1	**B0**
1	xxx			**B1**	1	**B7**	**B6**	**B5**	**B4**	**B4**	**B5**	**B6**	**B7**	B1	B0	**B3**	**B2**	B0	B3	B2	**B1**
2	xxx			**B2**	2									B7	B6	**B5**	**B4**	B1	B0	B3	**B2**
3	xxx			**B3**	3									B5	B4	**B7**	**B6**	B2	B1	B0	**B3**
4	xxx			**B4**	4													B7	B6	B5	**B4**
5	xxx			**B5**	5																
6	xxx			**B6**	6																
7	xxx			**B7**	7																
8	xxx			**B8**	8																
	WSI = 1					**WSO = 3**				**WSO = 2**				**WSO = 1**				**WSO = 0**			
	D[35:18]		**D[17:0]**			**Q[35:0]**				**Q[35:0]**				Q[35:18]		**Q[17:0]**		Q[35:9]			**Q[8:0]**
0	xx		**B1**	**B0**	0	**B3**	**B2**	**B1**	**B0**	**B0**	**B1**	**B2**	**B3**	B3	B2	**B1**	**B0**	B3	B2	B1	**B0**
1	xx		**B3**	**B2**	1	**B7**	**B6**	**B5**	**B4**	**B4**	**B5**	**B6**	**B7**	B1	B0	**B3**	**B2**	B0	B3	B2	**B1**
2	xx		**B5**	**B4**	2									B7	B6	**B5**	**B4**	B1	B0	B3	**B2**
3	xx		**B7**	**B6**	3									B5	B4	**B7**	**B6**	B2	B1	B0	**B3**
4	xx		**B9**	**B8**	4													B7	B6	B5	**B4**
	WSI = 3					**WSO = 3**				**WSO = 2**				**WSO = 1**				**WSO = 0**			
	D[35:0]					**Q[35:0]**				**Q[35:0]**				Q[35:18]		**Q[17:0]**		Q[35:9]			**Q[8:0]**
0	**B3**	**B2**	**B1**	**B0**	0	**B3**	**B2**	**B1**	**B0**	**B0**	**B1**	**B2**	**B3**	B3	B2	**B1**	**B0**	B3	B2	B1	**B0**
1	**B7**	**B6**	**B5**	**B4**	1	**B7**	**B6**	**B5**	**B4**	**B4**	**B5**	**B6**	**B7**	B1	B0	**B3**	**B2**	B0	B3	B2	**B1**
														B7	B6	**B5**	**B4**	B1	B0	B3	**B2**
														B5	B4	**B7**	**B6**	B2	B1	B0	**B3**
																		B7	B6	B5	**B4**

* **NOTE:** B0, B1, . . ., represent data bytes.

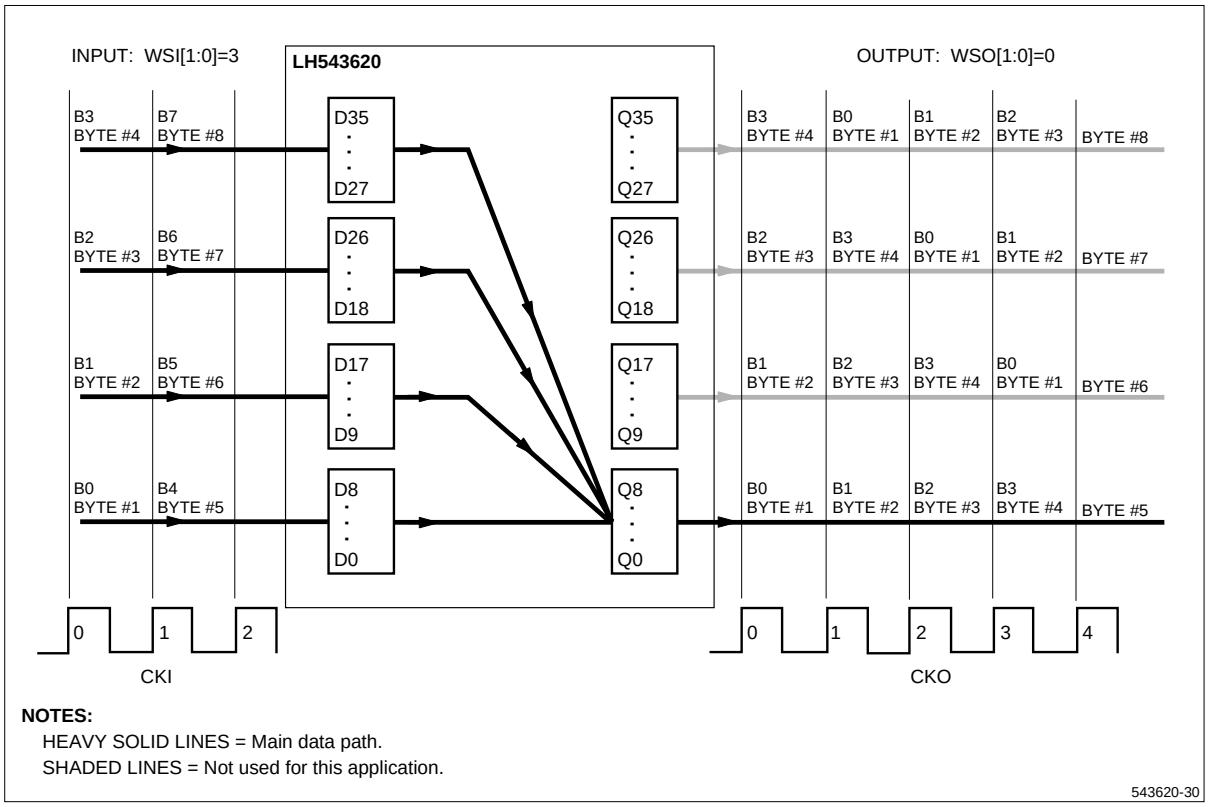


Figure 5. Example of 36-to-9 Bus Funneling

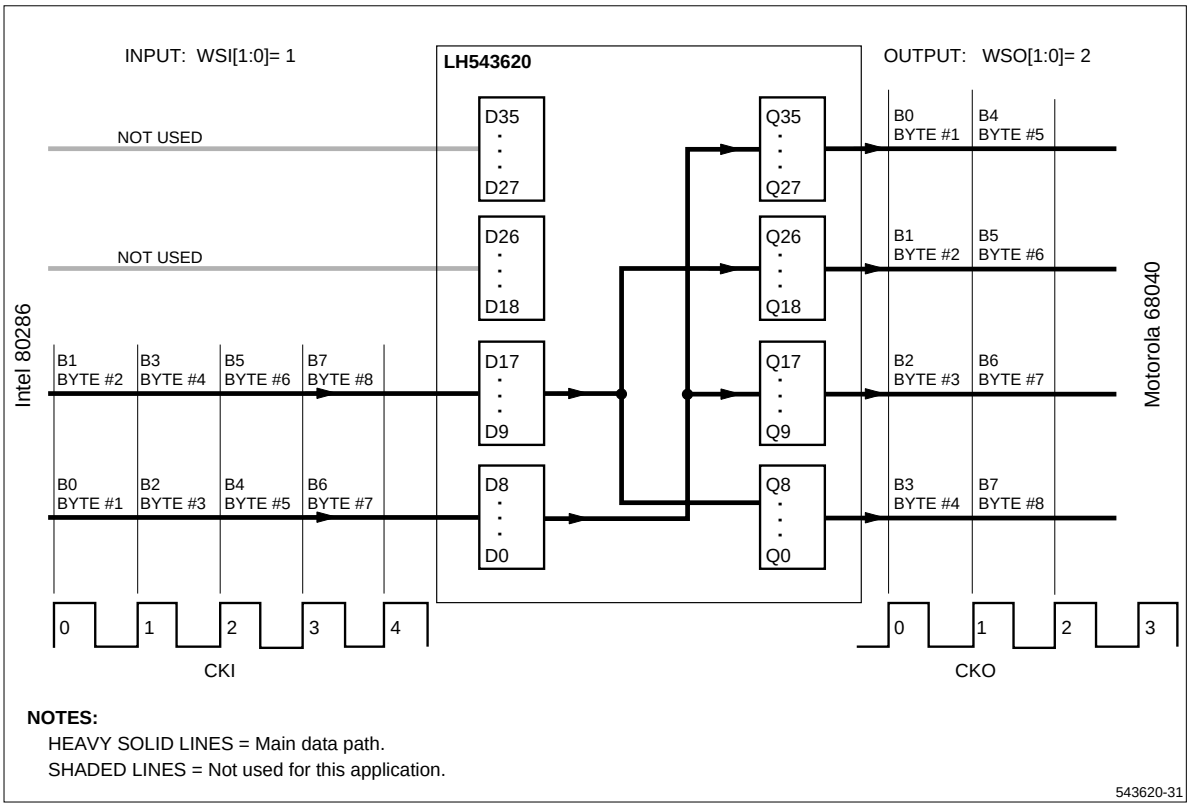


Figure 6. Example of 18-to-36 Bus Defunneling With Byte Order Reversal

Status Flags

There are five status flags:

$\overline{FF}$ Full Flag

$\overline{AF}$ Almost-Full Flag

$\overline{HF}$ Half-Full Flag

$\overline{AE}$ Almost-Empty Flag

$\overline{EF}$ Empty Flag

The functionality and the synchronization of the status flags are detailed in the *Pins Descriptions (Functional)* section. All status flags are generated for 36-bit word widths, not according to selected input or output port widths.

Retransmit Mechanism

With standard FIFO operations, every data word can be read out of the FIFO once. The Retransmit mechanism allows reading the data more than once by providing flexible control of the Read Pointer.

Associated with the Retransmit mechanism are three control lines: RTMD[1:0], $\overline{RT}$, and two Resource registers: RBASE and ROFFSET.

RTMD[1:0] sets the mode of operation. See Table 6.

$\overline{RT}$ enables the operation synchronous to CKO.

Retransmit allows three modes of operation:

Mark: RTMD[1:0] = 3 and $\overline{RT}$ is asserted. The value of the Read Pointer is saved into the RBASE register.

Retransmit: RTMD[1:0] = 1 and $\overline{RT}$ is asserted. The Read Pointer is loaded by the value of RBASE plus the value of ROFFSET.

Retransmit and Mark: RTMD[1:0] = 2 and $\overline{RT}$ is asserted: The Read Pointer is loaded by the value of RBASE plus the value of ROFFSET. Then the value of the Read Pointer is saved into the RBASE register.

The timing of the retransmit is illustrated in Figures 26 and 27.

When $\overline{RT}$ is asserted and RTMD[1:0] is set to 1 or 2, the flags change their value to indicate a 'Retransmit state', i.e., $\overline{EF}$, $\overline{AE}$, $\overline{FF}$ deasserted; $\overline{AF}$, $\overline{HF}$ asserted. Three enable-read cycles are required to read the new data word. The flags reflect the new status. The retransmit is acknowledged even when the output is disabled (ENO = LOW), but enable-read cycles are needed to fill the pipeline with new information before reading the new data.

NOTES

1. The Retransmit mechanism can be used independently and parallel to the write operation.
2. RTMD[1:0] must be selected two cycles prior to **RT** being asserted and remain stable during **RT** low.
3. At least two words need to be in the FIFO memory array prior to performing a retransmit.
4. When using normal read and write operations, the $\overline{FF}$ inhibits writing when the FIFO is full and the $\overline{EF}$ inhibits reading when the FIFO is empty. This behavior provides a protection from wraparound situations (i.e., the Read pointer is ahead of the Write Pointer). This protection is NOT provided when using retransmit. The user should be careful not to write more than 1024 words from the marked point.
5. When the retransmit mechanism is not used, the recommended connection is:
   RTMD[1:0] = 3
   $\overline{RT}$ = HIGH

The Retransmit mechanism can be useful in many applications. For example:

1. Computer-communications applications.

   When the receiver reads a block of data and finds no errors in the data block, it can mark the beginning of the new message by setting the FIFO in MARK mode RTMD[1:0] = 3 and assert the $\overline{RT}$ signal for one clock cycle.

   If the receiver finds an error in the data block, it can read the last message again by setting the FIFO in Retransmit mode RTMD[1:0] = 1 and asserting the $\overline{RT}$ signal for one cycle.

2. Overlap addressing for DSP applications.

   A typical DSP consists of A/D-FIFO-DSP. In many applications, the DSP needs to read a block of data where each block overlaps the previous block (like the overlap-and-save method for filtering.) The overlap addressing can be implemented by using the LH543620 with no additional hardware as follows:

   The FIFO is set to retransmit and mark mode: RTMD[1:0] = 2, the $\overline{AF}$ offset register is programmed to N = Block Size, and the ROFFSET register is programmed to (N – Overlap). The data is loaded into the FIFO each time CKin is triggered.

   The DSP can sense the $\overline{AF}$ flag of the FIFO. Whenever this flag is being asserted, a new block of data is available in the FIFO. The DSP then reads a block of data, and then asserts the FIFO's $\overline{RT}$ signal, which causes the RP and RBASE register to be set at the beginning of the new block.

Parity Checking

The Parity checking mechanism is always active. Parity checking is done separately for each of the 9-bit bytes of the 36-bit word read from the memory array. Toggling Bit 0 of the control register selects odd or even parity. When a parity error is detected in one or more bytes, the signal $\overline{PF}$ is asserted and the result of the individual parity checks are written to the parity register. See Example 3.

To avoid a possible invalid $\overline{PF}$ signal, ENO_1 and ENO_2 should not be deasserted during the CLKO low time.

The parity register is frozen until read. When read, the parity register is released and ready to store the next parity error data.

Parity Generation

After Reset, parity generation is not active. Parity generation is active only when Bit 1 of the control register is HIGH. The parity mechanism, when enabled, creates a parity bit for each of the bytes of the input word. The parity bit for each byte is created based on its 8 least significant bits of each 9-bit byte of the input-data word and on Bit 0 of the control register (it specifies odd or even parity). The result of the parity generation is written back to the MSB of the data byte. See Example 4.

PROGRAMMABLE RESOURCE REGISTERS

The LH543620 has six programmable resource registers. The resource registers may be loaded from either the Input Port or the Output Port. They can be read from the Output Port. The selection and loading or reading of the resource registers is controlled by ADI, ADO and CAPR. See Tables 1 and 4 and Figure 4.

The resource registers are:

Control (Default = 1).

$\overline{AE}$ Offset – Offset value of the $\overline{AE}$ flag (Default = 8).

$\overline{AF}$ Offset – Offset value of the $\overline{AF}$ flag (Default = 8).

$\overline{RT}$ Offset – Offset value of the Retransmit mechanism (Default = 0).

$\overline{RT}$ Base – Base register of the Retransmit mechanism (Default = 0).

Parity

EXAMPLE 3 **PARITY CHECK**

	Q35			Q0
Output word:	100111100	000111100	100111000	000111000
Odd parity:	Parity Register = 0110; PF-Asserted Low			
Even parity:	Parity Register = 1001; PF-Asserted Low			

EXAMPLE 4 **PARITY GENERATION**

	D35			D0
Input word:	**1**00111100	**0**00111100	**1**00111000	**0**00111000
Output, odd parity:	**1**00111100	**1**00111100	**0**00111000	**0**00111000
Output, even parity:	**0**00111100	**0**00111100	**1**00111000	**1**00111000

Control Register (See Figure 7)

After reset, the control register's value is 1. This sets the following conditions:

Odd parity

Disabling parity generation (parity check is active).

$\overline{AF}$, $\overline{HF}$, $\overline{AE}$ flags are asynchronous.

$\overline{OE}$ signal does not control the Read pointer.

Read/Write Resource Register Mode

It is possible to write to the resource registers from either the Input Port or the Output Port. Reading from the resource register is possible only from the Output Port. The source port for the write operation is determined by the control signal CAPR.

Input Port:

Data from the Input Port is written to a resource register when:

the value of the input-address field, ADI, selects the register (see Table 1)

CAPR is LOW

The operation is enabled by ADI[2:0] and synchronized to CKI.

Output Port:

Data from the Output Port is written to a resource register when:

the value of the output-address field, ADO, selects the register (see Table 4)

CAPR is HIGH

$\overline{OE}$ is HIGH

NOTE: ADI[2:0] should remain stable whenever data is coming in from the output port.

Data is read from a resource register to the Output Port when:

the value of the output-address field, ADO, selects the register (see Table 4)

$\overline{OE}$ is LOW

Both operations are enabled by ADO[2:0] and are synchronous to CKO.

MAILBOX

The mailbox mechanism includes:

One 36-bit data register.

Two status flags:
– $\overline{MFF}$ Mailbox Full Flag
– $\overline{MEF}$ Mailbox Empty Flag

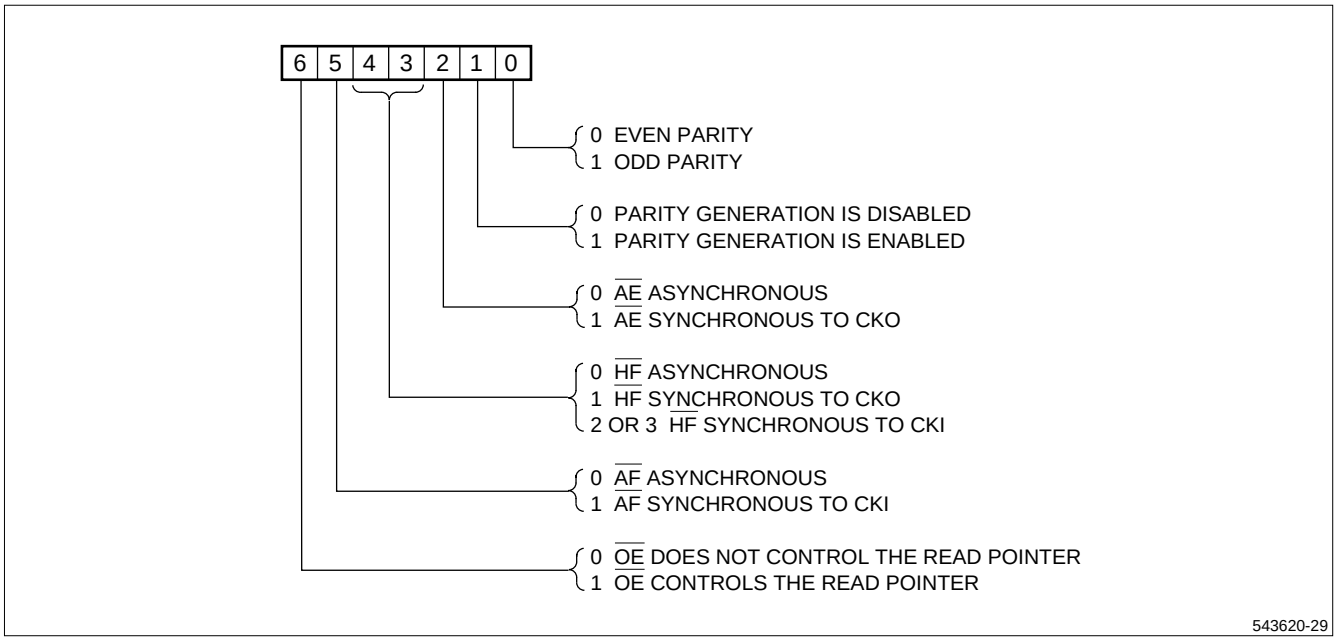


Figure 7. LH543620 Control Register

Writing to the Mailbox is enabled from the Input Port when the Input Port address field ADI[2:0] = 6. The write operation is synchronous to the rising edge of CKI.

When writing to the Mailbox, the status flags are changed as follows:

$\overline{MEF}$ is deasserted HIGH on the rising edge of CKO.

$\overline{MFF}$ is asserted LOW on the rising edge of CKI.

A Mailbox read is enabled from the Output Port, when the Output Port address field ADO[2:0] = 6. The Read operation is synchronized to CKO.

When reading the Mailbox, the status flags are changed as follows:

$\overline{MEF}$ is asserted LOW on the rising edge of CKO.

$\overline{MFF}$ is deasserted HIGH on the rising edge of CKI.

After reset the Mailbox is empty (i.e., $\overline{MFF}$ = HIGH, $\overline{MEF}$ = LOW).

When using Mailbox, the transmitter side can transfer a message to the receiver side without interrupting the data in the FIFO memory array.

DATA BYPASS MODE

Data Bypass mode is selected when $\overline{BYE}$ = LOW. In this mode, data may be transferred asynchronously from the Input Port to the Output Port. The device may be placed in Data Bypass mode without voiding the contents of the FIFO memory array, the Mailbox Register, or the Resource Register. However, if the input is enabled ($ENI_{1,2}$ = HIGH) then the input data D is also written to the FIFO memory array on the rising edge of CKI. If the Output is enabled, ($ENO_{1,2}$ = HIGH) then the input data D is transferred to the output buffer, and the Read Pointer is incremented by CKO. The control signal $\overline{OE}$ is functioning when $\overline{BYE}$ is asserted.

The recommended control setting for bypass is:

ENI = LOW, ENO = LOW, ADI[2:0] = 7,
ADO[2:0] = 7, $\overline{OE}$ = LOW, $\overline{BYE}$ = LOW

OPERATIONAL MODES AND CONFIGURATIONS

Interlocked Width Expansion (Figure 8A)

Two LH543620s may be configured to expand the width to 72 bits. This is accomplished by:

Cross-connecting the $\overline{FF}$ output of each FIFO to ENI_1 (or ENI_2) input of the other FIFO.

Cross-connecting the $\overline{EF}$ output of each FIFO to ENO_1 (or ENO_2) input of the other FIFO.

The composite status flags are the OR function of the individual flags.

Pipeline Cascading Mode and 'Two-Dimension' Pipeline Cascading Mode (Figure 8B and 8C)

Depth cascading is accomplished by:

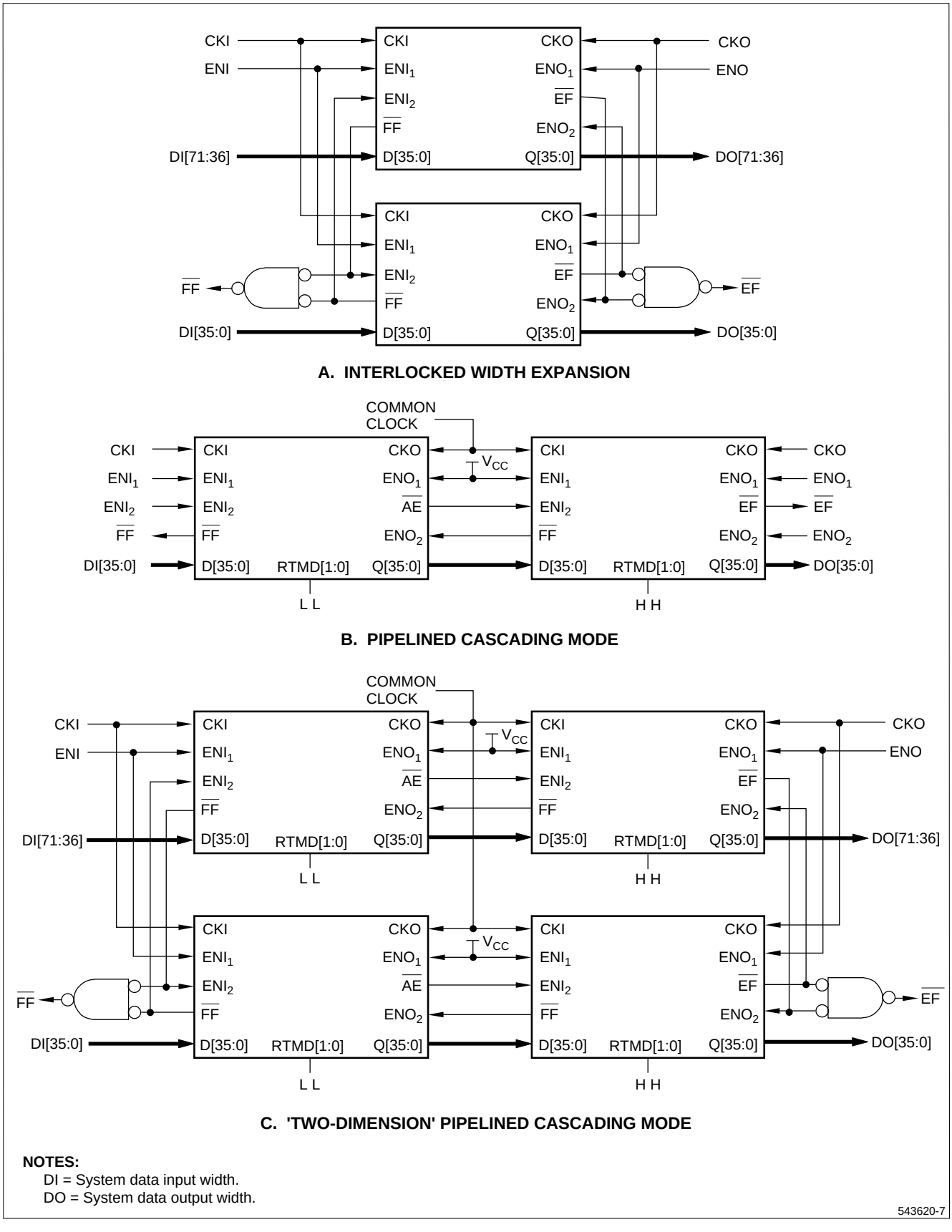
Setting the upper FIFO into cascade mode:
RTMD[1:0] = 0

Connecting the same free-running clock to CKO of the upper FIFO and to CKI input of the lower FIFO.

Connecting the $\overline{AE}$ output of the upper FIFO to ENI_1 input (or ENI_2) of the lower FIFO.

Connecting the $\overline{FF}$ output of the lower FIFO to ENO_1 input (or ENO_2) of the upper FIFO.

NOTE: RTMD[1:0] should remain stable during cascade mode operation (i.e., remain low).

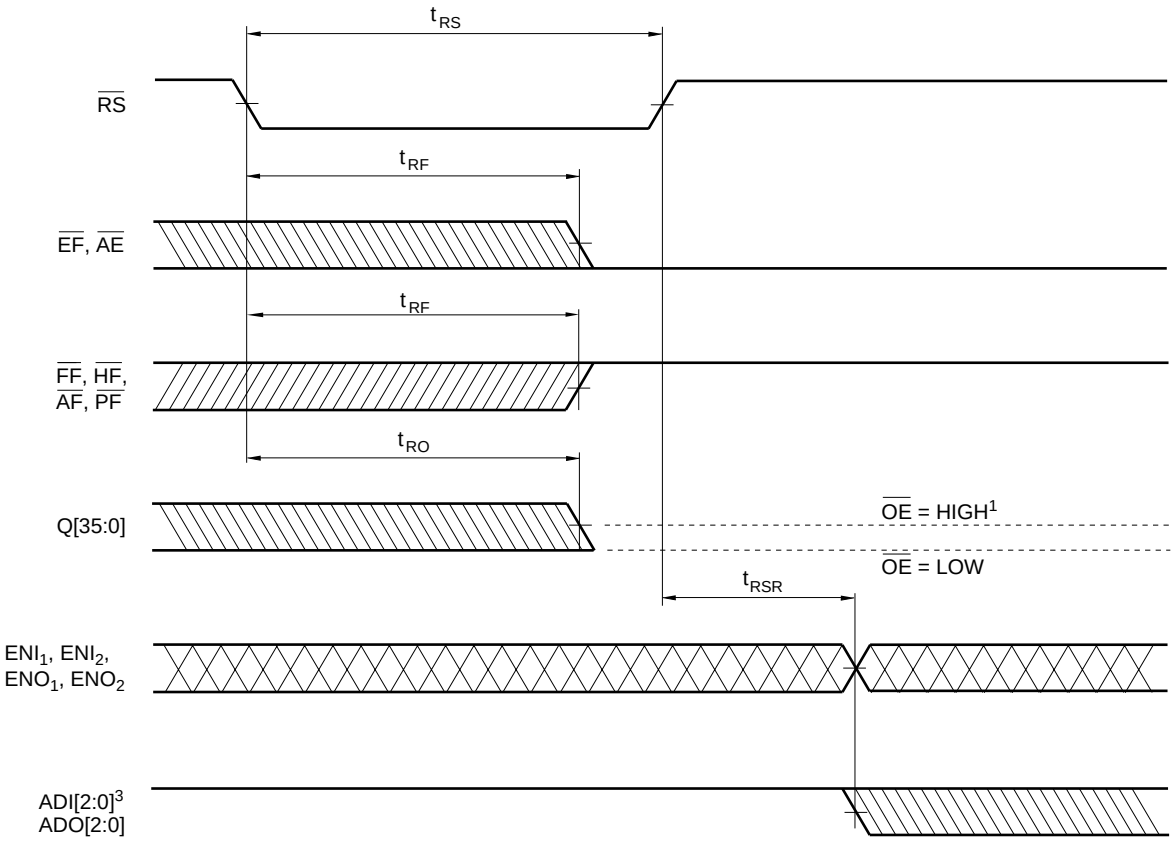


NOTES:
DI = System data input width.
DO = System data output width.

543620-7

Figure 8. LH543620 Width and Depth Expansion Scheme

TIMING DIAGRAMS

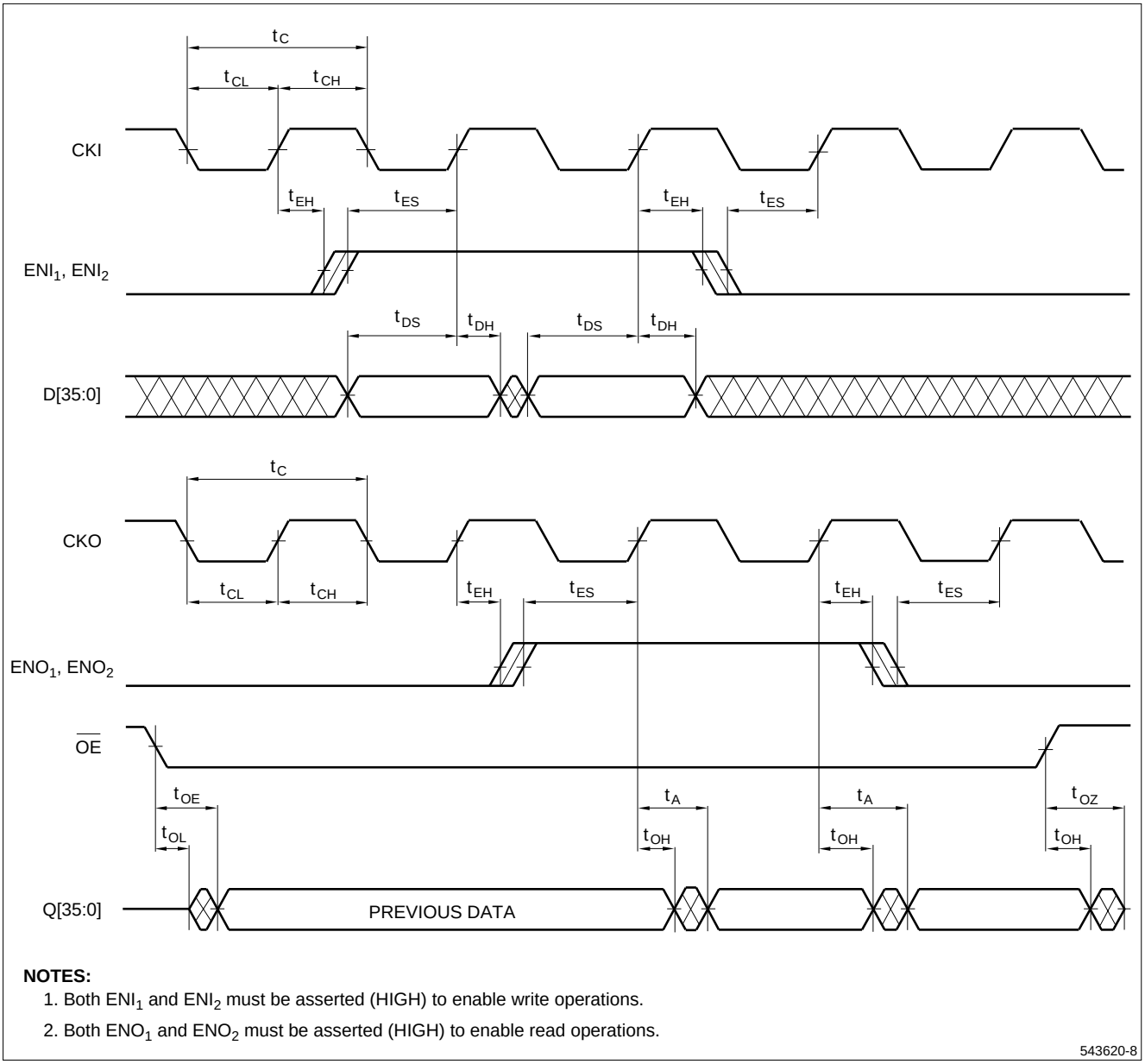


NOTES:

1. After reset, the outputs will be LOW if $\overline{OE}$ = LOW, and in a high-impedance state if $\overline{OE}$ = HIGH.
2. The clocks (CKI, CKO) may be free-running during a reset operation.
3. If CAPR = L, then ADO = XXX and ADI must be = H,H,H for proper reset.
   If CAPR = H, then ADI = XXX and ADO must be = H,H,H for proper reset.

543620-15

Figure 9. Reset Timing



NOTES:

1. Both ENI_1 and ENI_2 must be asserted (HIGH) to enable write operations.
2. Both ENO_1 and ENO_2 must be asserted (HIGH) to enable read operations.

543620-8

Figure 10. Write and Read Operation

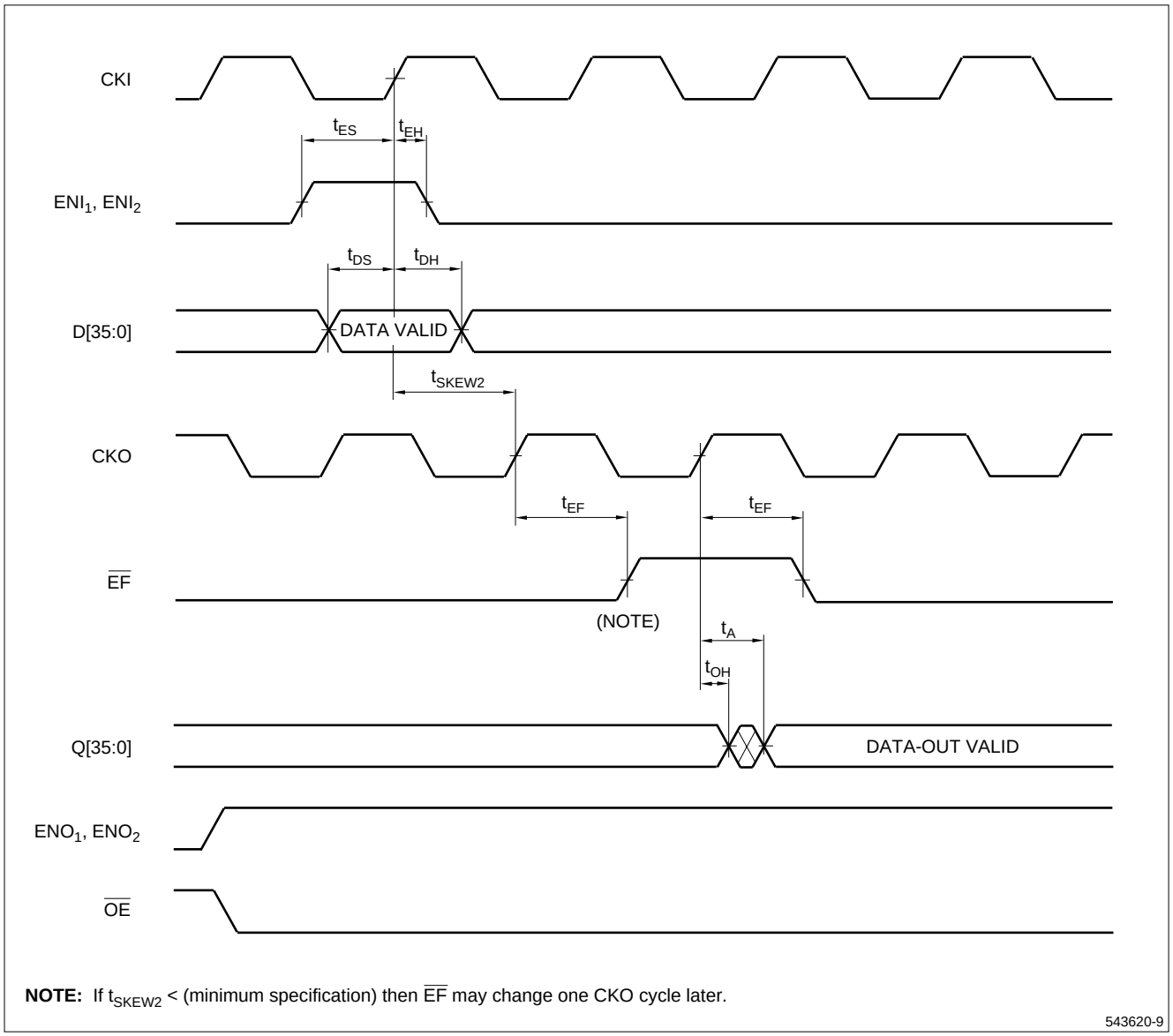


Figure 11. Empty Flag Timing

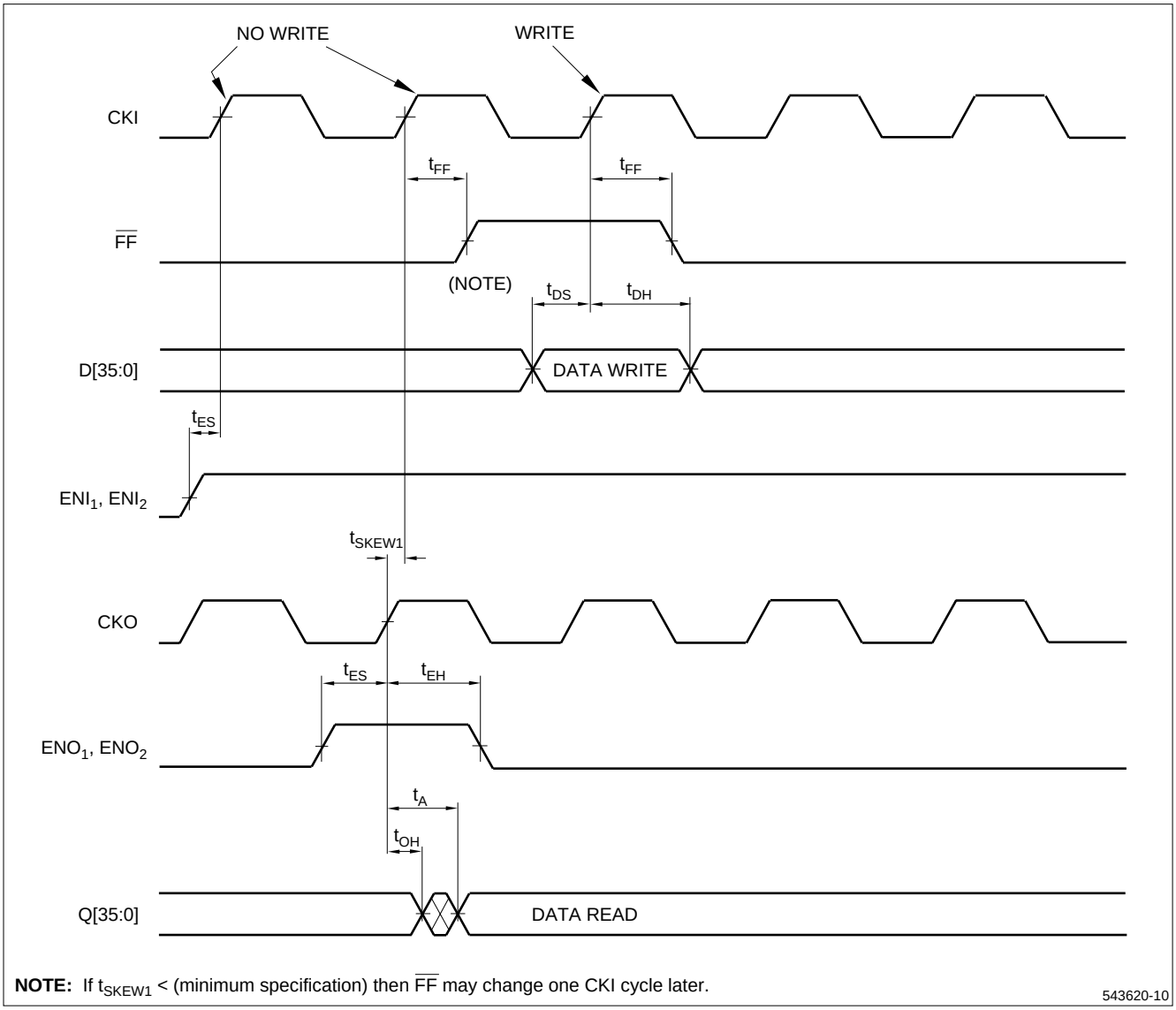
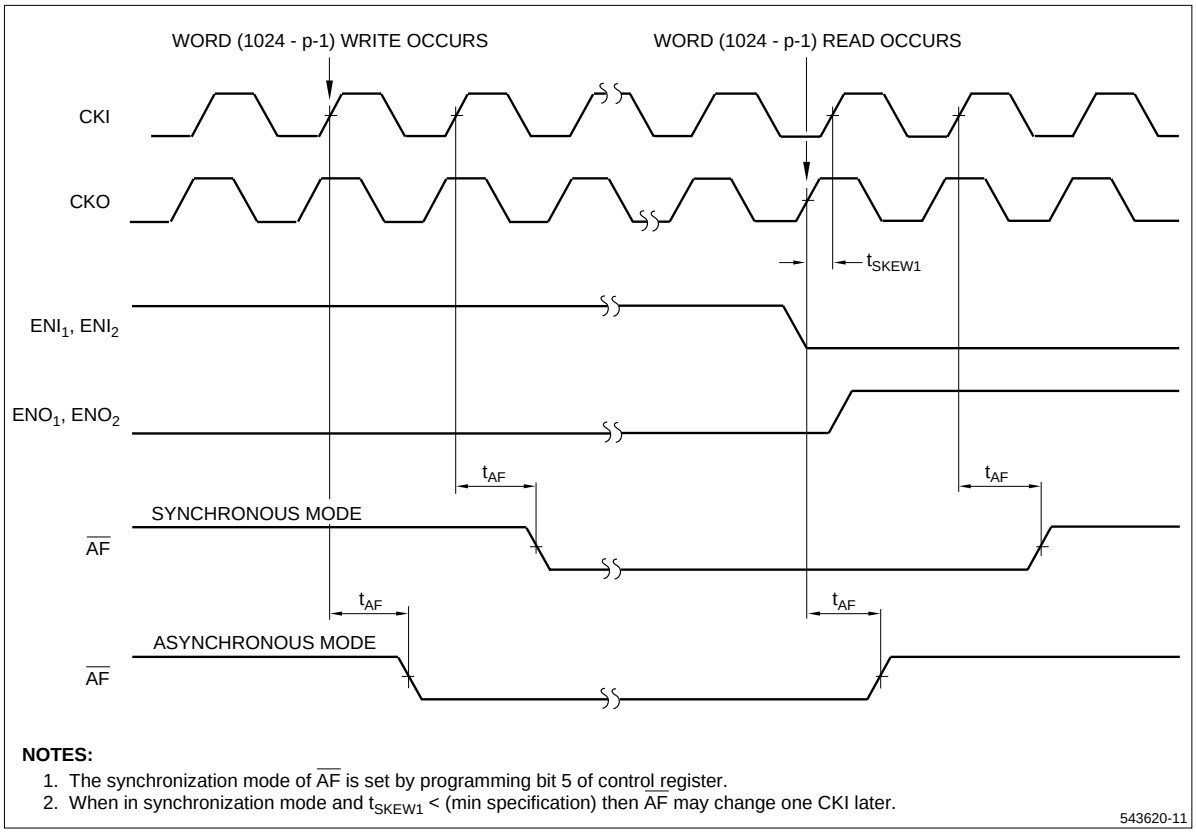


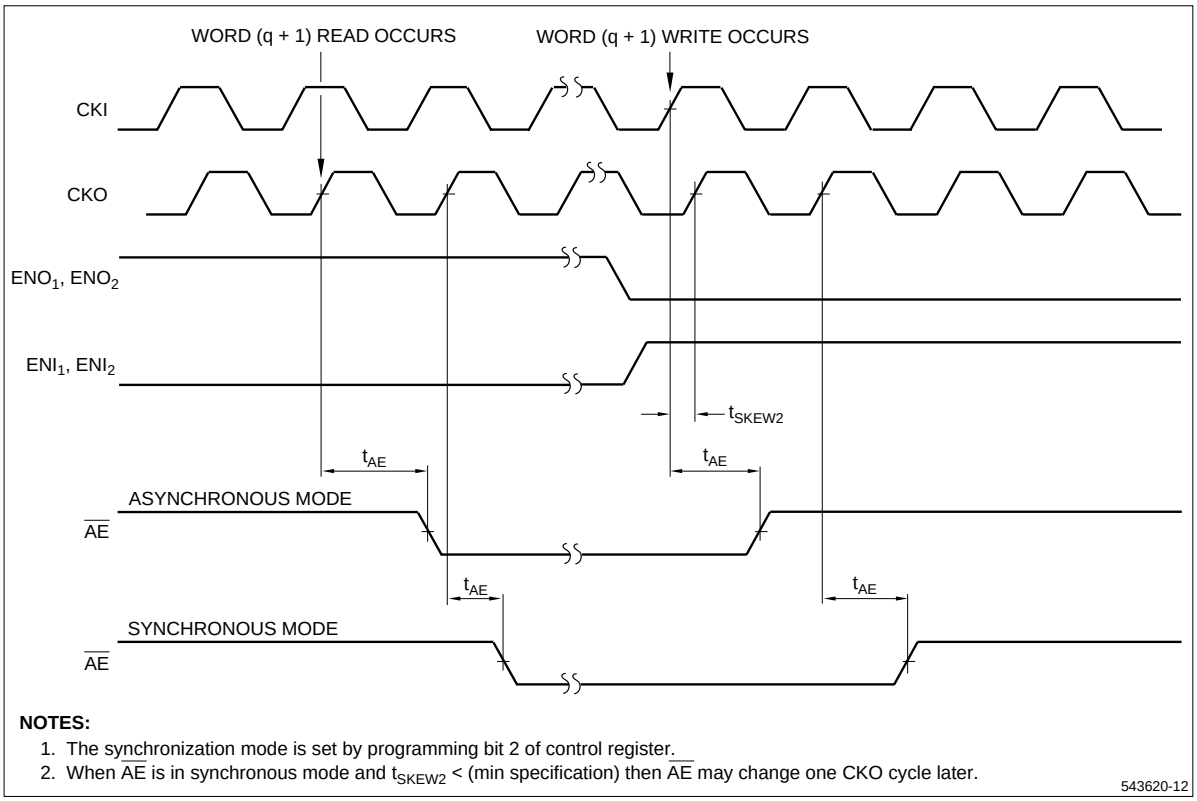
Figure 12. Full Flag Timing



NOTES:
1. The synchronization mode of $\overline{AF}$ is set by programming bit 5 of control register.
2. When in synchronization mode and t_{SKEW1} < (min specification) then $\overline{AF}$ may change one CKI later.

543620-11

Figure 13. Almost-Full Flag - Synchronous and Asynchronous Modes



NOTES:
1. The synchronization mode is set by programming bit 2 of control register.
2. When $\overline{AE}$ is in synchronous mode and t_{SKEW2} < (min specification) then $\overline{AE}$ may change one CKO cycle later.

543620-12

Figure 14. Almost-Empty Flag - Synchronous and Asynchronous Modes

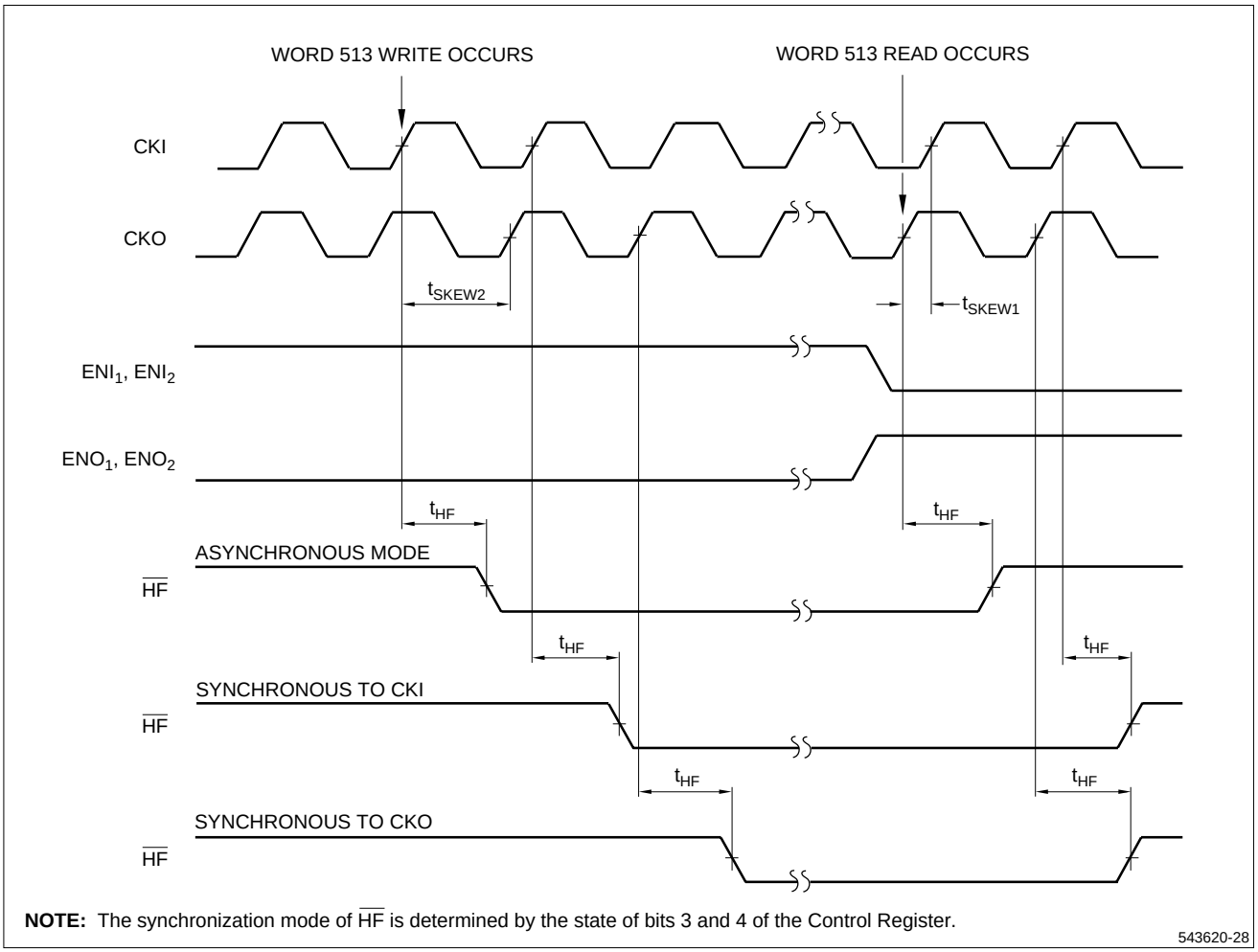
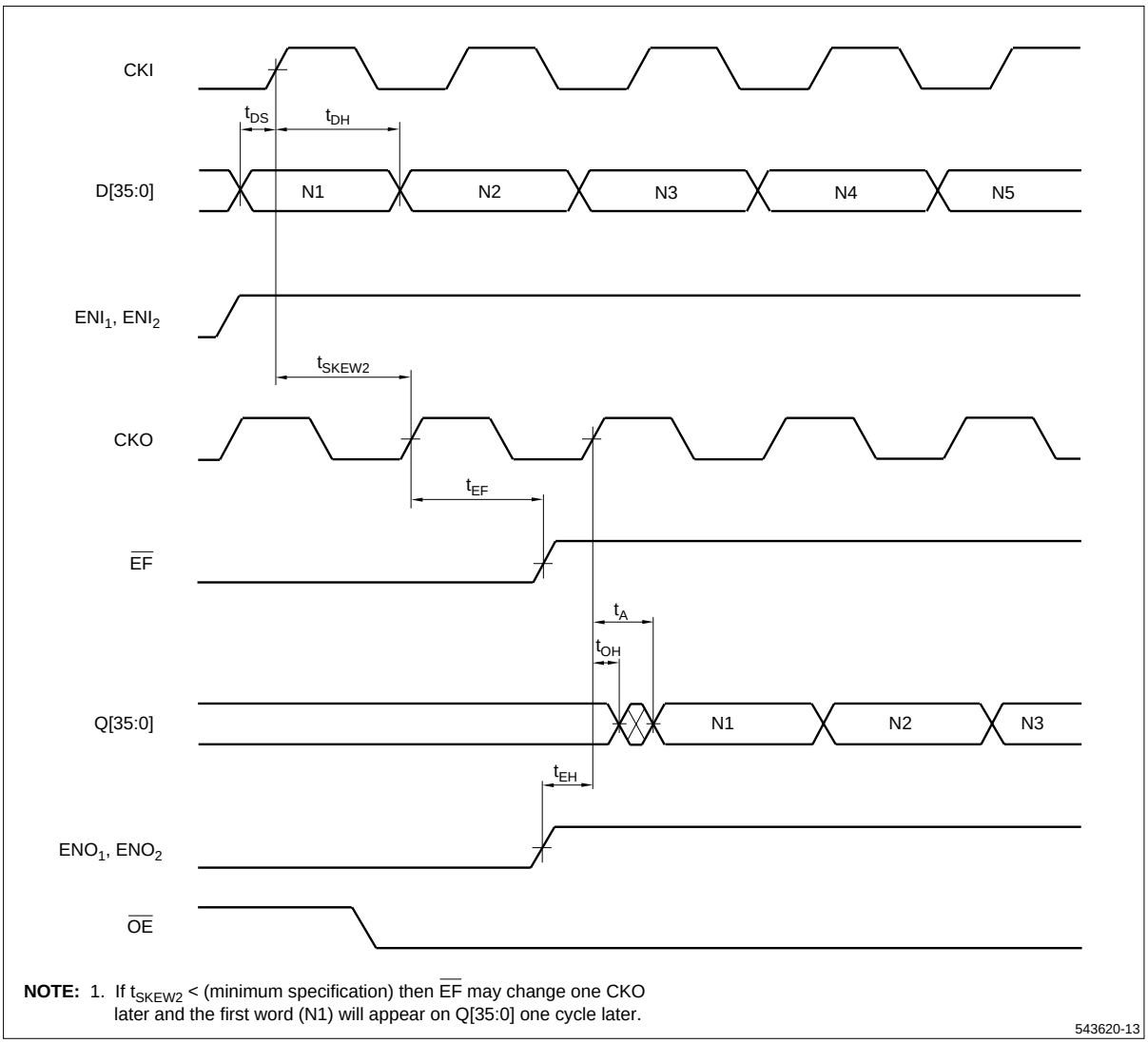


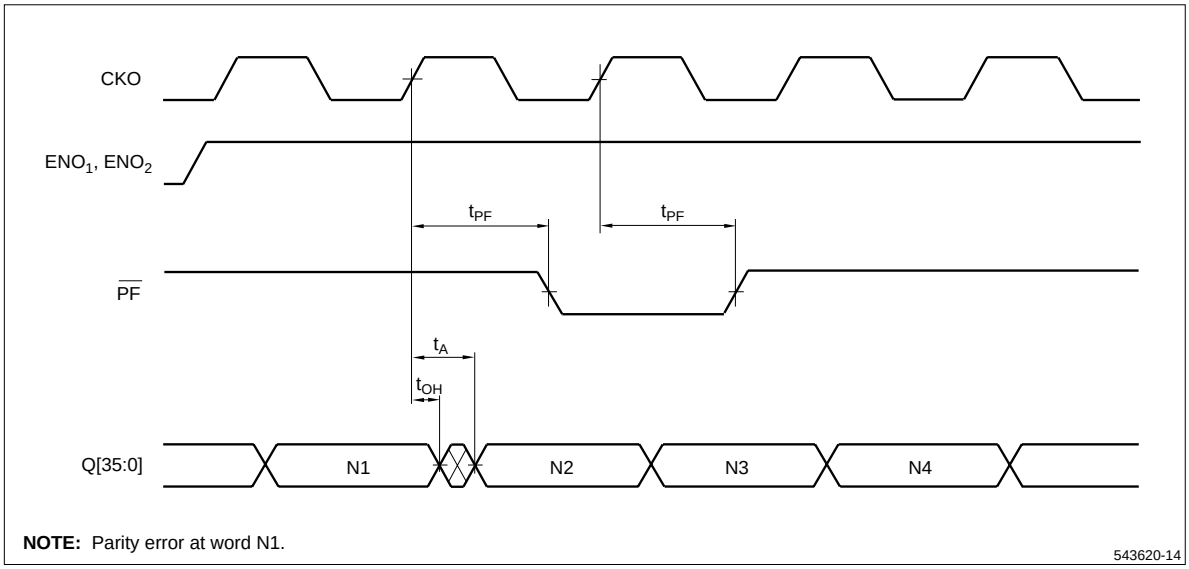
Figure 15. Half-Full Flag - Synchronous and Asynchronous Modes



NOTE: 1. If t_{SKEW2} < (minimum specification) then $\overline{EF}$ may change one CKO later and the first word (N1) will appear on Q[35:0] one cycle later.

543620-13

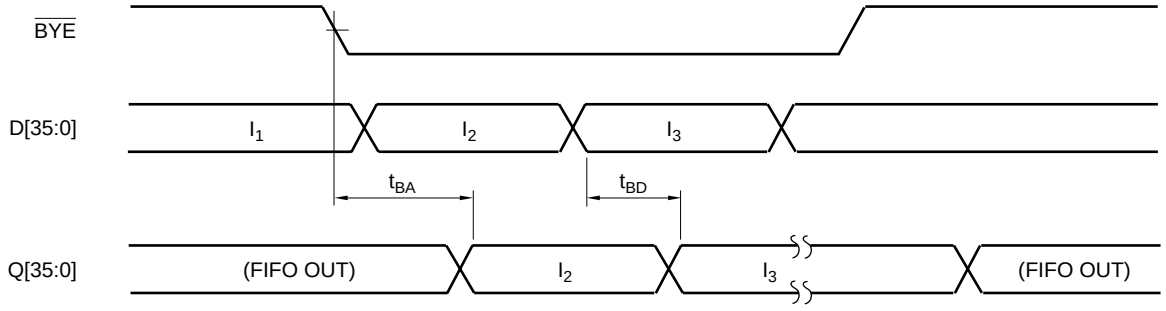
Figure 16. First Word Latency



NOTE: Parity error at word N1.

543620-14

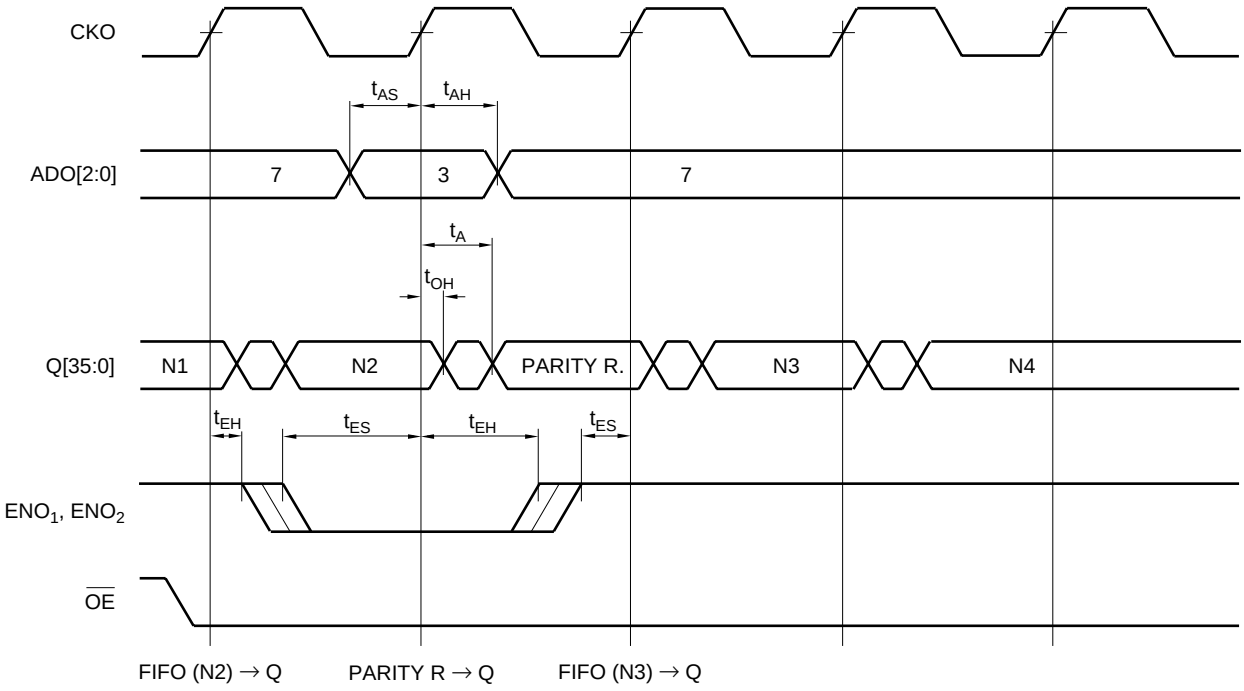
Figure 17. Parity Flag



NOTES:
1. If ENI is enabled during $\overline{BYE}$ = LOW, the bypass data will be written into the FIFO.
2. If ENO is enabled the data at the Q Port is the bypass data. The RP will be updated according to CKO.

543620-16

Figure 18. Bypass



NOTE: N1, N2, N3, N4 are data from the FIFO and PARITY R. is the Parity Register value.

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Figure 19. Read Resource Register

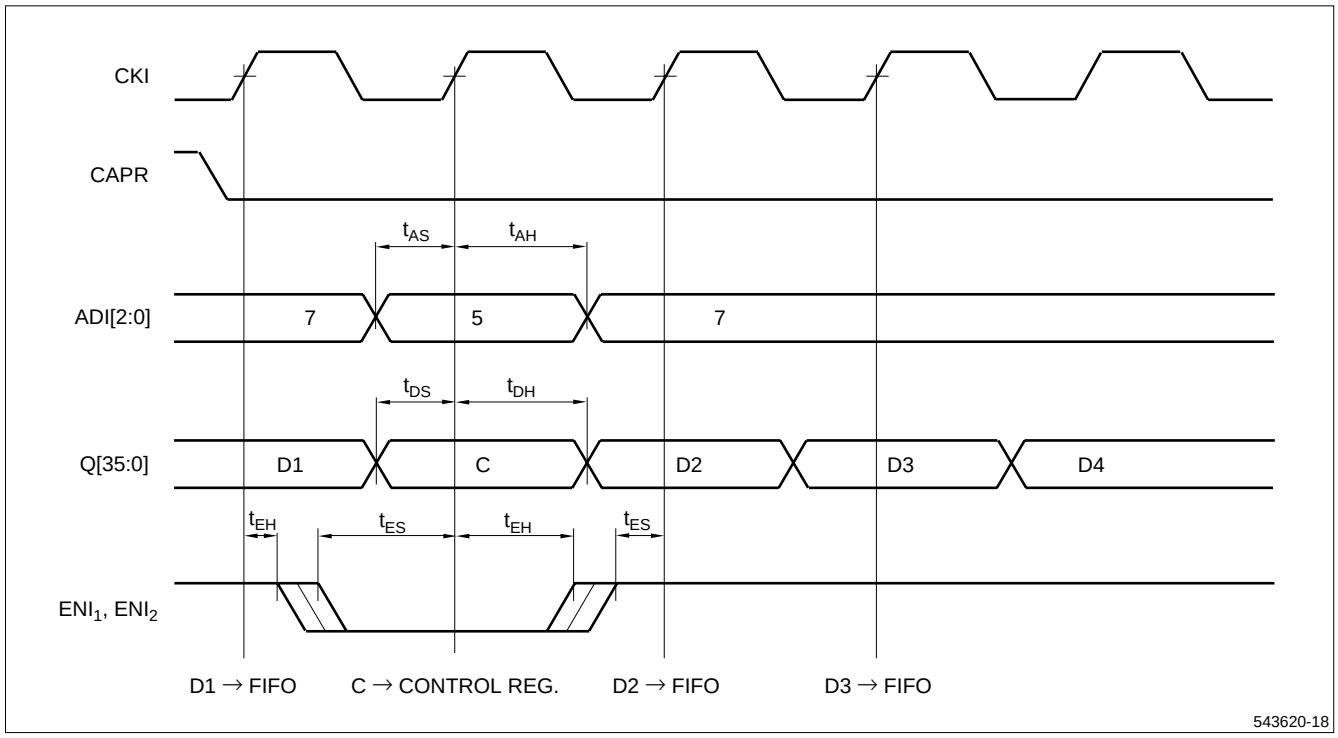


Figure 20. Write Resource Register From the Input Port

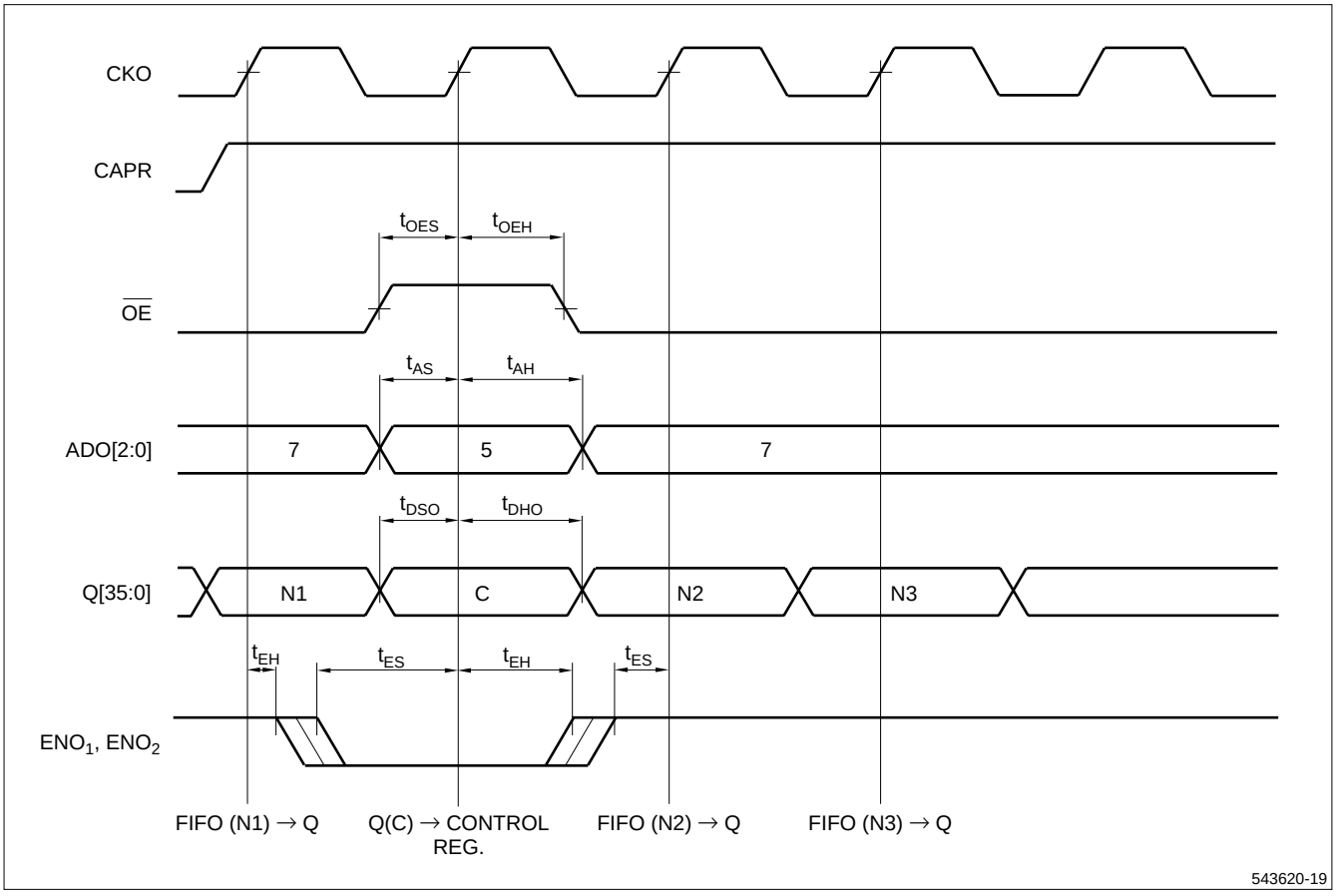


Figure 21. Write Resource Register From Output Port

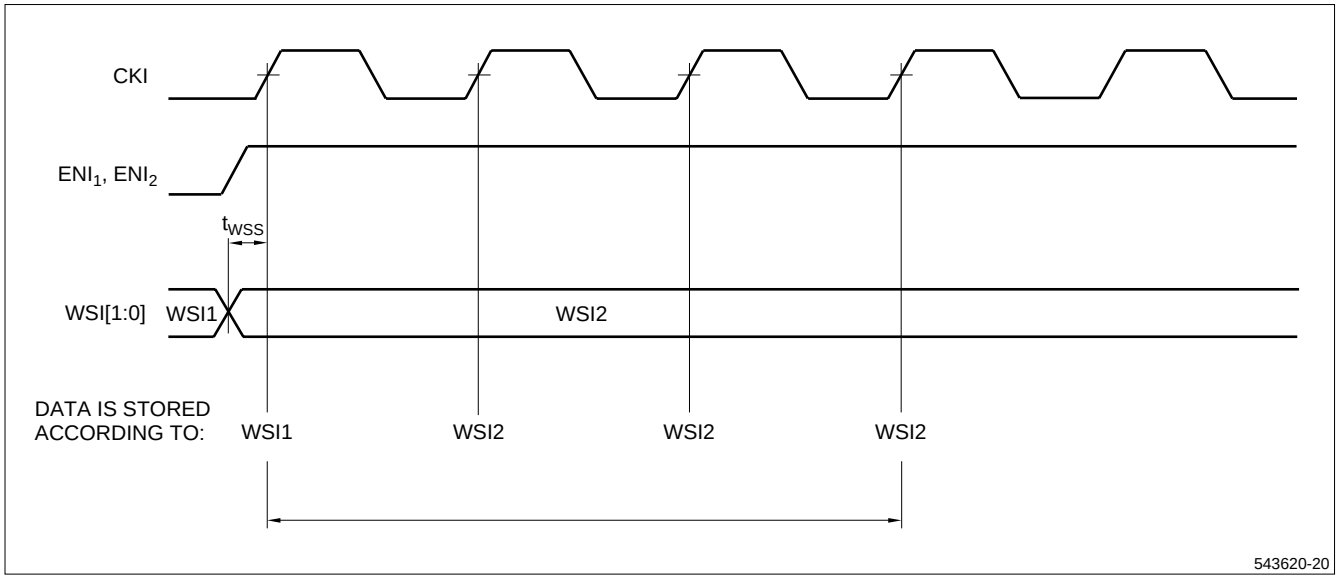


Figure 22. WSI[1:0] Timing

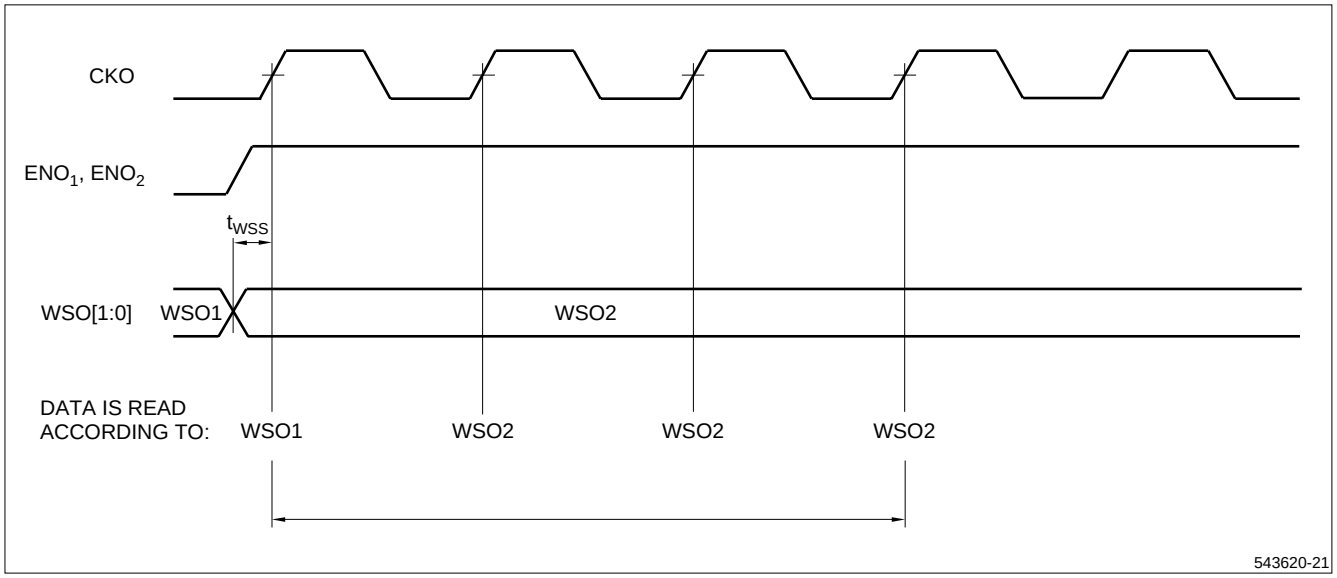
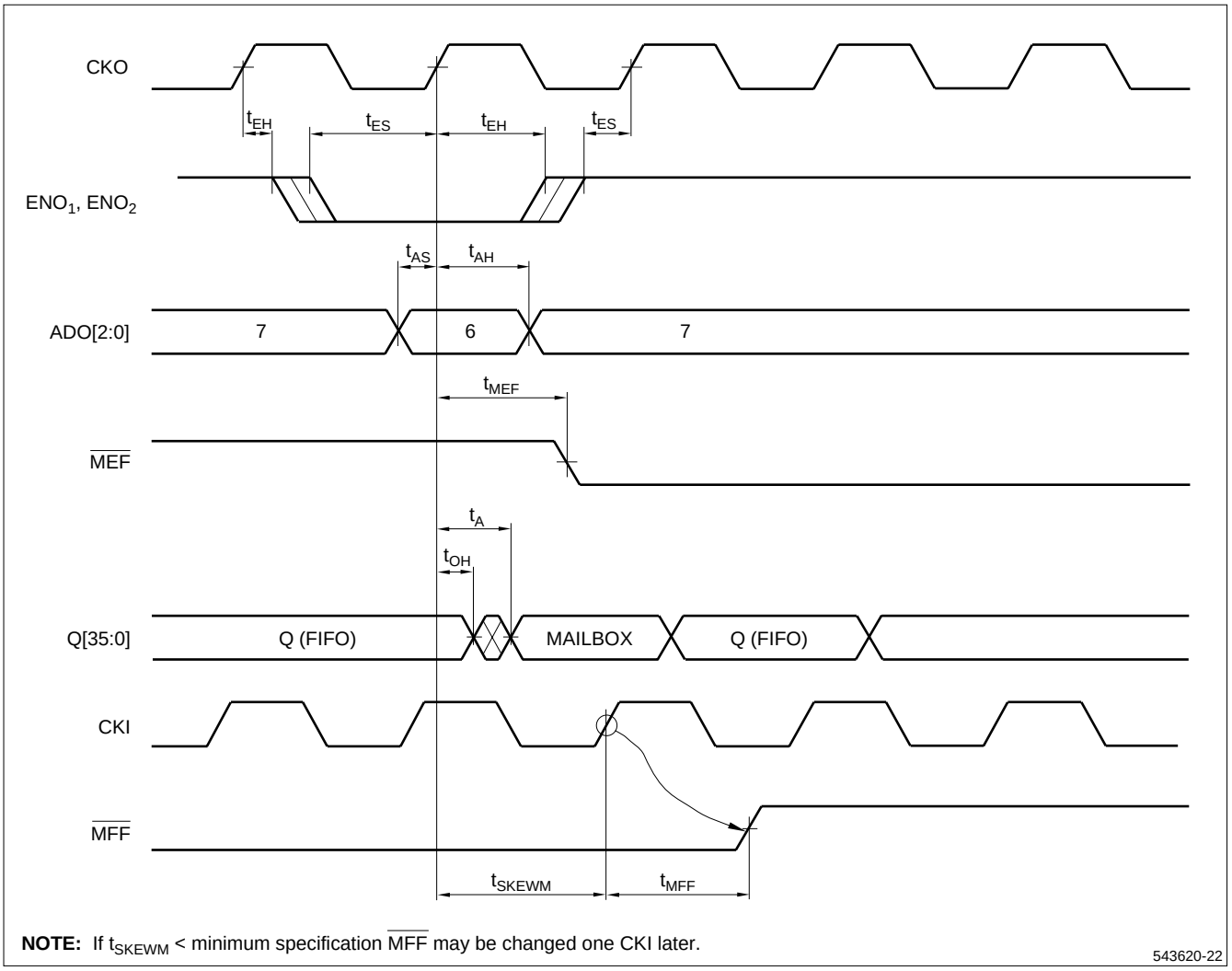


Figure 23. WSO[1:0] Timing



NOTE: If t_{SKEWM} < minimum specification $\overline{MFF}$ may be changed one CKI later.

543620-22

Figure 24. Mailbox Read

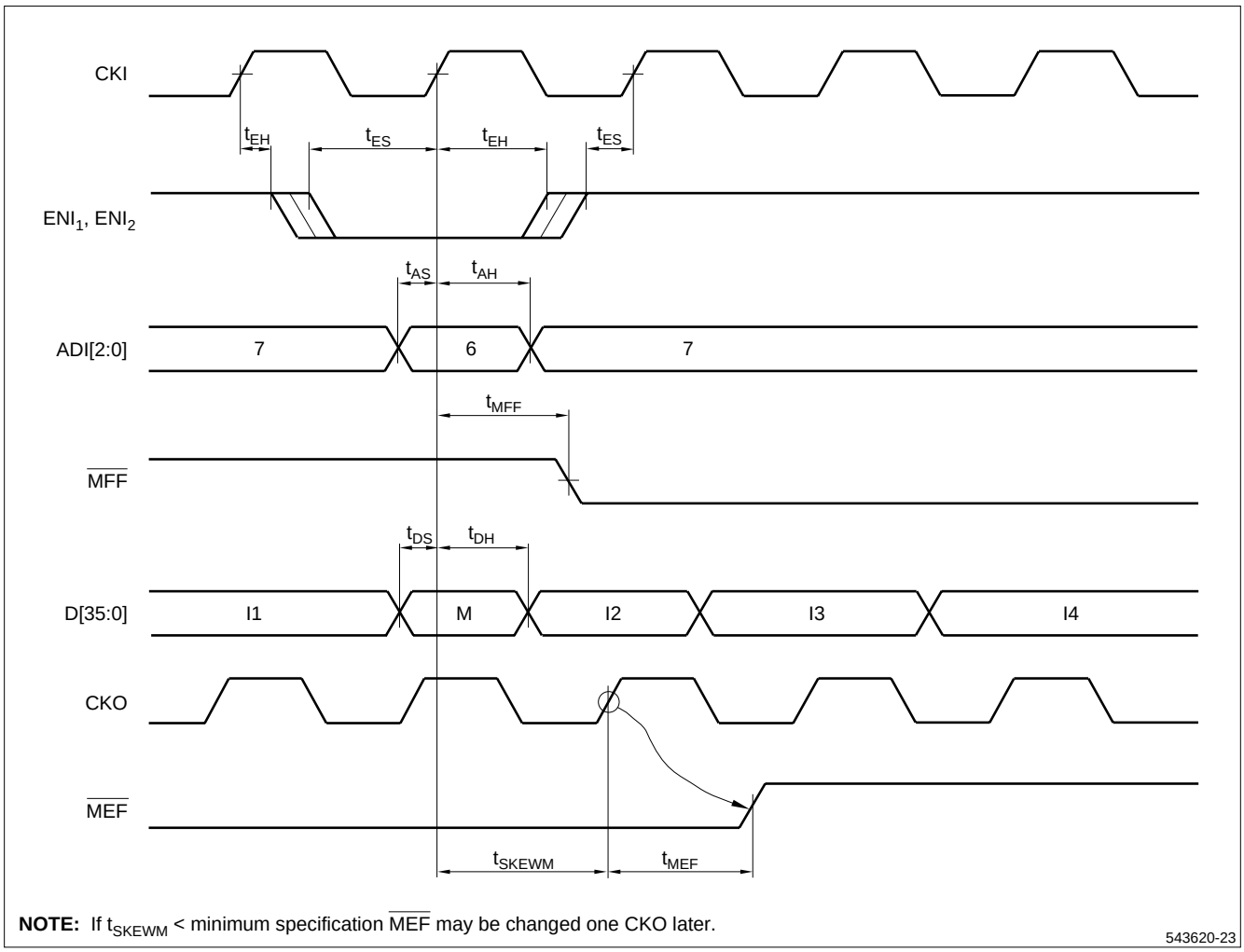
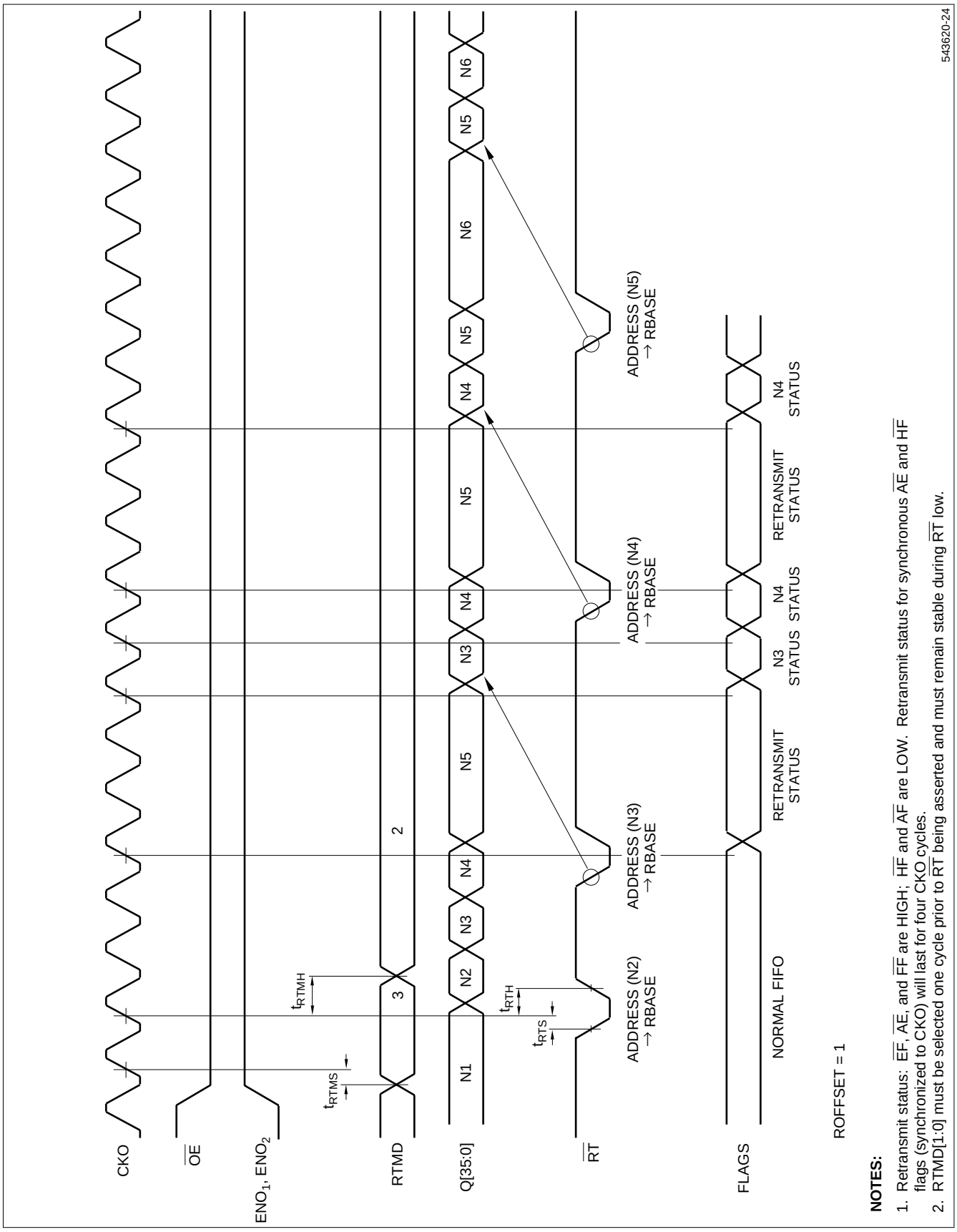


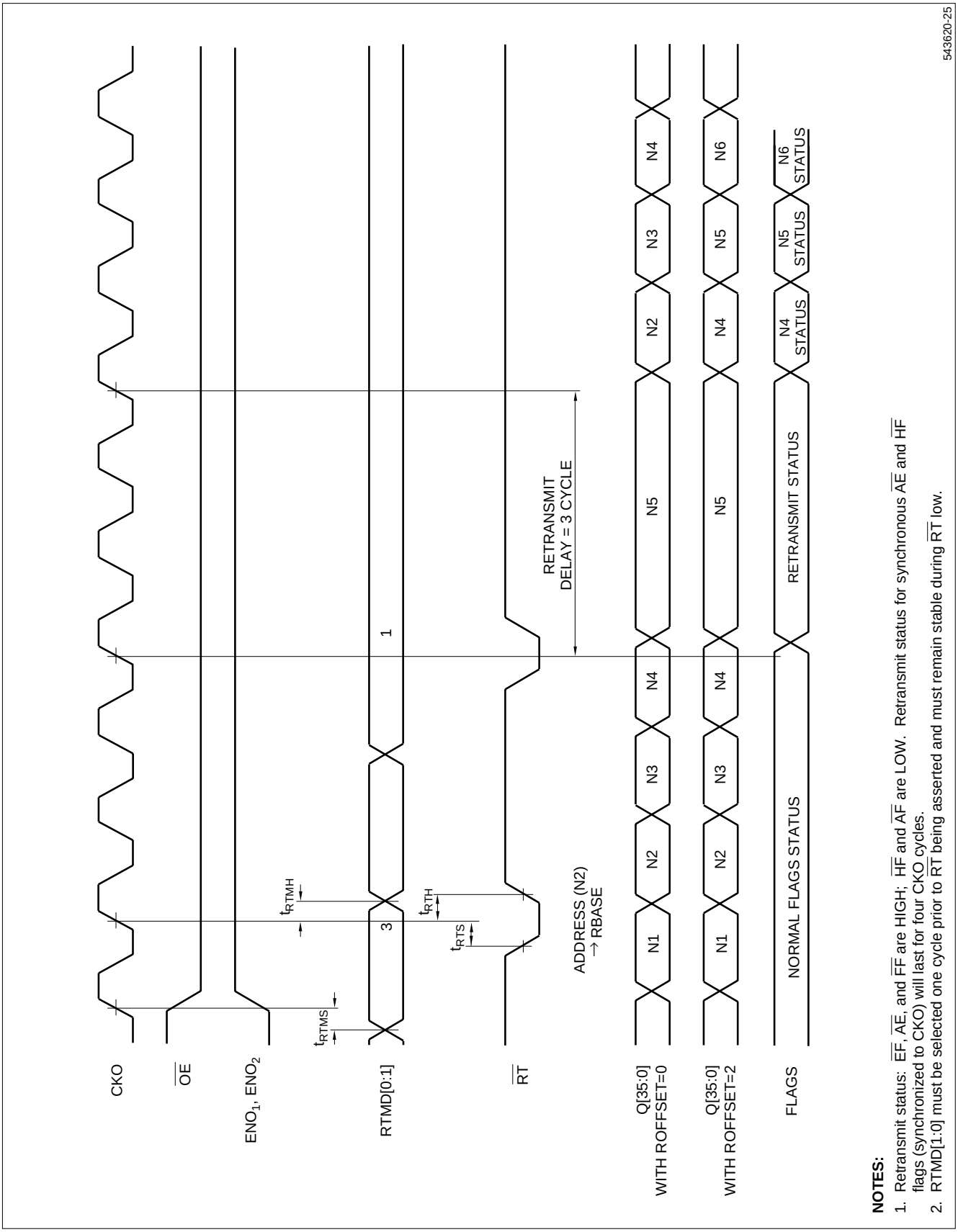
Figure 25. Mailbox Write



NOTES:

1. Retransmit status: $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ are HIGH; $\overline{HF}$ and $\overline{AF}$ are LOW. Retransmit status for synchronous $\overline{AE}$ and $\overline{HF}$ flags (synchronized to CKO) will last for four CKO cycles.
2. RTMD[1:0] must be selected one cycle prior to $\overline{RT}$ being asserted and must remain stable during $\overline{RT}$ low.

Figure 26. Retransmit Using Retransmit and Mark Mode



NOTES:

1. Retransmit status: $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ are HIGH; $\overline{HF}$ and $\overline{AF}$ are LOW. Retransmit status for synchronous $\overline{AE}$ and $\overline{HF}$ flags (synchronized to CKO) will last for four CKO cycles.
2. RTMD[1:0] must be selected one cycle prior to $\overline{RT}$ being asserted and must remain stable during $\overline{RT}$ low.

Figure 27. Retransmit Using Mark Mode and Retransmit Mode

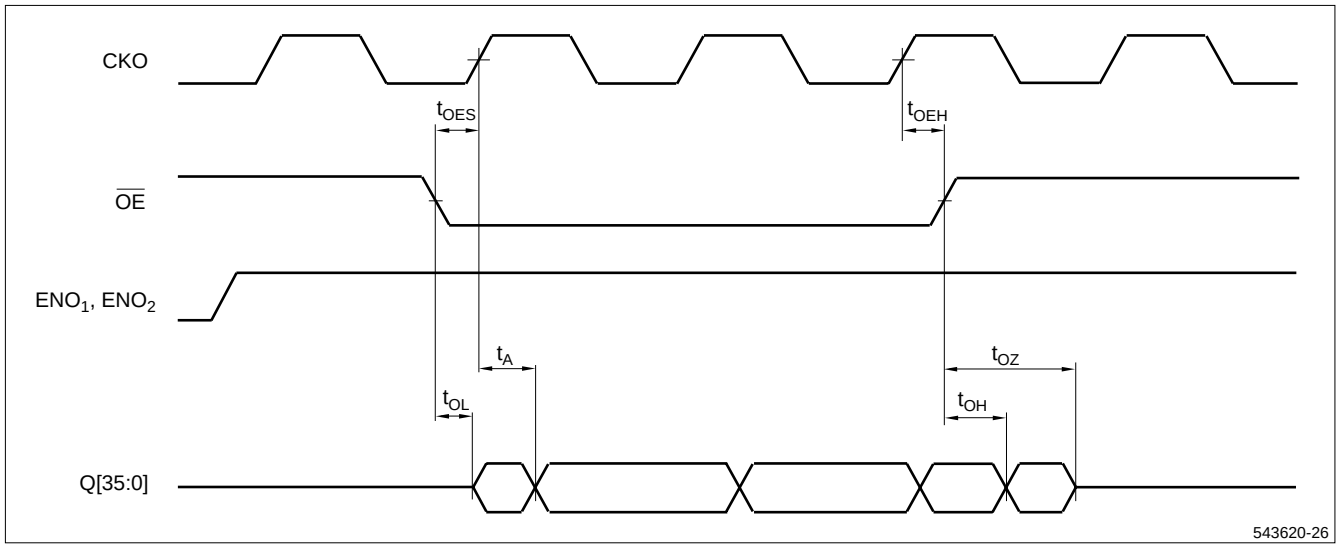
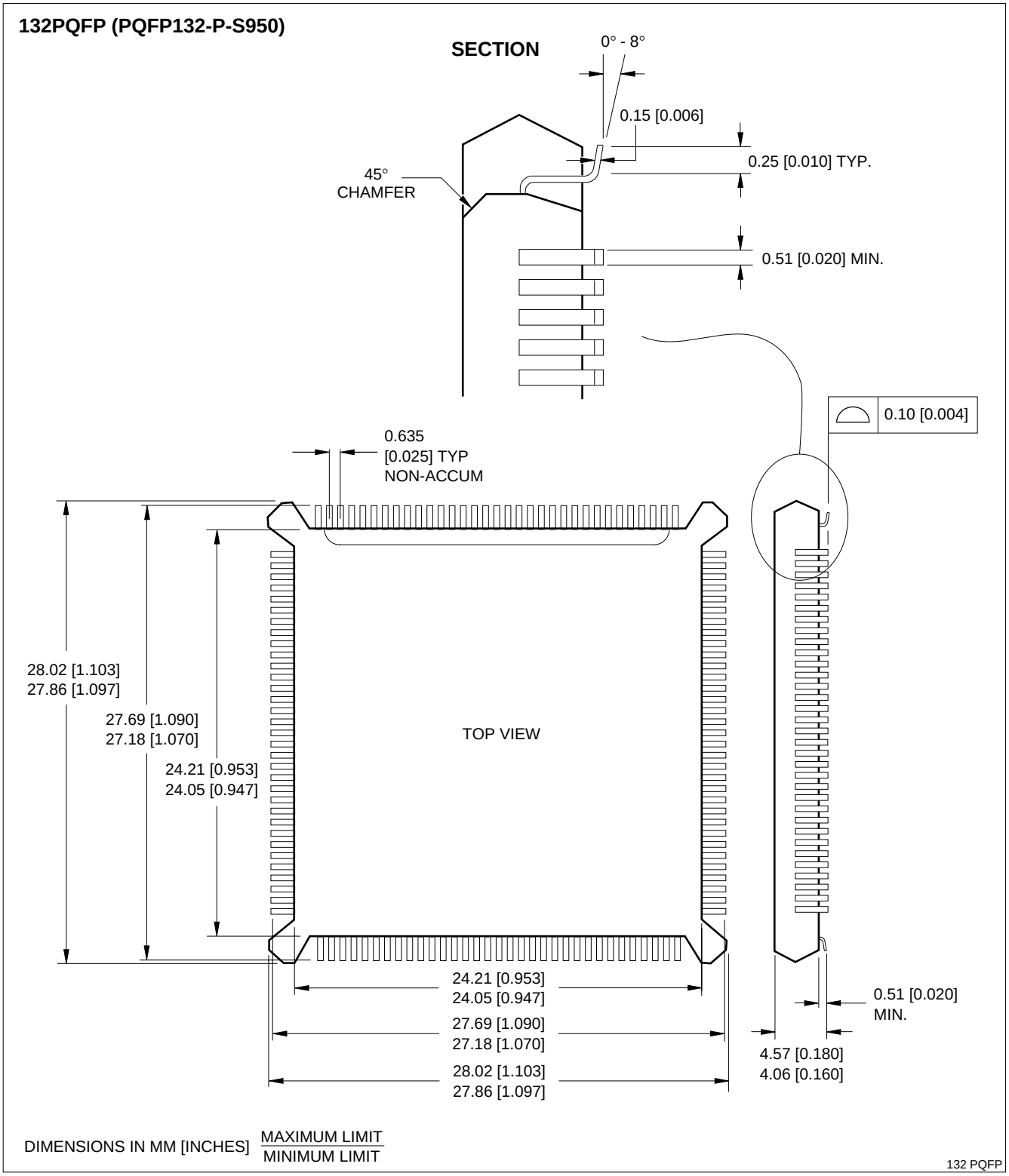


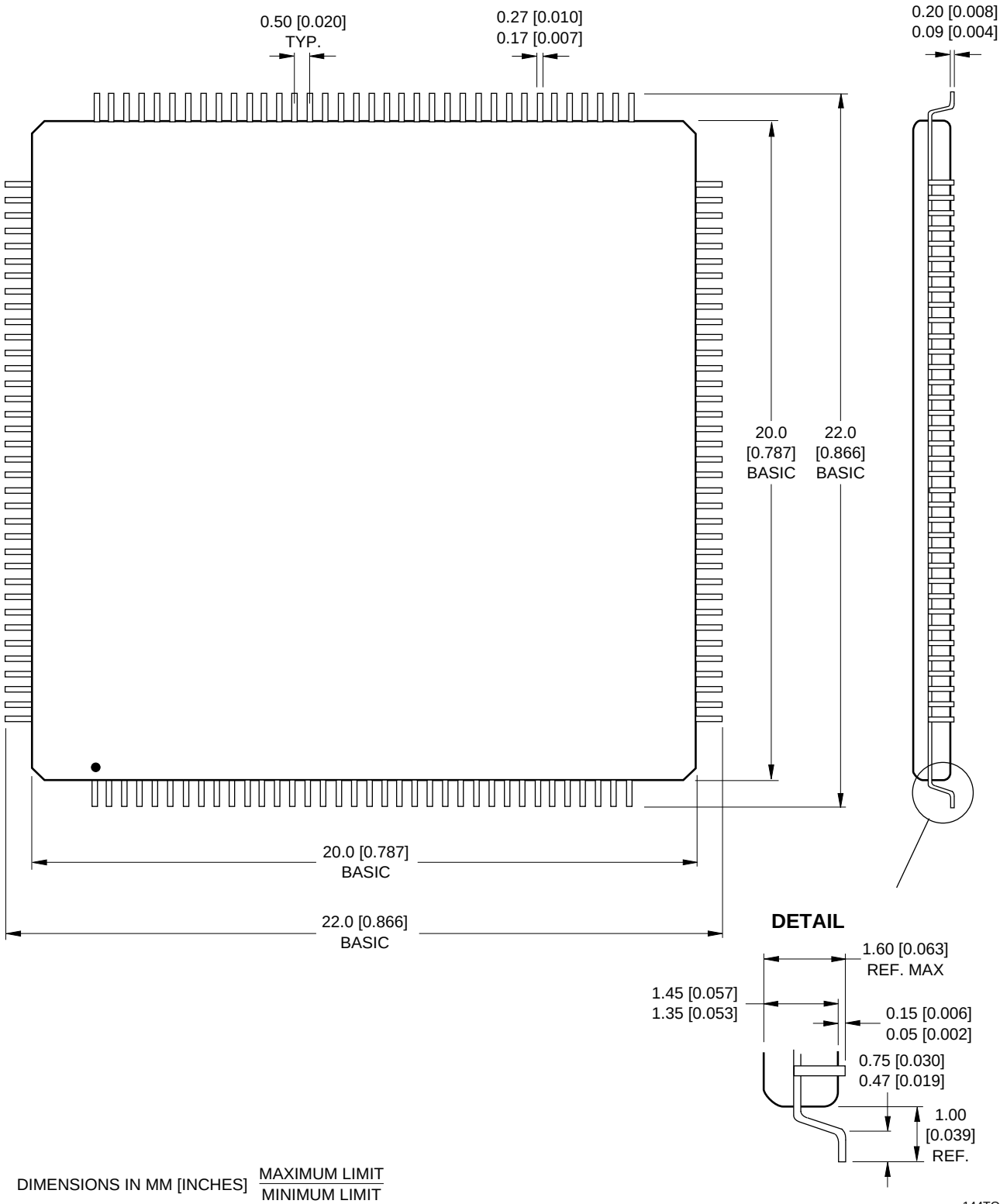
Figure 28. $\overline{OE}$ When Bit 6 of the Control Register is HIGH

PACKAGE DIAGRAM



132-pin PQFP

144TQFP (TQFP-144-P-2020)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

144TQFP

ORDERING INFORMATION