LH5PV8512

CMOS 4M (512K × 8) Pseudo-Static RAM

FEATURES

- 524,288 words × 8 bit organization
- $\overline{CE}$ access time (t_{CEA}): 120 ns (MAX.)
- Cycle time (t_{RC}): 190 ns (MIN.)
- Power supply:
  +3.0 V ± 0.15 V (Operating)
  +2.2 V to +3.15 V (Data retention)
- Power consumption (MAX.):
  126 mW (Operating)
  95 µW (Standby = CMOS input level)
  221 µW (Self-refresh = CMOS input level)
- Available for address refresh, auto-refresh, and self-refresh modes
- 2,048 refresh cycles/32 ms
- Address non-multiple
- Not designed or rated as radiation hardened
- Package:
  32-pin, 525-mil SOP
- Package material: Plastic
- Substrate material: P-type silicon
- Process: Silicon-gate CMOS
- Operating temperature: 0 - 70°C

DESCRIPTION

The LH5PV8512 is a 4M bit Pseudo-Static RAM with a 524,288 word × 8 bit organization. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo-static operation which eliminates external clock inputs, while having the same pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, existing 512K × 8 SRAM sockets can be filled with the LH5PV8512N with little or no changes. The advantage is the cost saving realized with the lower cost PSRAM.

The LH5PV8512 has the ability to fill the gap between DRAM and SRAM by offering low cost, low power standby and simple interface.

PIN CONNECTIONS

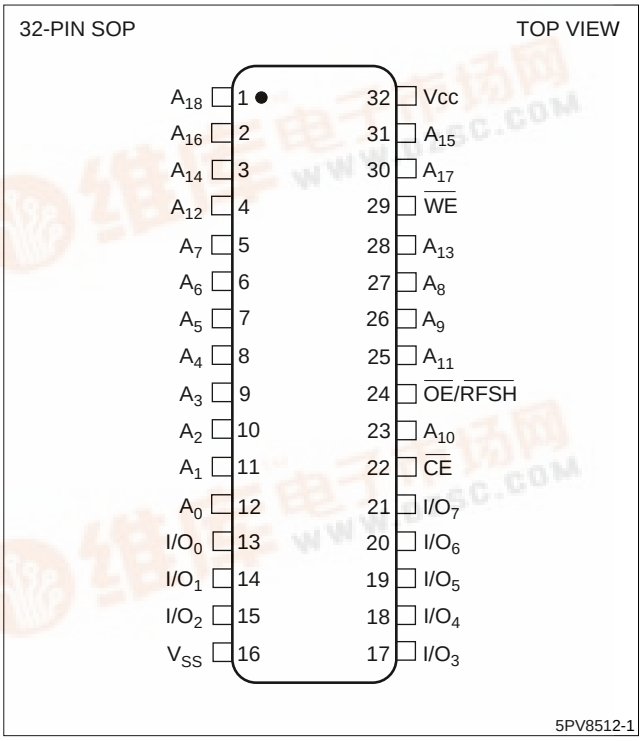


Figure 1. Pin Connections

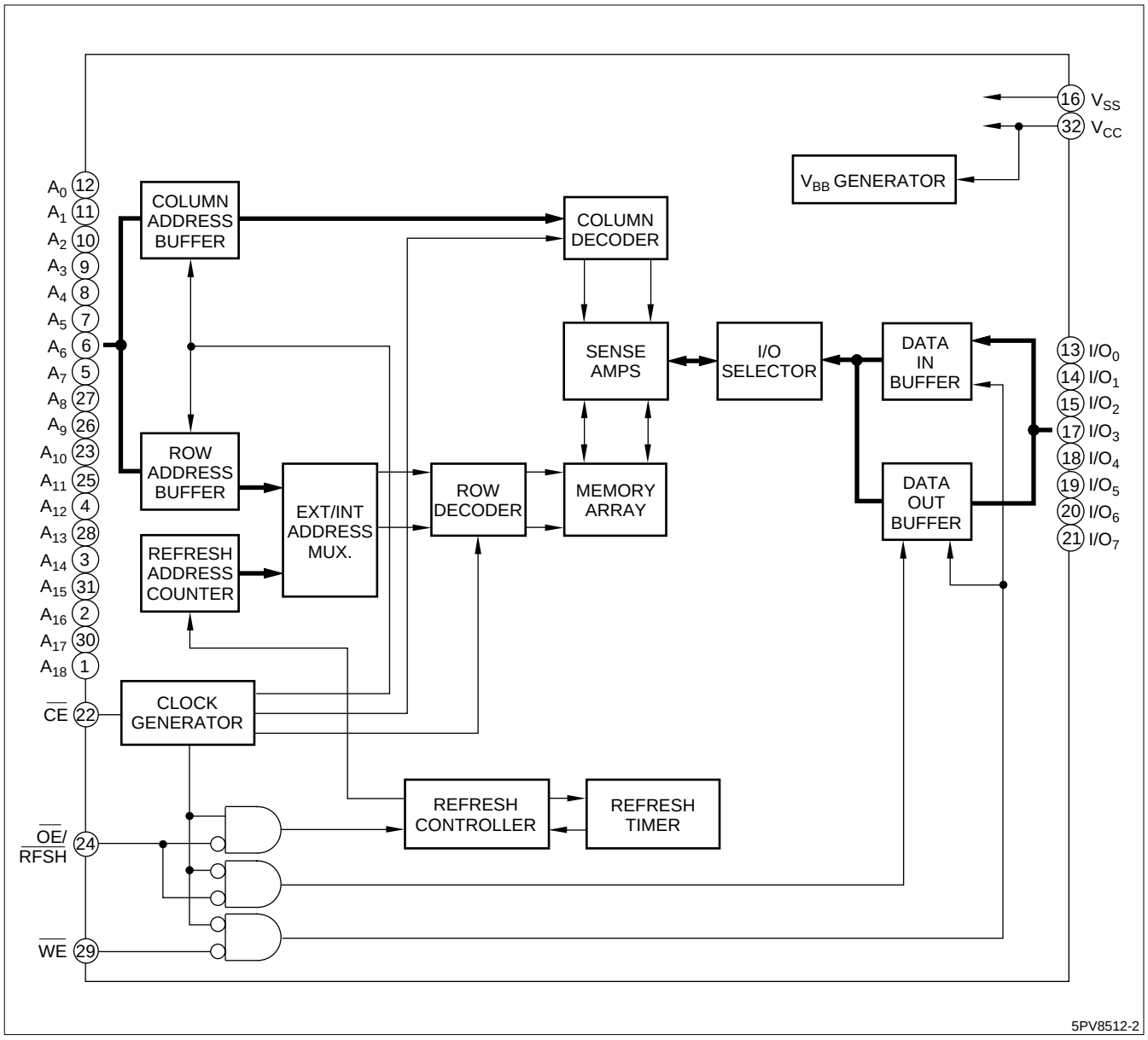


Figure 2. LH5PV8512 Block Diagram

PIN DESCRIPTION

PIN NAME	FUNCTION
A_0 - A_{18}	Address input
$\overline{WE}$	Write enable input
$\overline{OE}/\overline{RFSH}$	Output enable input Refresh control input

PIN NAME	FUNCTION
$\overline{CE}$	Chip enable input
I/O_0 - I/O_7	Data input/output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}/\overline{RFSH}$	$\overline{WE}$	I/O_{0-7}	MODE
L	L	H	Output data	Read
L	X	L	Input data	Write
L	H	H	High-Z	$\overline{CE}$ only refresh
H	L	X	High-Z	Auto-refresh
H	H	X	High-Z	Standby

NOTES:
1. X = H or L
2. If $\overline{RFSH}$ = L, it is necessary to meet t_{OEH} and t_{OCD}.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on all pins	V_T	-0.5 to +4.6	V	1
Operating temperature	T_{OPR}	0 to +70	°C	—
Storage temperature	T_{STG}	-65 to +150	°C	—
Output short circuit current	I_O	50	mA	—
Power dissipation	P_D	600	mW	—

NOTE:
1. The maximum applicable voltage on any pin with respect to V_{SS}.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	2.85	3.0	3.15	V	1
	V_{SS}	0	0	0	V	—
Input voltage	V_{IH}	2.4	—	4.5	V	—
	V_{IL}	-0.5	—	0.6	V	—

NOTE:
1. When the supply voltage falls down under the above recommended supply voltage by temporarily power-down, a wait time longer than 400 ms is necessary at V_{CC} = 0 V before the next power-up. After the supply voltage rises and gets stable, a pause of 100 µs with $\overline{CE}$ = $\overline{RFSH}$ = V_{IH} and 8 dummy cycles are also necessary after the rises.

PIN CAPACITANCE (T_A = +25°C, f = 1 MHz, V_{CC} = 3.0 V)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT	NOTE
Input capacitance	A_0 - A_{18}	C_{IN1}	—	8	pF	1
	$\overline{WE}$, $\overline{OE}/\overline{RFSH}$	C_{IN2}	—	8	pF	1
	$\overline{CE}$	C_{IN3}	—	8	pF	1
Input/output capacitance	I/O_0 - I/O_7	C_{OUT1}	—	10	pF	1

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 3.0 V ± 0.15 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	I_{CC1}	t_{RC} = 190 ns	—	40	mA	1
Average supply current in standby mode	I_{CC2}	$\overline{CE}$, $\overline{OE}$, $\overline{RFSH}$ = V_{IH}	—	0.5	mA	—
		$\overline{CE}$, $\overline{OE}$, $\overline{RFSH}$ = V_{CC} - 0.2 V	—	30	mA	—
Average supply current in self-refresh cycle	I_{CC3}	$\overline{CE}$ = V_{IH} $\overline{OE}$/$\overline{RFSH}$ = V_{IL}	—	0.5	mA	—
		$\overline{CE}$ = V_{CC} - 0.2 V, $\overline{OE}$, $\overline{RFSH}$ = 0.2 V	—	70	mA	—
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{CC} + 0.3 V 0 V on all other pins	-5	5	µA	—
I/O leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V Input/output pins in High-Z	-5	5	µA	—
Output HIGH voltage	V_{OH}	I_{OUT} = -1 mA	2.4	—	V	—
Output LOW voltage	V_{OL}	I_{OUT} = 2.1 mA	—	0.4	V	—

NOTE:

1. The input/output pins are in high impedance state. I_{CC1} depends on the cycle time.

AC ELECTRICAL CHARACTERISTICS [1, 2, 3, 4, 5] (T_A = 0 to +70°C, V_{CC} = 3.0 V ± 0.15 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
Random read, write cycle time	t_{RC}	190	—	ns	—
Random modify write cycle time	t_{RMW}	250	—	ns	—
$\overline{CE}$ pulse width	t_{CE}	120	10,000	ns	—
$\overline{CE}$ precharge time	t_P	70	—	ns	—
Address setup time	t_{AS}	0	—	ns	6
Address hold time	t_{AH}	30	—	ns	6
Read command setup time	t_{RCS}	0	—	ns	—
Read command hold time	t_{RCH}	0	—	ns	—
$\overline{CE}$ access time	t_{CEA}	—	120	ns	7
$\overline{OE}$ access time	t_{OEA}	—	60	ns	7
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20	—	ns	8
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0	—	ns	8
Write disable to output in Low-Z	t_{WLZ}	5	—	ns	8
Chip disable to output in High-Z	t_{CHZ}	0	30	ns	8
Output disable to output in High-Z	t_{OHZ}	—	30	ns	8
$\overline{WE}$ to output in High-Z	t_{WHZ}	—	30	ns	8
$\overline{OE}$ set up time from $\overline{CE}$	t_{OES}	0	—	ns	—
$\overline{OE}$ hold time from $\overline{CE}$	t_{OEH}	15	—	ns	—
$\overline{OE}$ setup time from chip disable	t_{OCD}	0	—	ns	—
Write command pulse width	t_{WP}	35	—	ns	—
Write command setup time	t_{WCS}	35	10,000	ns	—
Write command hold time	t_{WCH}	120	10,000	ns	—
Data setup time from write disable	t_{DSW}	30	—	ns	9
Data setup time from chip disable	t_{DSC}	30	—	ns	9
Data hold time from write disable	t_{DHW}	0	—	ns	9
Data hold time from chip disable	t_{DHC}	0	—	ns	9
Transition time (rise and fall)	t_T	2	50	ns	—
Refresh time interval (2,048 cycle)	t_{REF}	—	32	ms	10, 13, 14
Auto refresh cycle time	t_{FC}	190	—	ns	—
Refresh delay time from $\overline{CE}$	t_{RFD}	70	—	ns	—
Refresh pulse width (Auto refresh)	t_{FAP}	80	8,000	ns	11, 15
Refresh precharge time (Auto refresh)	t_{FP}	40	—	ns	—
Refresh pulse width (Self refresh)	t_{FAS}	8	—	ms	11, 12, 13, 14, 15
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	600	—	ns	—

DATA RETENTION CHARACTERISTICS [12, 13, 14, 15, 16, 17, 18, 19, 20] (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
Data retention voltage	V_R	2.2	3.15	V	—
Data retention current (V_{CC} = 3.15 V, $\overline{CE}$ = V_{CC} - 0.2 V, $\overline{OE}$/$\overline{RFSH}$ = 0.2 V)	I_{CCDR}	—	70	µA	—
Refresh setup time	t_{FS}	0	—	ns	—
Recover time from data retention mode	t_{FR}	5	—	ms	—

NOTES:

1. AC characteristics are measured at t_T = 2 ns.
2. AC characteristics are measured at the following condition:

	INPUT VOLTAGE		OUTPUT VOLTAGE	
	V_{IH}	V_{IL}	V_{OH}	V_{OL}
Input level	2.4 V	0.4 V	—	—
Input reference level	1.4 V	1.4 V	—	—
Output reference level	—	—	2.0 V	0.8 V

3. In order to initialize the circuit, $\overline{CE}$ and $\overline{OE}$/$\overline{RFSH}$ should be kept V_{IH} for 100 µs after power-up and followed by at least 8 dummy cycles.
4. If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffer proir to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on outputs buffer.
5. Because a PSRAM operates dynamically like a DRAM, it is recommended to put bypass capacitors between V_{CC} and GND to absorb power supply noise due to the peak current.
6. Address signals are latched in the memory at the falling edge of $\overline{CE}$.
7. Measured with a load equivalent to 50 pF.
8. t_{CLZ}, t_{OLZ}, t_{WLZ}, t_{CHZ}, t_{OHZ}, and t_{WHZ} are sampled, and not 100% tested. t_{CHZ}, t_{OHZ}, and t_{WHZ} define the time at which the output achieves the open circuit condition and they are not referenced to output voltage levels.
9. Input data is latched in the memory at the earlier rising edge of $\overline{CE}$ and $\overline{WE}$.
10. $\overline{CE}$ only refresh or auto-refresh is needed to be executed 2,048 times within 32 ms.
11. Auto-refresh and self-refresh are defined by $\overline{OE}$/$\overline{RFSH}$ pulse width during $\overline{CE}$ = V_{IH}. If $\overline{OE}$/$\overline{RFSH}$ pulse width is shorter than t_{FAP} (MAX.), the cycle is an auto-refresh cycle and memory cells are refreshed by an internal address counter. If $\overline{OE}$/$\overline{RFSH}$ pulse width is longer than t_{FAS} (MIN.), the cycle is a self-refresh cycle and memory cells are refreshed by an internal clock generator automatically.
12. If $\overline{CE}$ only refresh is used during normal read/write cycles, the first address refresh must be started within 15 µs after self-refresh or data retention mode ends, and the $\overline{CE}$ only refresh must be executed continuously for 2,048 refresh cycles.
13. If distributed auto-refresh is used during normal read/write cycles, the first auto-refresh must be started within 15 µs after self-refresh or data retention mode ends.
14. If burst auto-refresh is used during normal read/write cycles, the first auto-refresh must be started within 15 µs after self-refresh or data retention mode ends, and the auto-refresh must be executed continuously for 2,048 refresh cycles.
15. After 8,000 ns (t_{FAP} (MAX.)) from $\overline{RFSH}$ falling, the memory resets its internal address counter and enters self-refresh cycle. At the beginning of the self-refresh cycle, it takes longer than 8 ms (t_{FAS} (MIN.)) for all addresses to be refreshed. Therefore, in case that the $\overline{RFSH}$ = L pulse length is from 8,000 ns to 8 ms, refresh all addresses by external clocks within 32 ms before the self-refresh to keep refresh time interval (t_{REF}).
16. After self-refresh cycle or data retention mode ends, t_{FRS} (MIN.) is necessary to reset the refresh operation. $\overline{CE}$ and $\overline{OE}$/$\overline{RFSH}$ should kept V_{IH} for t_{FRS} (MIN.).
17. The data retention period is longer than t_{FAS} (MIN.) like self-refresh cycle.
18. $\overline{OE}$/$\overline{RFSH}$ must be lower than 0.2 V during the data retention period.
19. $\overline{CE}$ must be higher than V_{CC} - 0.2 V during the data retention period.
20. The transition time of the supply voltage in data retention mode must be slower than 0.05 V/ms.

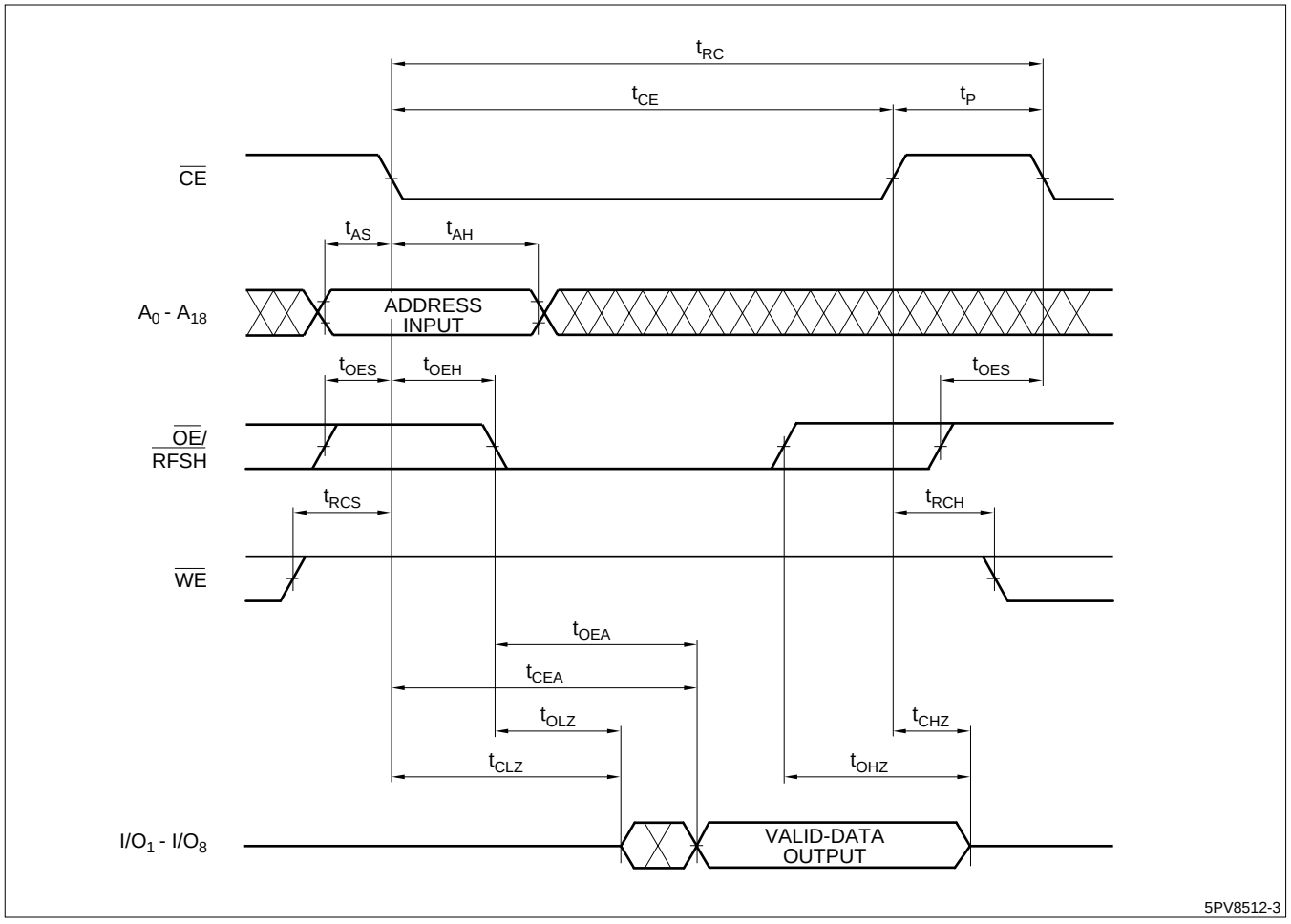


Figure 3. Read Cycle

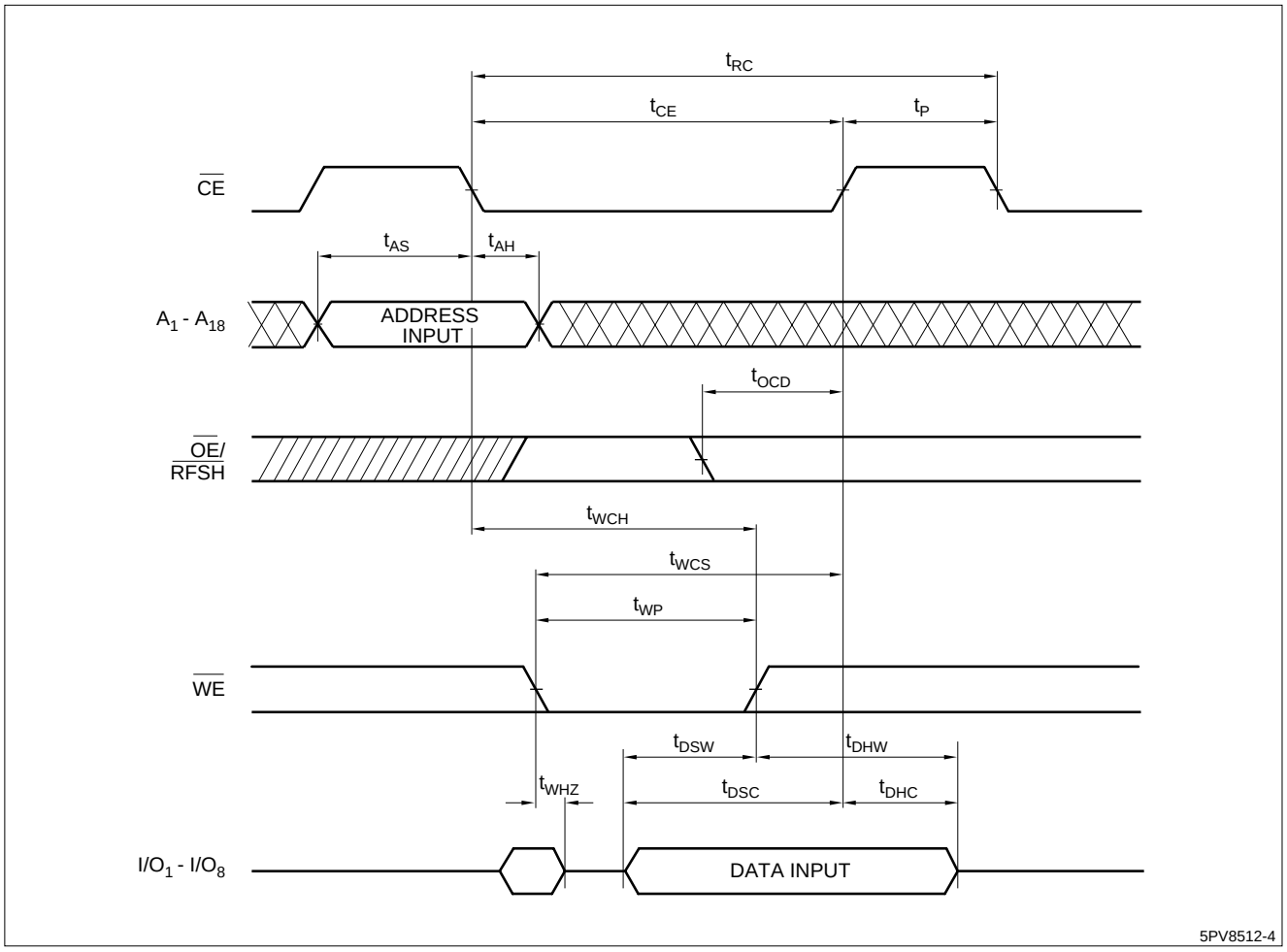


Figure 4. Write Cycle

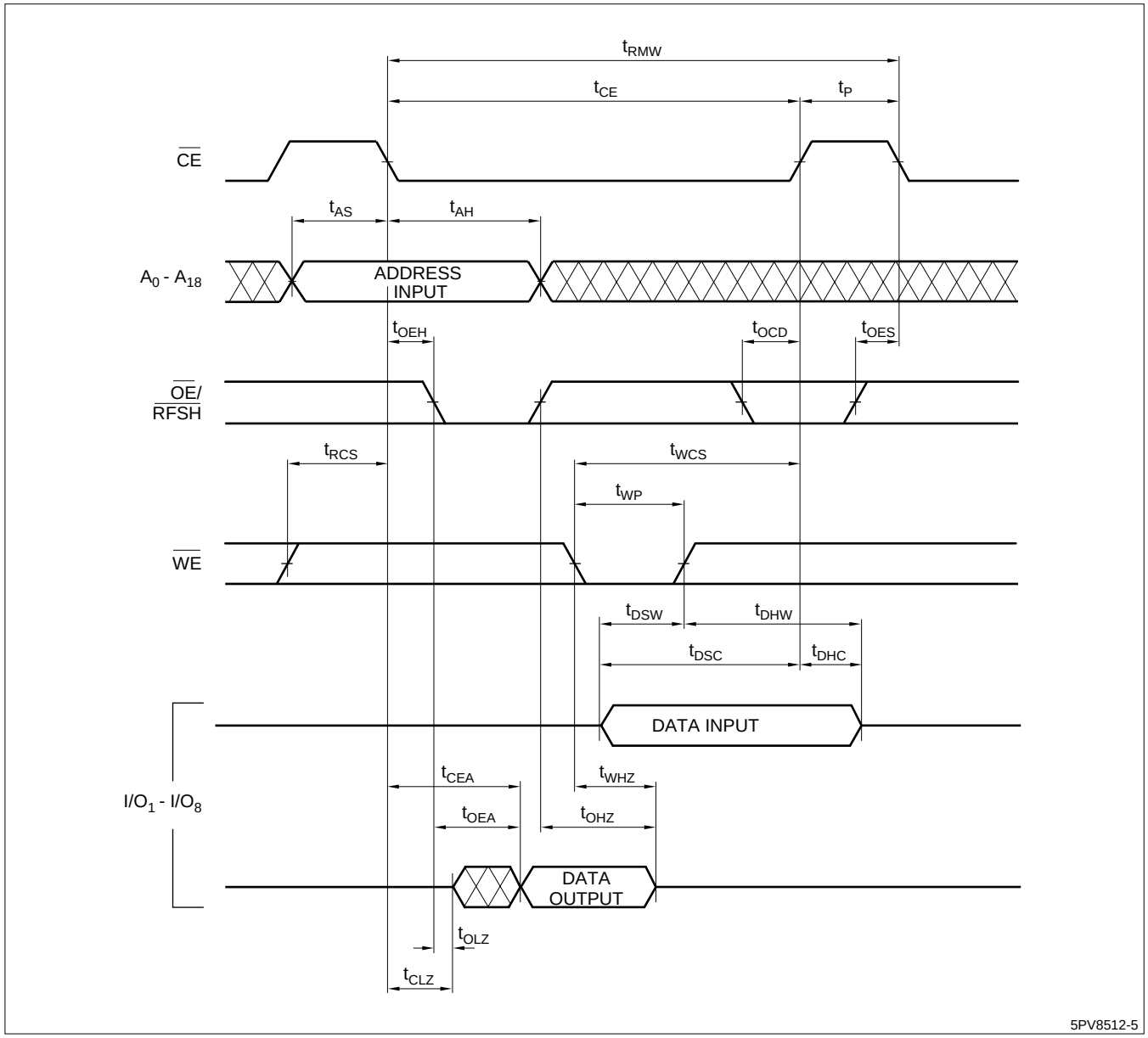


Figure 5. Read/Write Cycle

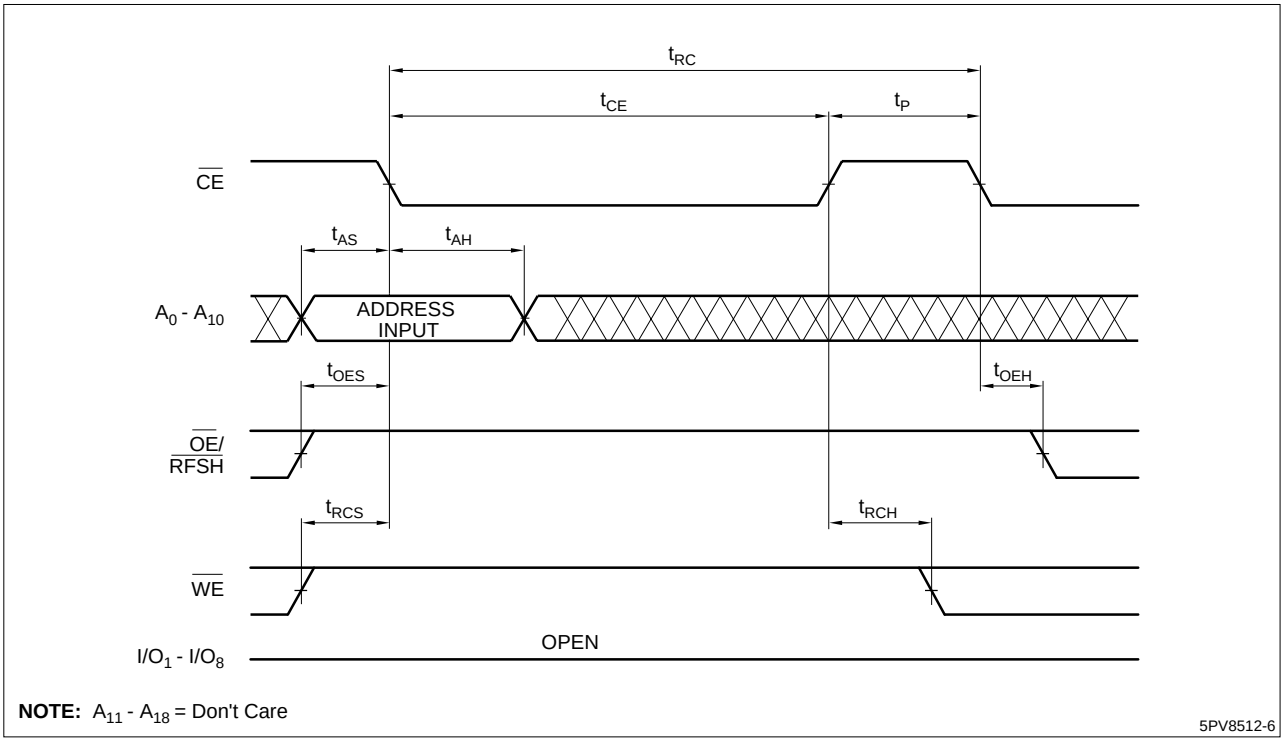


Figure 6. $\overline{CE}$ Only Refresh Cycle

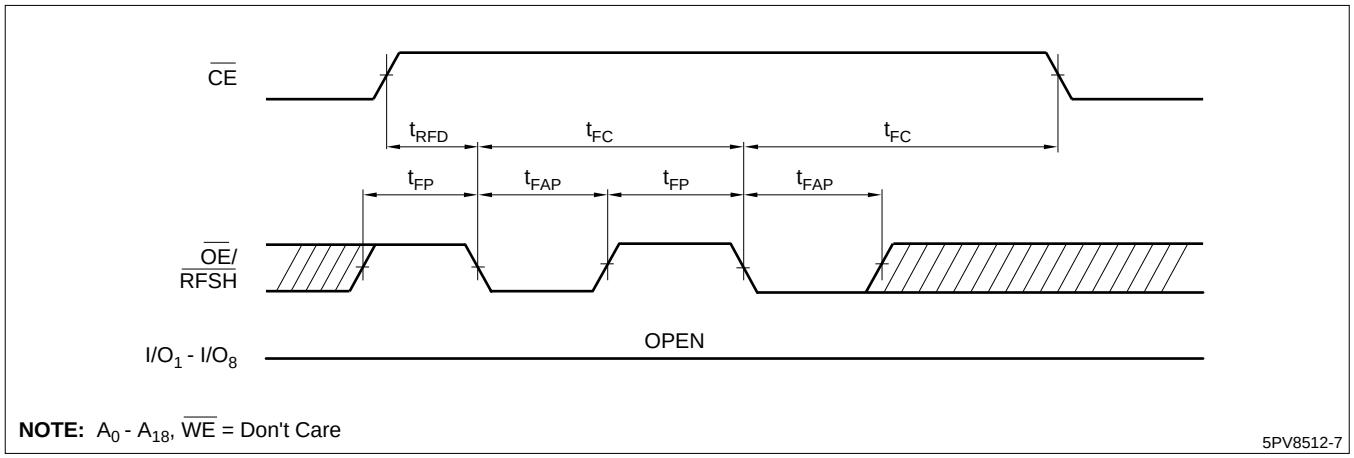


Figure 7. Auto-Refresh Cycle

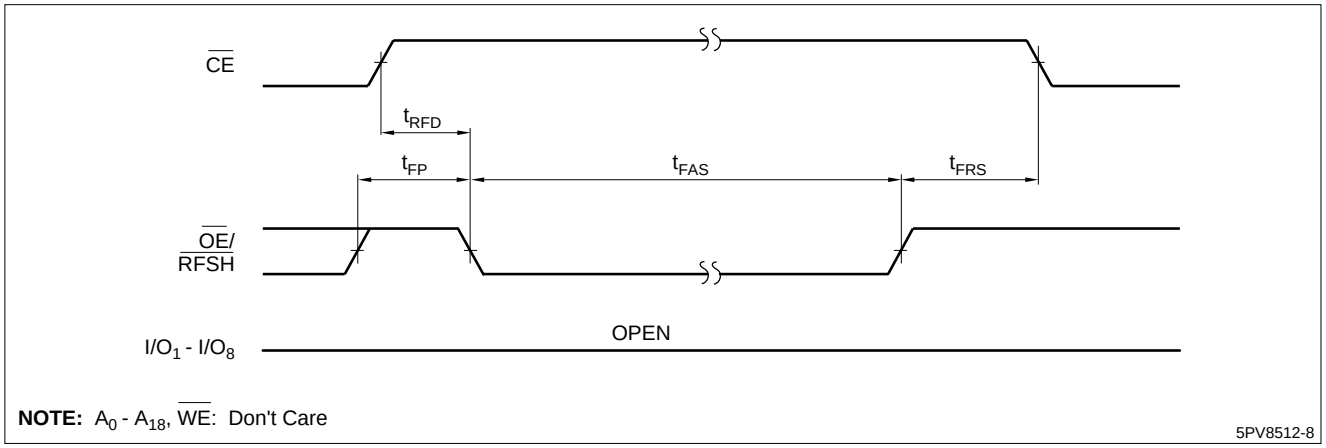


Figure 8. Self-Refresh Cycle

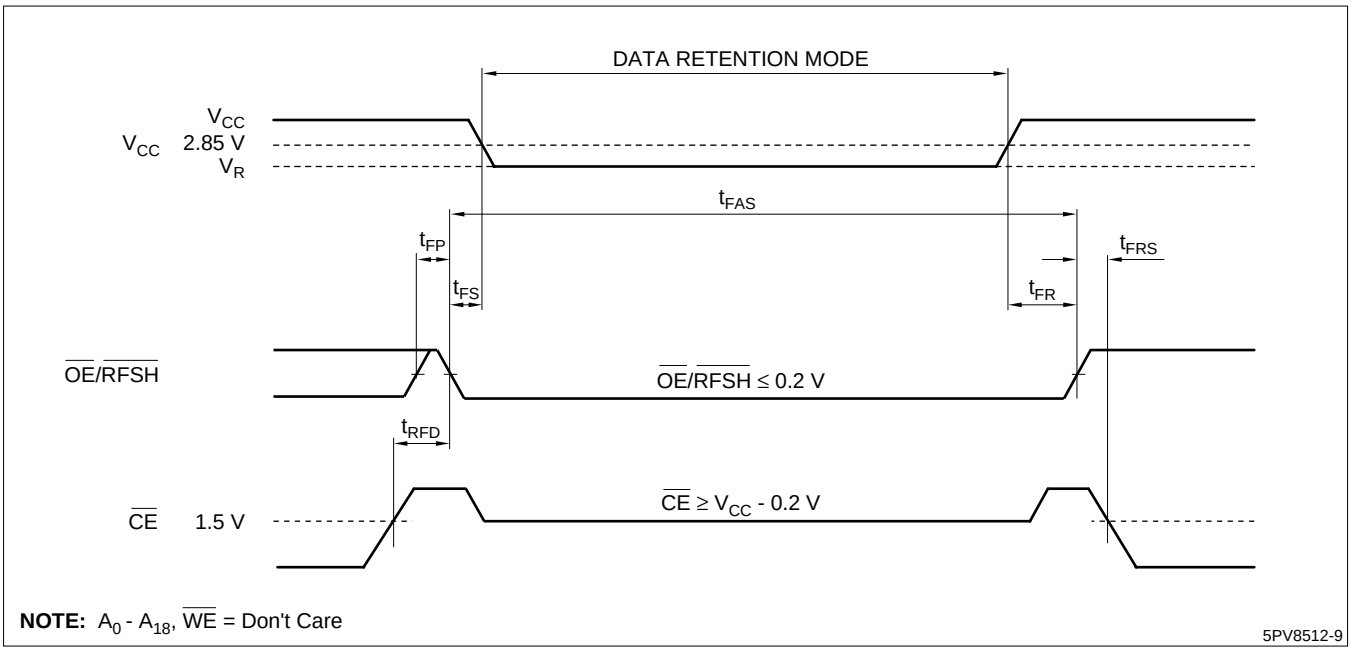
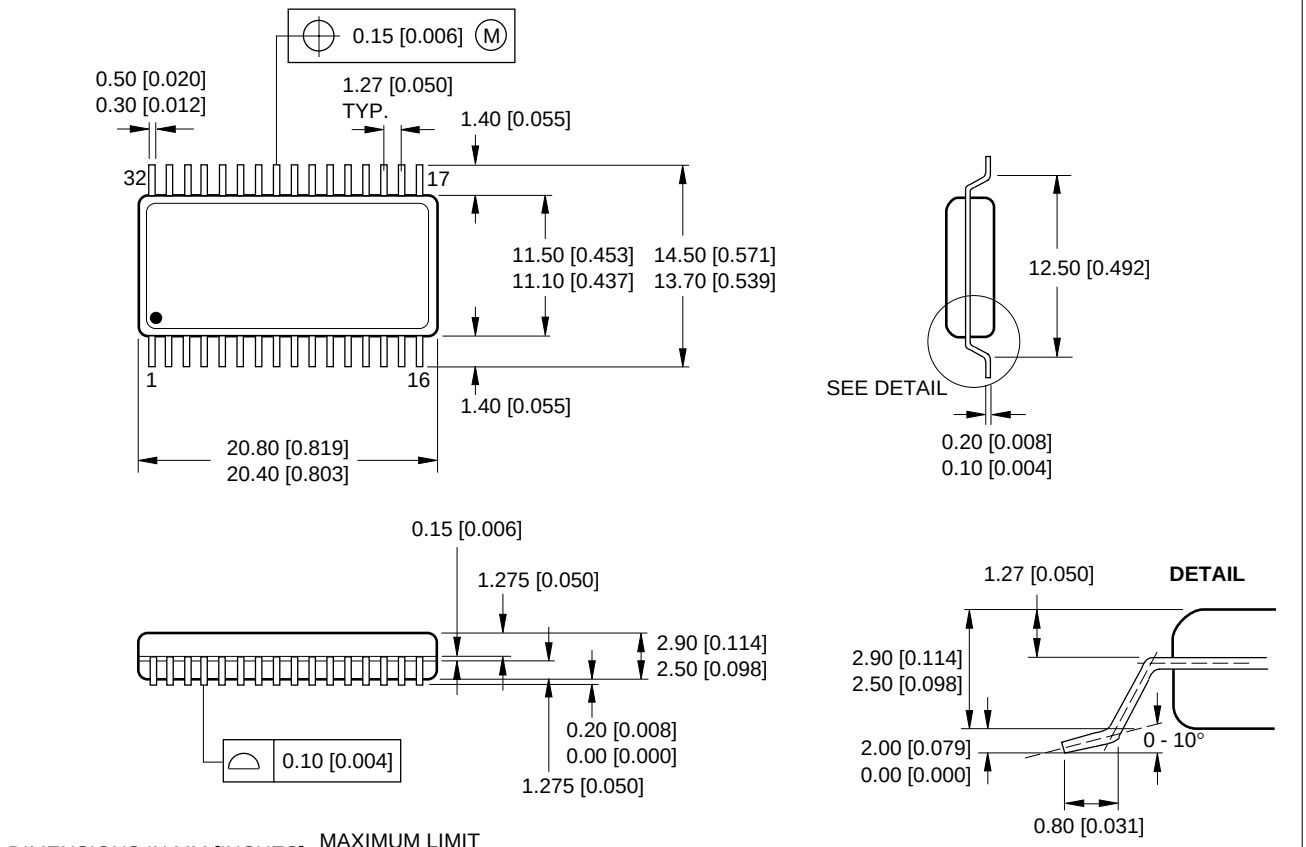


Figure 9. Data Retention Mode

PACKAGE DIAGRAM

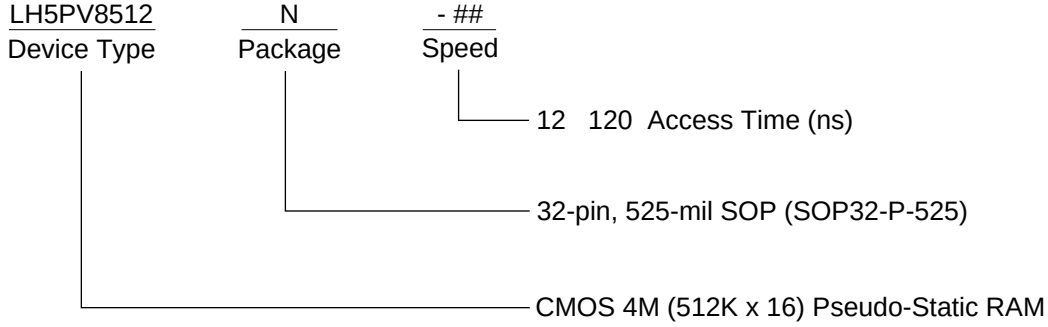
32SOP (SOP32-P-525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32SOP-2

ORDERING INFORMATION



Example: LH5PV8512N-12 (CMOS 4M (512K x 16) Pseudo-Static RAM, 120 ns, 32-pin, 525-mil SOP)

5PV8512-10