

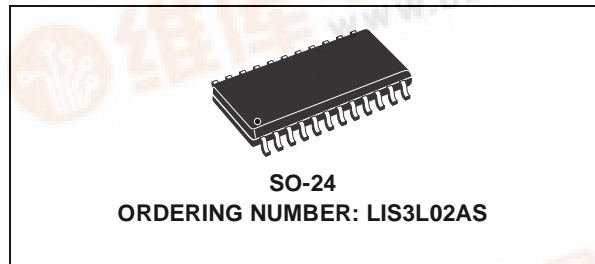


LIS3L02AS

INERTIAL SENSOR: 3Axis - 2g/6g LINEAR ACCELEROMETER

PRODUCT PREVIEW

- 3V TO 5.25V SINGLE SUPPLY OPERATION
- THE SENSITIVITY IS ADJUSTED WITH A TOTAL ACCURACY OF $\pm 10\%$
- THE OUTPUT VOLTAGE, OFFSET, SENSITIVITY AND TEST VOLTAGE ARE RATIOMETRIC TO THE SUPPLY VOLTAGE
- DEVICE SENSITIVITY IS ON-CHIP FACTORY TRIMMED
- EMBEDDED SELF TEST
- HIGH SHOCK SURVIVABILITY



DESCRIPTION

The LIS3L02AS is a tri-axis linear accelerometer that includes a sensing element and an IC interface able to take the information from the sensing element and to provide an analog signal to the external world.

The sensing element, capable to detect the acceleration, is manufactured using a dedicated process called THELMA (Thick Epi-Poly Layer for Microactuators and Accelerometers) developed by ST to produce inertial sensors and actuators in silicon.

The IC interface instead is manufactured using a CMOS process that allows high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LIS3L02AS has a user selectable full scale of

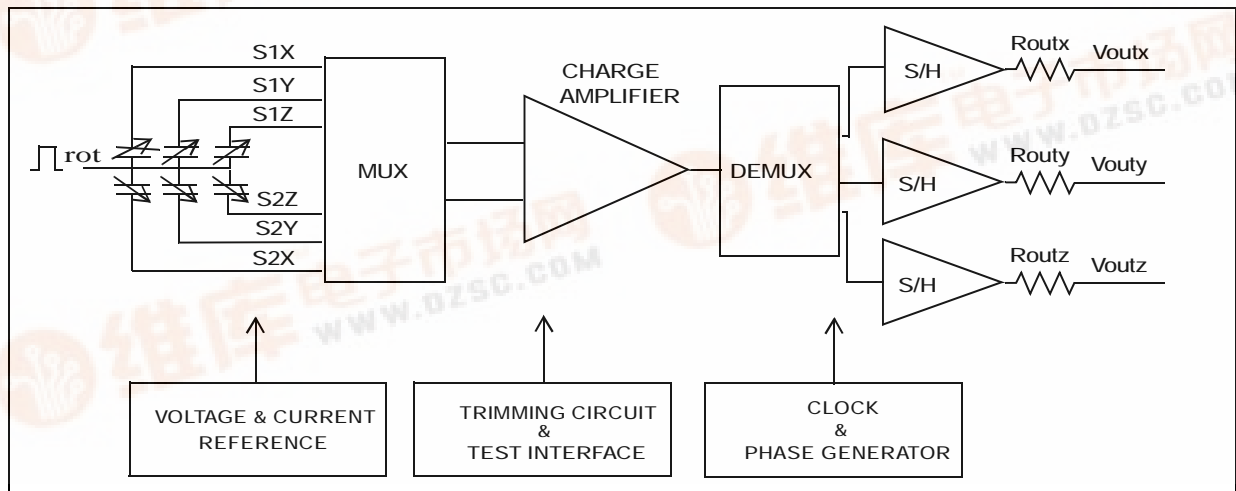
2g, 6g and it is capable of measuring accelerations over a maximum bandwidth of 4.0 KHz for the X and Y axis and 2.5KHz for the Z axis. The device bandwidth may be reduced by using external capacitances. A self-test capability allows the user to check the functioning of the system.

The LIS3L02AS is available in plastic SMD package and it is specified over a temperature range extending from -40°C to $+85^{\circ}\text{C}$.

The LIS3L02AS belongs to a family of products suitable for a variety of applications:

- Antitheft systems
- Inertial navigation
- Virtual reality input devices
- Vibration Monitoring, recording and compensation
- Appliance control
- Robotics

BLOCK DIAGRAM

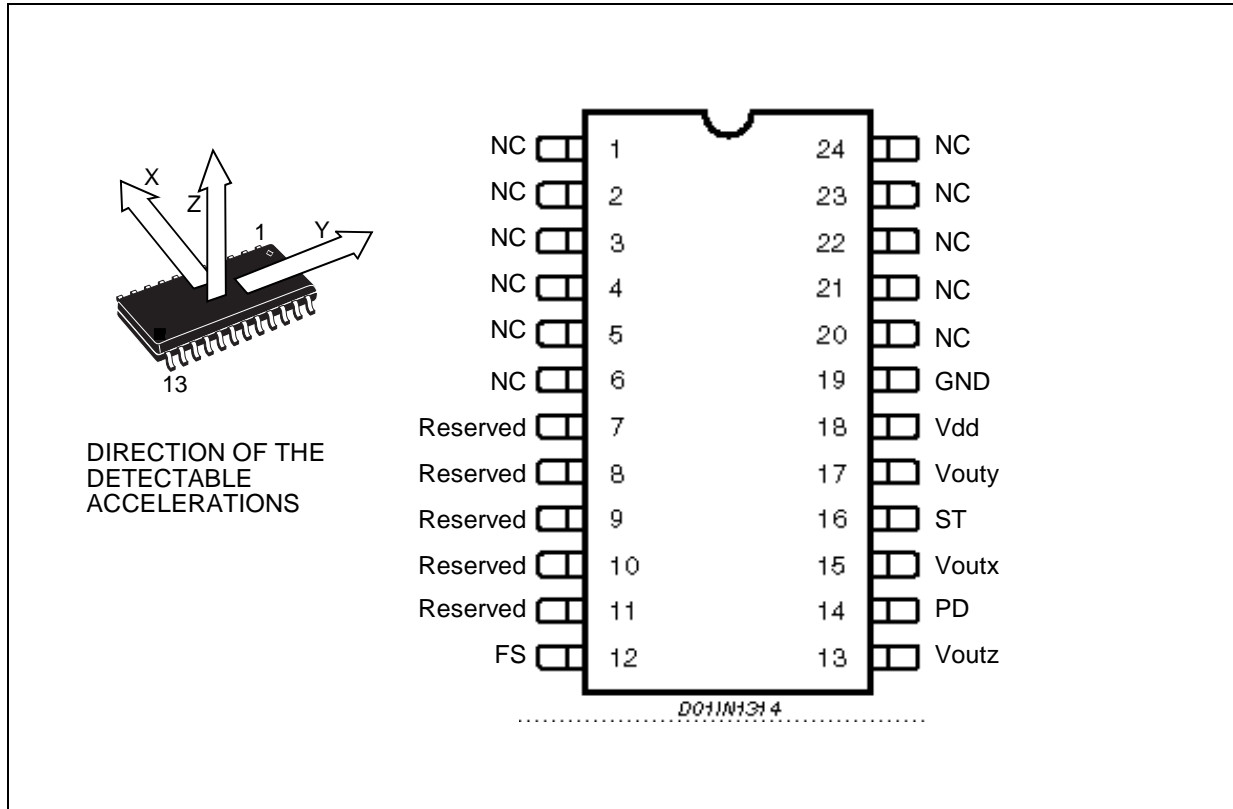


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PIN DESCRIPTION

| N° | Pin | Function |
|----------|----------|---|
| 1 to 6 | NC | Internally not connected |
| 7 | Reserved | Leave unconnected or connect to ground |
| 8 | Reserved | Leave unconnected or connect to Vdd |
| 9 | Reserved | Connect to Vdd or ground |
| 10-11 | Reserved | Leave unconnected or connect to Vdd |
| 12 | FS | Full Scale selection (Logic 0: 2g Full-scale; Logic 1: 6g Full-scale) |
| 13 | Voutz | Output Voltage |
| 14 | PD | Power Down (Logic 0: normal mode; Logic 1: Power-Down mode) |
| 15 | Voutx | Output Voltage |
| 16 | ST | Self Test (Logic 0: normal mode; Logic 1: Self-test) |
| 17 | Vouty | Output Voltage |
| 18 | Vdd | Power supply |
| 19 | GND | 0V supply |
| 20 to 24 | NC | Internally not connected |

PIN CONNECTION (Top view)



ELECTRICAL CHARACTERISTICS (Temperature range -40°C to +85°C)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|--------|--|--|------------|--------|------------|--------|
| Vdd | Supply voltage | | 3 | | 5.25 | V |
| Idd | Supply current | | | 1.0 | | mA |
| Voff | Zero-g level | T = 25°C ratiometric to Vdd | Vdd/2-10% | Vdd/2 | Vdd/2+10% | V |
| Ar | Acceleration range | 0V on FS pin | ±1.8 | ±2.0 | ±2.2 | g |
| | | Vdd on FS pin | | ±±6.0 | | g |
| So | Sensitivity ratiometric to Vdd | T = 25°C Full-scale = 2g | Vdd/5-10% | Vdd/5 | Vdd/5+10% | V/g |
| | | T = 25°C Full-scale = 6g | Vdd/15-10% | Vdd/15 | Vdd/15+10% | V/g |
| NL | Non Linearity | Best fit straight line X, Y axis Full-scale = 2g | | ±0.3 | | % |
| | | Best fit straight line Z axis Full-scale = 2g | | ±0.6 | | % |
| fuc | Sensing Element Resonant Frequency | X, Y axis | | 4.0 | | KHz |
| | | Z axis | | 2.5 | | KHz |
| an | Acceleration noise density | Vdd=5V Full-scale = 2g | | 100 | | µg/√Hz |
| Vt | Self test output voltage Ratiometric to Vdd | T = 25°C @ 5V | | TBD | | V |
| Vst | Self test input | Logic 0 level | 0 | | 0.8 | V |
| | | Logic 1 level | 2.8 | | Vdd | V |
| Rout | Output impedance | | | 100 | | kΩ |
| Cload | Capacitive load drive | | 320 | | | pF |

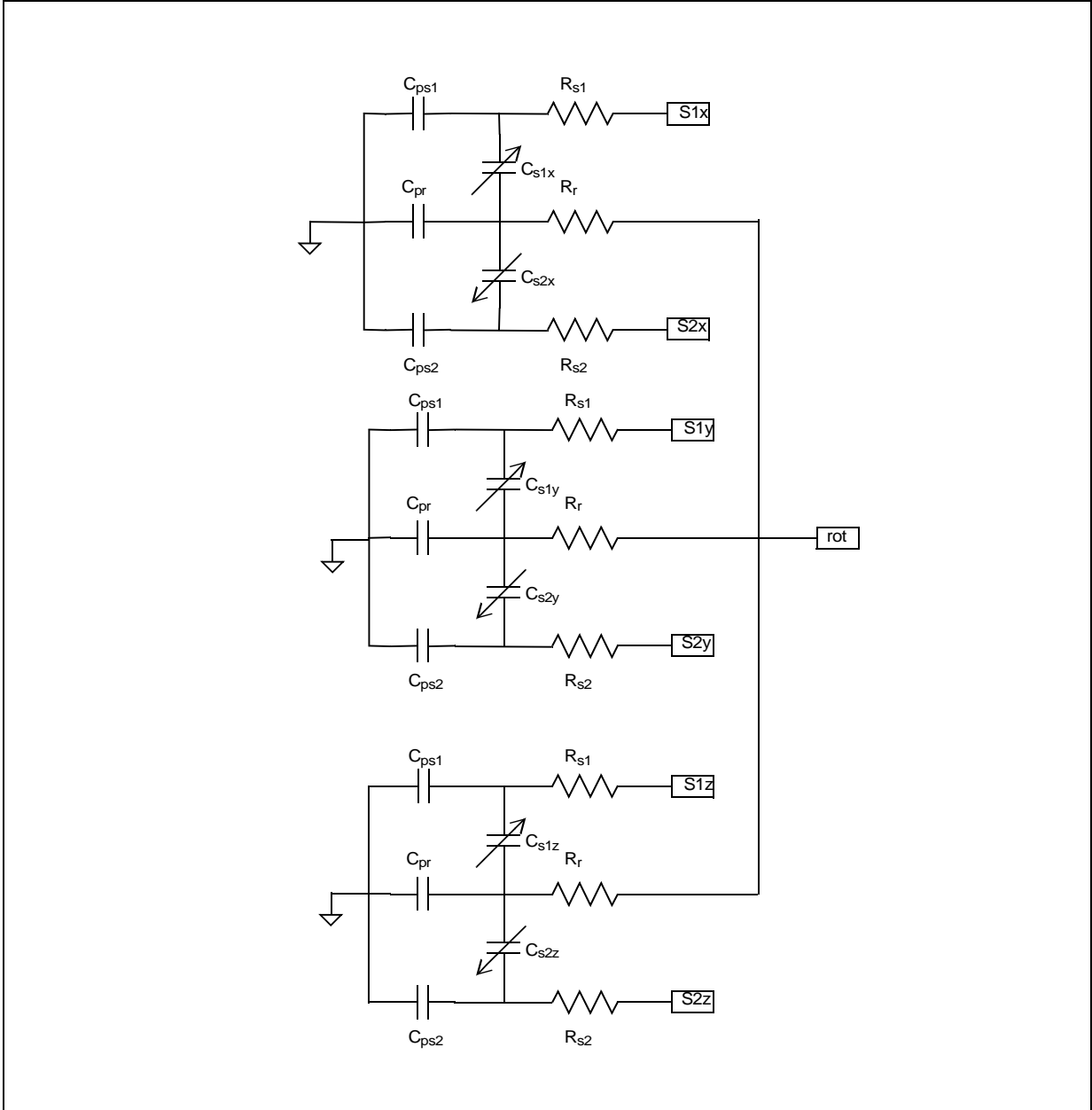
1 FUNCTIONALITY**1.1 Sensing element**

The THELMA process is utilized to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and free to move on a plane parallel to the substrate itself. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase.

The equivalent circuit for the sensing element is shown in the below figure; when a linear acceleration is applied, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

The nominal value of the capacitors, at steady state, is few pF and when an acceleration is applied the maximum variation of the capacitive load is few tenth of pF.

Figure 1. Equivalent electrical circuit



1.2 IC Interface

The complete signal processing uses a fully differential structure, while the final stage converts the differential signal into a single-ended one to be compatible with the external world.

The first stage is a low-noise capacitive amplifier that implements a Correlated Double Sampling (CDS) at its output to cancel the offset and the $1/f$ noise. The produced signal is then sent to three different S&Hs, one for each channel, and made available to the outside.

The low noise input amplifier operates at 200 kHz while the three S&Hs operate at a sampling frequency of 66 kHz. This allows a large oversampling ratio, which leads to in-band noise reduction and to an accurate output waveform.

All the analog parameters (output offset voltage and sensitivity) are ratiometric to the voltage supply. In-

creasing or decreasing the voltage supply, the sensitivity and the offset will increase or decrease linearly. The feature provides the cancellation of the error related to the voltage supply along an analog to digital conversion chain.

1.3 Factory calibration

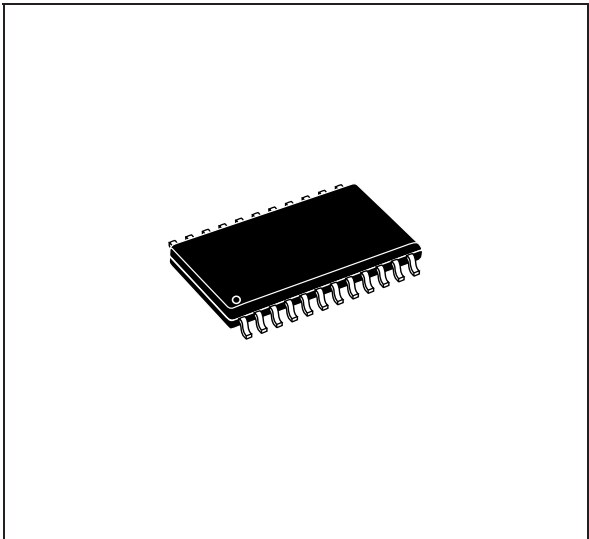
The IC interface is factory calibrated to provide to the final user a device ready to operate. The parameters which are trimmed are: gain, offset, common mode and internal clock frequency.

The trimming values are stored inside the device by a poly-fuse structure. Any time the device is turned on, the memorized bits are downloaded into the registers to be employed during the normal operation. The poly-fuse approach allows the final user to utilize the device without any need for further calibration

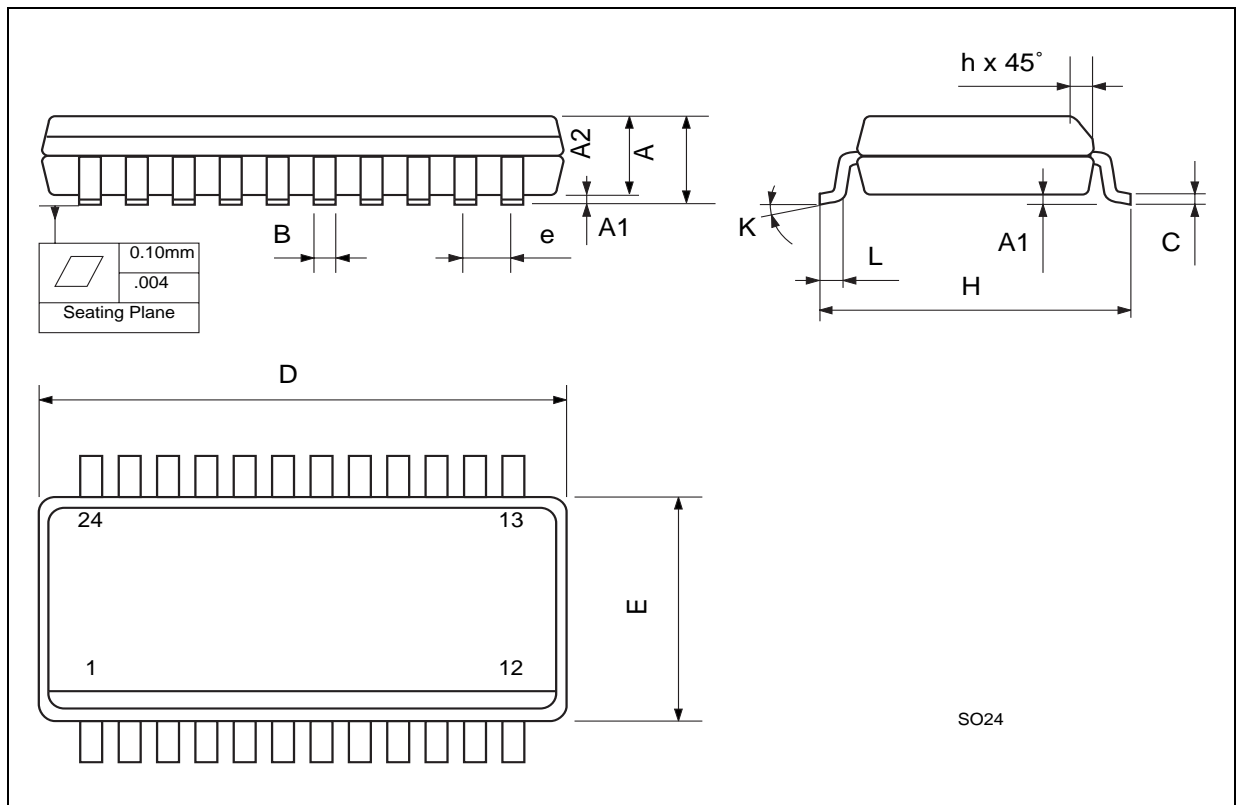
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| DIM. | mm | | | inch | | |
|------|----------------------|------|-------|-------|-------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.35 | | 2.65 | 0.093 | | 0.104 |
| A1 | 0.10 | | 0.30 | 0.004 | | 0.012 |
| A2 | | | 2.55 | | | 0.100 |
| B | 0.33 | | 0.51 | 0.013 | | 0.0200 |
| C | 0.23 | | 0.32 | 0.009 | | 0.013 |
| D | 15.20 | | 15.60 | 0.598 | | 0.614 |
| E | 7.40 | | 7.60 | 0.291 | | 0.299 |
| e | | 1.27 | | | 0,050 | |
| H | 10.0 | | 10.65 | 0.394 | | 0.419 |
| h | 0.25 | | 0.75 | 0.010 | | 0.030 |
| k | 0° (min.), 8° (max.) | | | | | |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |

OUTLINE AND MECHANICAL DATA



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