查询LM3146供应商 捷多邦，专业PCB打样工厂，24小时加急出货

National Semiconductor

February 1995

LM3146 High Voltage Transistor Array

General Description

The LM3146 consists of five high voltage general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the dc through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3146 is supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

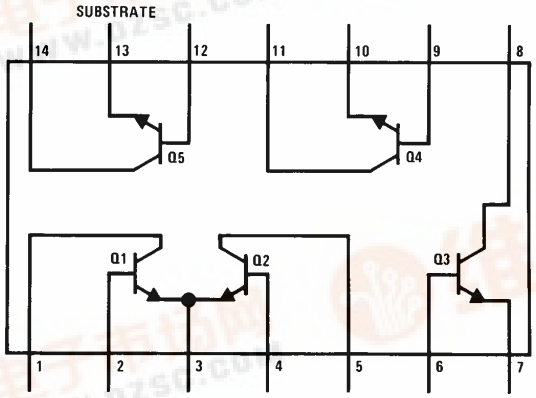
- High voltage matched pairs of transistors, V_{BE} matched ±5 mV, input offset current 2 μA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from dc to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from dc to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7959–1

Top View

Order Number LM3146M or LM3146N
See NS Package Number M14A or N14A

©1995 National Semiconductor Corporation TL/H/7959 RRD-B30M115/Printed in U. S. A.

找PDF 维库一下 pdf.dzsc.com

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM3146	Units
Power Dissipation: Each transistor		
$T_A = 25°C$ to 55°C	300	mW
$T_A > 55°C$	Derate at 6.67	mW/°C
Power Dissipation: Total Package		
$T_A = 25°C$	500	mW
$T_A > 25°C$	Derate at 6.67	mW/°C
Collector to Emitter Voltage, V_{CEO}	30	V
Collector to Base Voltage, V_{CBO}	40	V
Collector to Substrate Voltage, V_{CIO} (Note 1)	40	V
Emitter to Base Voltage, V_{EBO} (Note 2)	5	V
Collector to Current, I_C	50	mA
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 ''Surface Mounting Methods and Their Effect on Product Reliability'' for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$	40	72		V
$V_{(BR)CEO}$	Collector to Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	30	56		V
$V_{(BR)CIO}$	Collector to Substrate Breakdown Voltage	$I_{CI} = 10\ \mu A$, $I_B = 0$, $I_E = 0$	40	72		V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage (Note 2)	$I_C = 0$, $I_E = 10\ \mu A$	5	7		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10V$, $I_E = 0$		0.002	100	nA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 10V$, $I_B = 0$		(Note 3)	5	μA
h_{FE}	Static Forward Current Transfer Ratio (Static Beta)	$I_C = 10$ mA, $V_{CE} = 5V$ $I_C = 1$ mA, $V_{CE} = 5V$ $I_C = 10\ \mu A$, $V_{CE} = 5V$	30	85 100 90		
$I_{B1}-I_{B2}$	Input Offset Current for Matched Pair Q1 and Q2	$I_{C1} = 1_{C2} = 1$ mA, $V_{CE} = 5V$		0.3	2	μA
V_{BE}	Base to Emitter Voltage	$I_C = 1$ mA, $V_{CE} = 3V$	0.63	0.73	0.83	V
$V_{BE1}-V_{BE2}$	Magnitude of Input Offset Voltage for Differential Pair	$V_{CE} = 5V$, $I_E = 1$ mA		0.48	5	mV
$\Delta V_{BE}/\Delta T$	Temperature Coefficient of Base to Emitter Voltage	$V_{CE} = 5V$, $I_E = 1$ mA		−1.9		mV/°C
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		0.33		V
$\Delta V_{10}/\Delta T$	Temperature Coefficient of Input Offset Voltage	$I_C = 1$ mA, $V_{CE} = 5V$		1.1		μV/°C

Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

Note 3: See curve.

AC Electrical Characteristics

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
NF	Low Frequency Noise Figure	f = 1 kHz, V_{CE} = 5V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
f_T	Gain Bandwidth Product	V_{CE} = 5V, I_C = 3 mA	300	500		MHz
C_{EB}	Emitter to Base Capacitance	V_{EB} = 5V, I_E = 0		0.70		pF
C_{CB}	Collector to Base Capacitance	V_{CB} = 5V, I_C = 0		0.37		pF
C_{CI}	Collector to Substrate Capacitance	V_{CI} = 5V, I_C = 0		2.2		pF
Low Frequency, Small Signal Equivalent Circuit Characteristics						
h_{fe}	Forward Current Transfer Ratio	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		100		
h_{ie}	Short Circuit Input Impedance	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		3.5		kΩ
h_{oe}	Open Circuit Output Impedance	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		15.6		μmho
h_{re}	Open Circuit Reverse Voltage Transfer Ratio	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		1.8×10^{-4}		
Admittance Characteristics						
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		mmho
Y_{ie}	Input Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.3 + j 0.04		mmho
Y_{oe}	Output Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.001 + j 0.03		mmho
Y_{re}	Reverse Transfer Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		(Note 3)		mmho

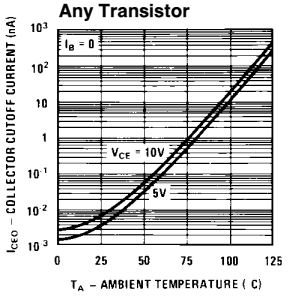
Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

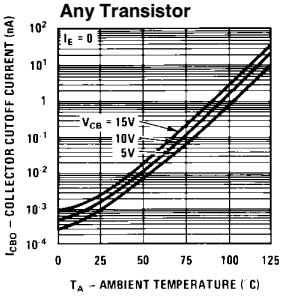
Note 3: See curve.

Typical Performance Characteristics

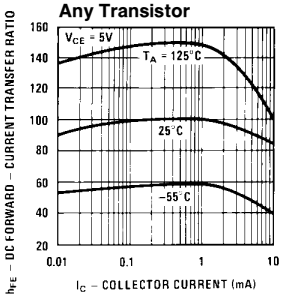
I_{CEO} vs T_A for Any Transistor



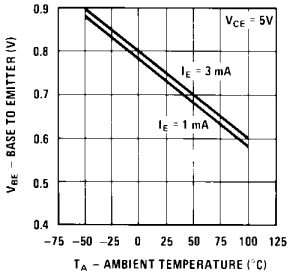
I_{CBO} vs T_A for Any Transistor



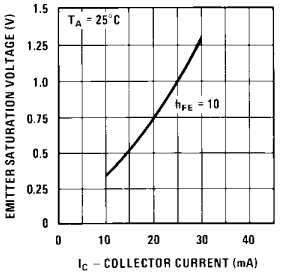
h_{FE} vs I_C for Any Transistor



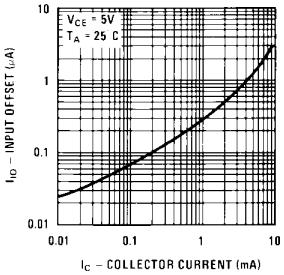
V_{BE} vs T_A for Any Transistor



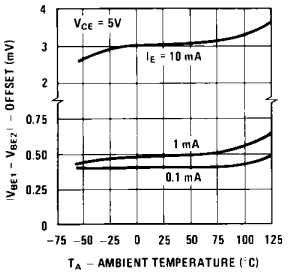
$V_{CE(SAT)}$ vs I_C for Any Transistor



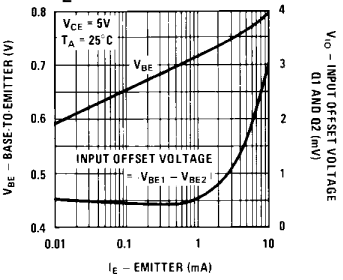
I_{IO} vs I_C (Q1 and Q2)



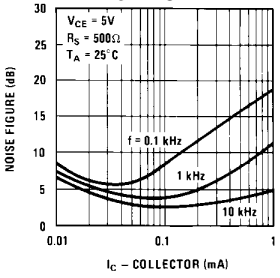
V_{IO} vs T_A for Q1 and Q2



V_{BE} and V_{IO} vs I_E for Q1 and Q2



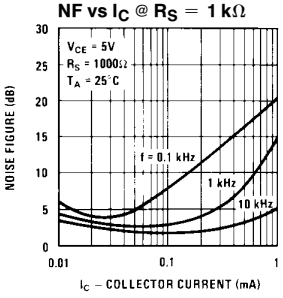
NF vs I_C @ R_S = 500Ω



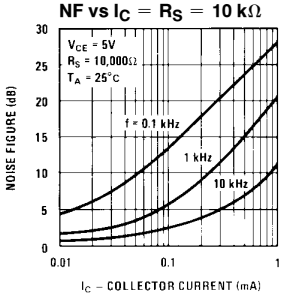
TL/H/7959–2

Typical Performance Characteristics (Continued)

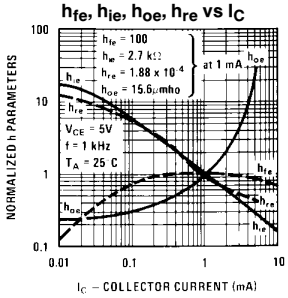
NF vs I_C @ R_S = 1 kΩ



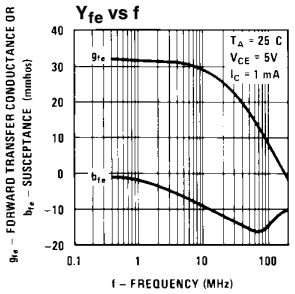
NF vs I_C = R_S = 10 kΩ



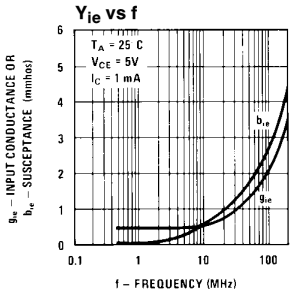
h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C



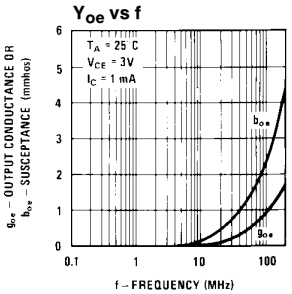
Y_{fe} vs f



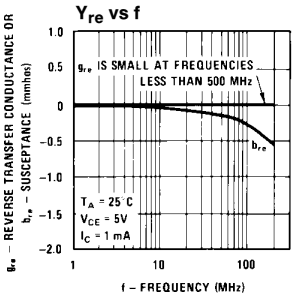
Y_{ie} vs f



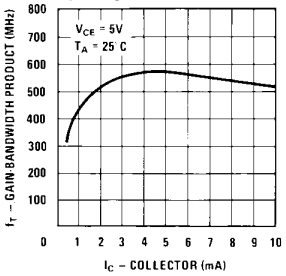
Y_{oe} vs f



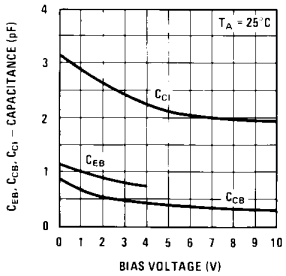
Y_{re} vs f



f_T vs I_C

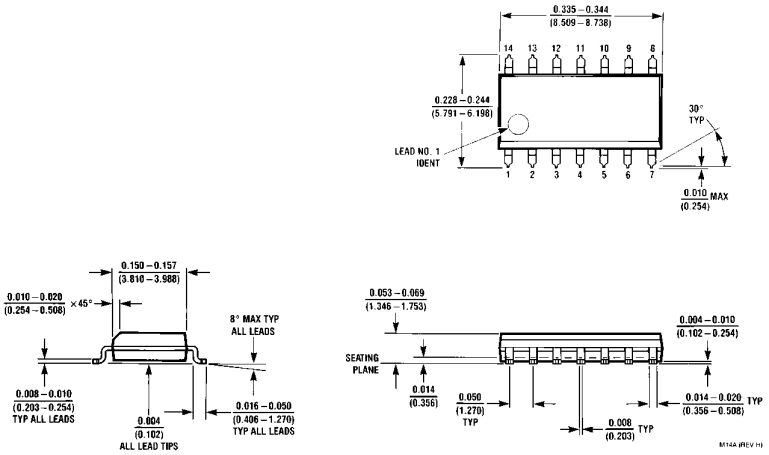


C_{EB}, C_{CB}, C_{CI} vs Bias Voltage

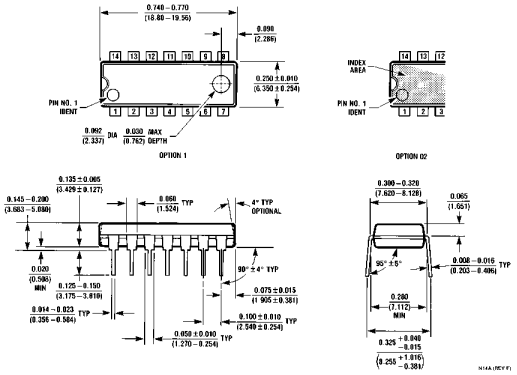


TL/H/7959–3

Physical Dimensions inches (millimeters)



SO Package (M)
Order Number LM3146M
NS Package Number M14A



Molded Dual-In-Line Package (N)
Order Number LM3146N
NS Package Number N14A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.