

SANYO	No.1434G	N MOS LSI
	LM7000, 7000N	
Direct PLL Frequency Synthesizer for Electronic Tuning		

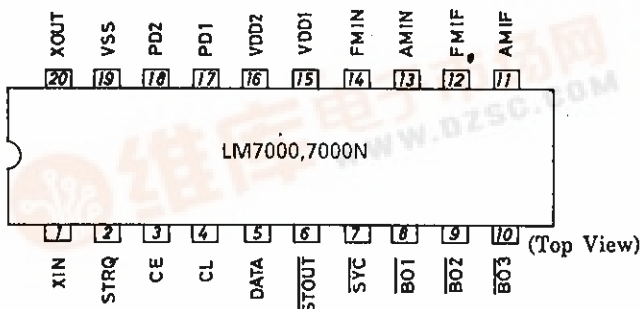
Features

- The LM7000N is a modified version of the LM7000 whose phase comparator dead zone is changed.
- High-speed programmable divider capable of direct dividing FM band VCO frequency.
- Reference frequency (7 kinds) : 100,50,25,10,9,5,1kHz
- Output for band select (3 bits)
- Clock output for controller (400kHz)
- Time base output for clock (8Hz)
- Data input : Serial input (CE,CL,DATA pins)
- On-chip IF count circuit : FM : ±10kHz
MW, SW : ±3kHz
LW : ±0.6kHz

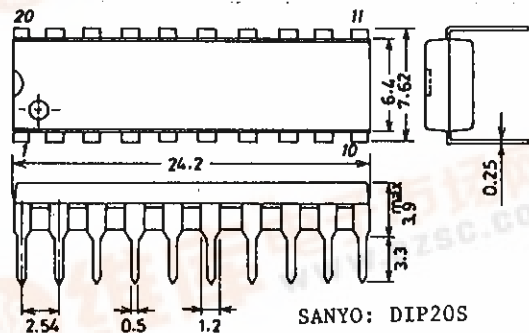
Absolute Maximum Ratings at Ta=25°C, VSS=0V

				unit
Maximum Supply Voltage	V _{DD} max	V _{DD1} , V _{DD2}	-0.3 to +7.0	V
Maximum Input Voltage	V _{IN1} max	CE, CL, DATA, STRQ	-0.3 to +7.0	V
	V _{IN2} max	Input pins other than V _{IN1}	-0.3 to V _{DD} +0.3	V
Maximum Output Voltage	V _{OUT1} max	SYC, STOUT	-0.3 to +7.0	V
	V _{OUT2} max	BO1, BO2, BO3	-0.3 to +13	V
	V _{OUT3} max	Output pins other than V _{OUT1,2}	-0.3 to V _{DD} +0.3	V
Allowable Power Dissipation	Pd max	Ta=85°C	300	mW
Operating Temperature	Topr		-40 to +85	°C
Storage Temperature	Tstg		-55 to +125	°C

Pin Assignment



Package Dimensions 3021B
(unit : mm)



LM7000,7000N

Allowable Operating Conditions at $T_a = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{V}$

				unit
Supply Voltage	V_{DD1}	V_{DD1} , PLL operation	4.5 to 6.5	V
	V_{DD2}	V_{DD2} , Xtal OSC time base	3.5 to 6.5	V
Input 'H'-Level Voltage	V_{IH}	CE, CL, DATA, STRQ	2.2 to 6.5	V
Input 'L'-Level Voltage	V_{IL}	CE, CL, DATA, STRQ	0 to 0.7	V
Output Voltage	V_{OUT1}	<u>SYC</u> , <u>STOUT</u>	0 to 6.5	V
	V_{OUT2}	<u>BO1</u> , <u>BO2</u> , <u>BO3</u>	0 to 13	V
Output Current	I_{OUT}	<u>BO1</u> , <u>BO2</u> , <u>BO3</u> , $V_{DD} = 4.5$ to 6.5V	0 to 3.0	mA
Input Frequency	$fin1$	XIN, sine wave, capacitive coupling	1.0 to 7.2typ to 8.0	MHz
	$fin2$	FMIN, " (Note 1), *(S=1)	45 to 130	MHz
	$fin3$	FMIN, " (Note 2), *(S=1)	5 to 30	MHz
	$fin4$	AMIN, " *(S=0)	0.5 to 10	MHz
	$fin5$	FMIF, "	10.0 to 10.7typ to 11.5	MHz
	$fin6$	AMIF, "	400 to 450typ to 500	kHz
Oscillation-Guaranteed Crystal Resonator	Xtal	XIN-XOUT, $C_1 \leq 30\Omega$	5.0 to 7.2typ to 8.0	MHz
Input Amplitude	V_{in1}	XIN, sine wave, capacitive coupling	0.5 to 1.5	Vrms
	V_{in2}	FMIN, "	0.1 to 1.5	Vrms
	V_{in3}	AMIN, "	0.1 to 1.5	Vrms
	V_{in4}	FMIF, "	0.1 to 1.5	Vrms
	V_{in5}	AMIF, "	0.1 to 1.5	Vrms

* : 'S' : Control bit in serial data

(Note 1) : $f_{ref} = 100, 50, 25\text{kHz}$ (Note 2) : Reference frequency other than $f_{ref} =$ (Note 1)

Electrical Characteristics / Under allowable operating conditions

			min	typ	max	unit
On-chip Feedback Resistance	R_{f1}	XIN		1.0		$M\Omega$
	R_{f2}	FMIN		0.5		$M\Omega$
	R_{f3}	AMIN		0.5		$M\Omega$
	R_{f4}	FMIF		0.5		$M\Omega$
	R_{f5}	AMIF		0.5		$M\Omega$
Input 'H'-Level Current	I_{IH}	CE, CL, DATA, STRQ			5.0	μA
Input 'L'-Level Current	I_{IL}	CE, CL, DATA, STRQ			5.0	μA
Output 'L'-Level Voltage	V_{OL1}	FMIF, AMIF, FMIN, AMIN			3.5	V
	V_{OL2}	<u>SYC</u>		0.02	0.3	V
Output Off Leak Current	I_{off1}	<u>SYC</u>			5.0	μA
Output 'L'-Level Voltage	V_{OL3}	<u>STOUT</u>			1.0	V
Output Off Leak Current	I_{off2}	<u>STOUT</u>			5.0	μA
Output 'L'-Level Voltage	V_{OL4}	<u>BO1</u> to <u>3</u>			1.0	V
Output Off Leak Current	I_{off3}	<u>BO1</u> to <u>3</u>			3.0	μA
Output 'H'-Level Voltage	V_{OH1}	PD1,2			$0.5V_{DD}$	V
Output 'L'-Level Voltage	V_{OL5}	PD1,2			0.3	V
'H'-Level Tri-state Off Leak Current	I_{offH}	PD1,2		0.01	10.0	nA
'L'-Level Tri-state Off Leak Current	I_{offL}	PD1,2		0.01	10.0	nA
Supply Voltage	I_{DD1}	$V_{DD1} + V_{DD2}$		25	40	mA
	I_{DD2}	V_{DD2}		2.0	3.5	mA
Input Capacitance	c_{in}	FMIN	1	2	3	pF

(Note 3) $V_{DD} = 3.5$ to 6.5V

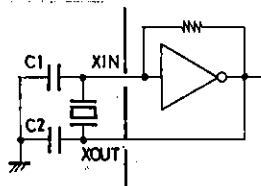
(Note 4) 7.2MHz Xtal connected across XIN and XOUT

$fin2 = 130\text{MHz}$

$V_{IN2} = 100\text{mVrms}$

Other input pins = V_{SS}

Output pins = Open



Kinseki Co., Ltd

HC43/U: 2114-84521 (1) : $CL = 10\text{pF}$ $C1 = 15$ (10 to 22)pF $C2 = 15\text{pF}$

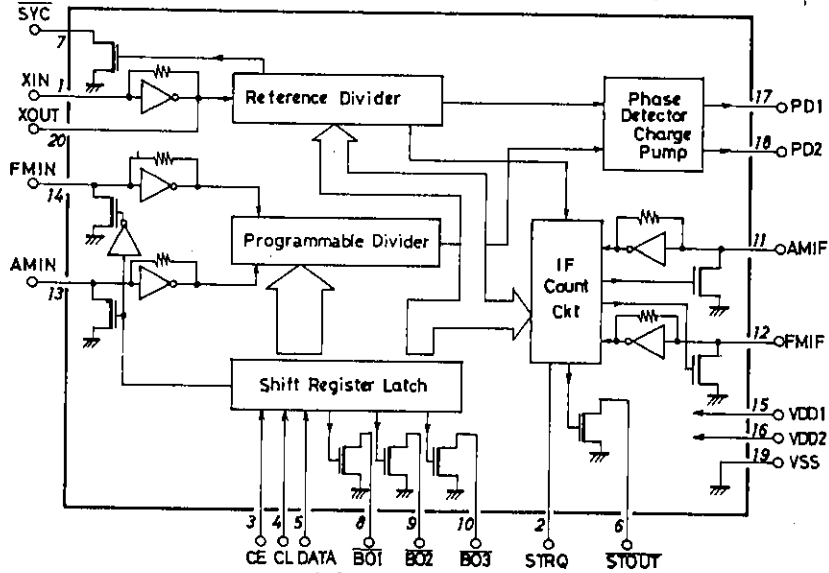
HC43/U: 2114-84521 (2) : $CL = 16\text{pF}$ $C1 = 22$ (15 to 33)pF $C2 = 33\text{pF}$

Nihon Denpa Kogyo Co., Ltd

NR-18: LM-X-0701 : $CL = 10\text{pF}$ $C1 = 15\text{pF}$ $C2 = 15\text{pF}$

LM7000, 7000N

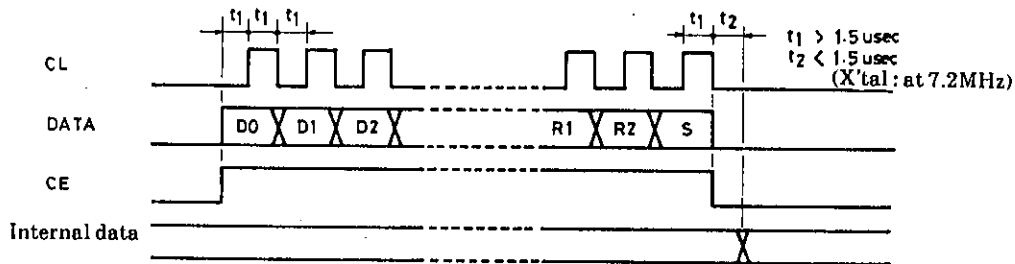
Equivalent Circuit Block Diagram



Pin Description

- SYC** : Controller clock (400kHz)
- XIN, XOUT** : Xtal OSC (7.2MHz), on-chip feedback resistor
- FMIN, AMIN** : Local oscillation signal input
- CE, CL, DATA** : Data input
- BO1, BO2, BO3** : Band data output, $\overline{BO1}$ can be also used for time base output (8Hz)
- STRQ** : IF' count request input
- STOUT** : Auto search stop signal output
- VDD1, VDD2, VSS** : Power supply (V_{DD2} is for backup)
- AMIF, FMIF** : IF signal input
- PD1, PD2** : Charge pump output

Data Input



← Inputting starts at D0.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	T0	T1	B0	B1	B2	TB	R0	R1	R2	S
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(1) D0 (LSB) to D13 (MSB) : Division ratio data

For FMIN, use D0 to D13 ; for AMIN, use D4 to D13.

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
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	1	1	1	1	0	1	1	1	1	1	0	0	0	0															
LSB					1	0	0	0	1	0	0	1	0	0	MSB	→	FMIN division ratio = 1007												
	X	X	X	X											MSB	→	AMIN division ratio = 145												

LM7000,7000N

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Example

① FM 100kHz Step ($f_{ref}=100\text{kHz}$)

FM VCO = 100.7MHz (FM RF = 90.0MHz, IF = + 10.7MHz)

Division Ratio = 100.7MHz (FM VCO) \div 100kHz(f_{ref}) = 1007 \rightarrow 3EF_(HEX)

② AM 10kHz Step ($f_{ref}=10\text{kHz}$)

AM VCO = 1450kHz (AM RF = 1000kHz, IF = + 450kHz)

Division Ratio = 1450kHz (AM VCO) \div 10kHz (f_{ref}) = 145 \rightarrow 91_(HEX)

(2) T0, T1 : For LSI test (0, 0)

(3) B0 to B2, TB : Band data
: Time base data

Input				Output		
B0	B1	B2	TB	BO1	BO2	BO3
0	0	0	0	*	*	*
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	0	1	1	1
0	0	0	1	TB	*	*
×	1	0	1	TB	1	0
×	0	1	1	TB	0	1
×	1	1	1	TB	1	1
1	0	0	1	TB	0	0

* : Determined by R0 to R2

× : Don't care

TB : 8Hz

(4) R0 to R2 : Reference frequency data

R0	R1	R2	fref	BO1	BO2	BO3	IF Count
0	0	0	100 kHz	1	1	0	10.7MHz \pm 10kHz
0	0	1	50	1	1	0	
0	1	0	25	1	1	0	
0	1	1	5	0	0	1	450kHz \pm 3 kHz
1	0	0	10	1	0	1	
1	0	1	9	1	0	1	
1	1	0	1	0	1	1	450kHz \pm 0.6kHz
1	1	1	5	0	0	1	450kHz \pm 3 kHz

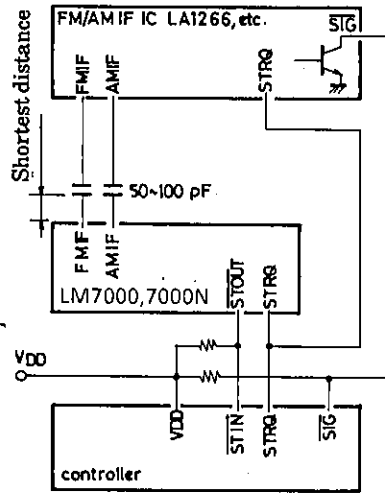
(Note) B0 to B2 = 0

(5) S : Divider select data

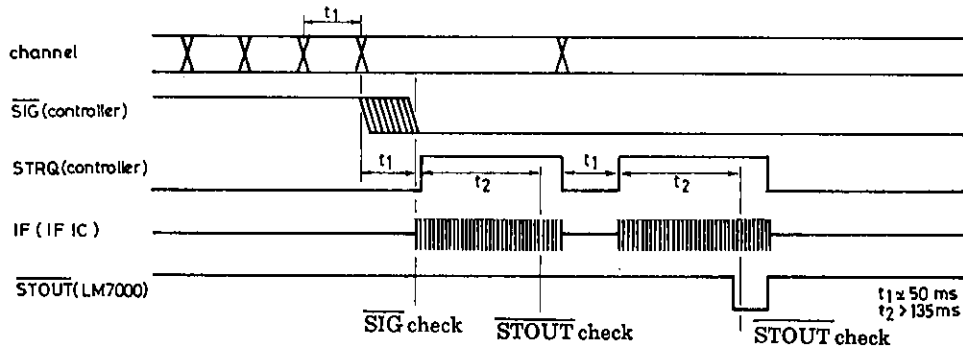
'1' : FMIN, '0' : AMIN

LM7000,7000N

IF Count Circuit : Circuit to stop auto tuning

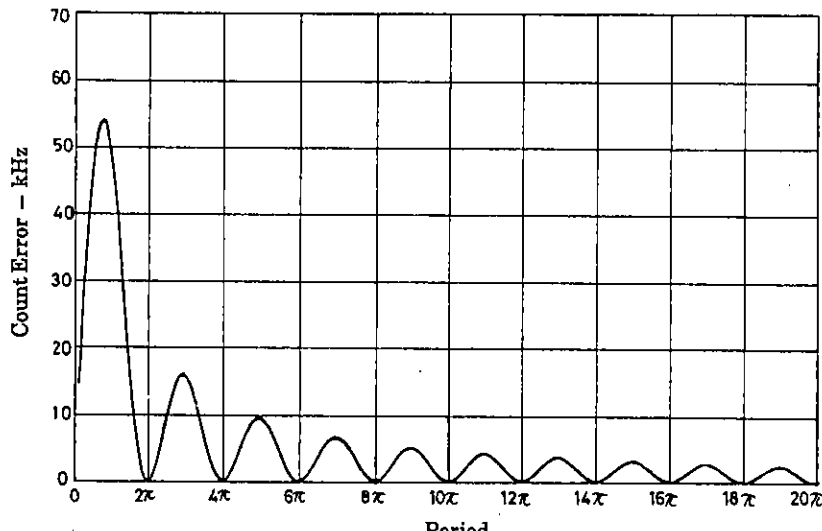


- When in the neighborhood of a broadcasting station, "SIG" signal is output, setting SIG of the controller to "0".
- "STRQ" signal is applied to the LM7000 and IF IC from the controller.
- IF signal is applied to the LM7000 from the IF IC and the LM7000 counts this signal.
- When a specified count value is reached, "STOUT" signal is applied to the controller from the LM7000, stopping auto tuning.



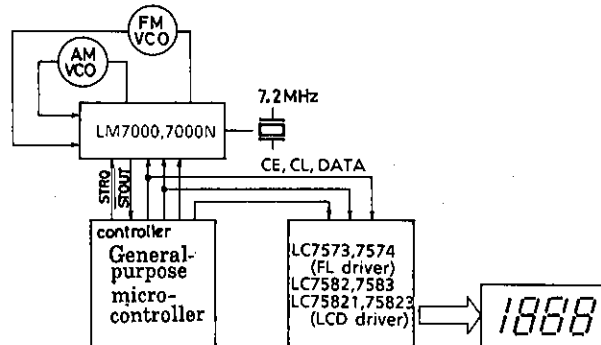
- Counting is performed only at "STRQ" = 1.
- The count time is 120msec.
- For FM, the count error is shown below.
(Example : For 50Hz-100% modulation, the maximum count error is 5kHz.)

Count Error - Period



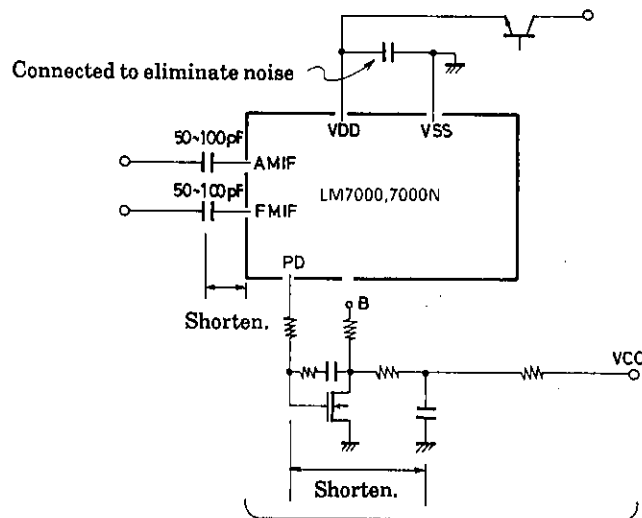
LM7000,7000N

Sample Connection to Controller



Notes for Using PLL IC

- (1) The layout nearby PLL-IC.



Surround this section with the ground pattern, because it is in a high impedance state and is very susceptible to noise.

- (2) State of output ports ($\overline{BO1}$ to $\overline{BO3}$) at power-on.

The output ports are undefined until the control data is transmitted.

The $\overline{BO1}$ and $\overline{BO3}$ ports may output an internal clock of PLL-IC, and so don't forget to transmit control data after power-on.

The control data should be input only after X'tal OSC have become stable.

- (3) VCO design.

At design of the VCO, try to do not stop oscillation no matter what Tuning Voltage (V_{tune}) is 0 Volt. When the VCO oscillation stops, the PLL is possible to become a dead-lock condition.

Differences Between the LM7000 and LM7000N

The only difference between LM7000 and LM7000N is the phase detector dead zone. Otherwise, they are identical.

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LM7000,7000N

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Dead Zone

The phase detector shown in figure 1 compares the reference frequency (f_r) with f_p . The characteristics of the phase detector are shown in figure 2. A phase detector ideally should output a voltage proportional to the phase difference (ϕ) as shown by curve (A), but in reality, delays in the internal circuitry mean that small phase differences cannot be detected. This causes the dead zone shown by curve (B). To realize a large signal-to-noise ratio, this dead zone should be made as small as possible.

Standard models, however, can have a rather wide dead zone. When there is a strong RF input signal, with these models, the VCO can be modulated to compensate for part of the RF signal being leak to the VCO from the MIX. In the case of dead zone is small, the VCO output is modulated and a beat between the RF and VCO is created.

Figure 1

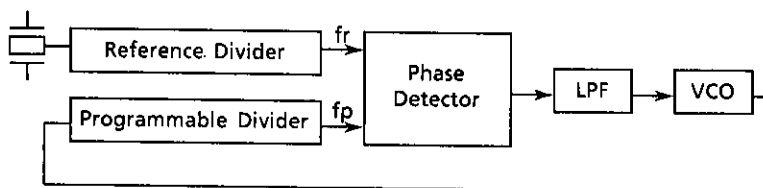
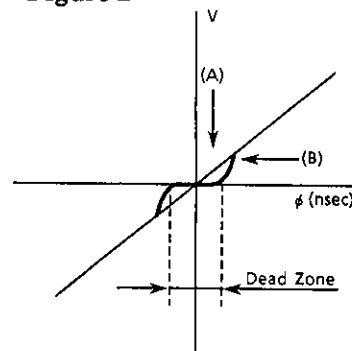


Figure 2



LM7000/LM7000N

Because of the above reasons, the LM7000 and LM7000N were developed with different dead zones.

LM7000 : Dead zone \approx 0 ns, S/N is 90 to 100 dB or greater

LM7000N : Dead zone \approx 5 to 10 ns, for standard models

Note

If the LM7000N is used in a circuit designed for the LM7000, the S/N ratio will decrease.

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