

Ordering number: EN3035A

SANYO	No.3035A	NMOS LSI
		LM7006, 7006H
Dual PLL Frequency Synthesizer Circuit		

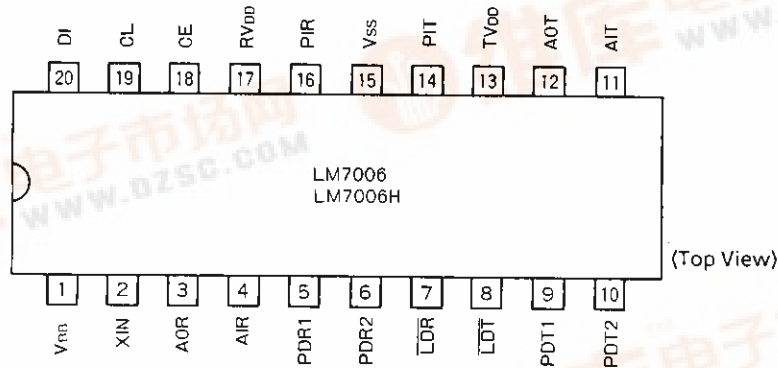
Overview

The LM7006, 7006H is a PLL Frequency Synthesizer circuit for use in cordless telephones. It incorporates separate programmable dividers, phase comparators and dual-gain charge pumps for the transmit and receive sides. (Transmit side is operated by an independent power supply for standby function.)

Device operation is controlled by a 40-bit serial input word, enabling simple control from a microcontroller by CCB.

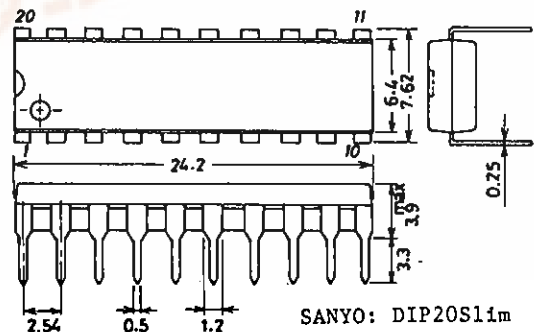
The LM7006, 7006H is available in a 20-pin plastic DIP (300MIL). It operates from a single 4.0 to 5.5V supply.

Pin Assignment : DIP20S



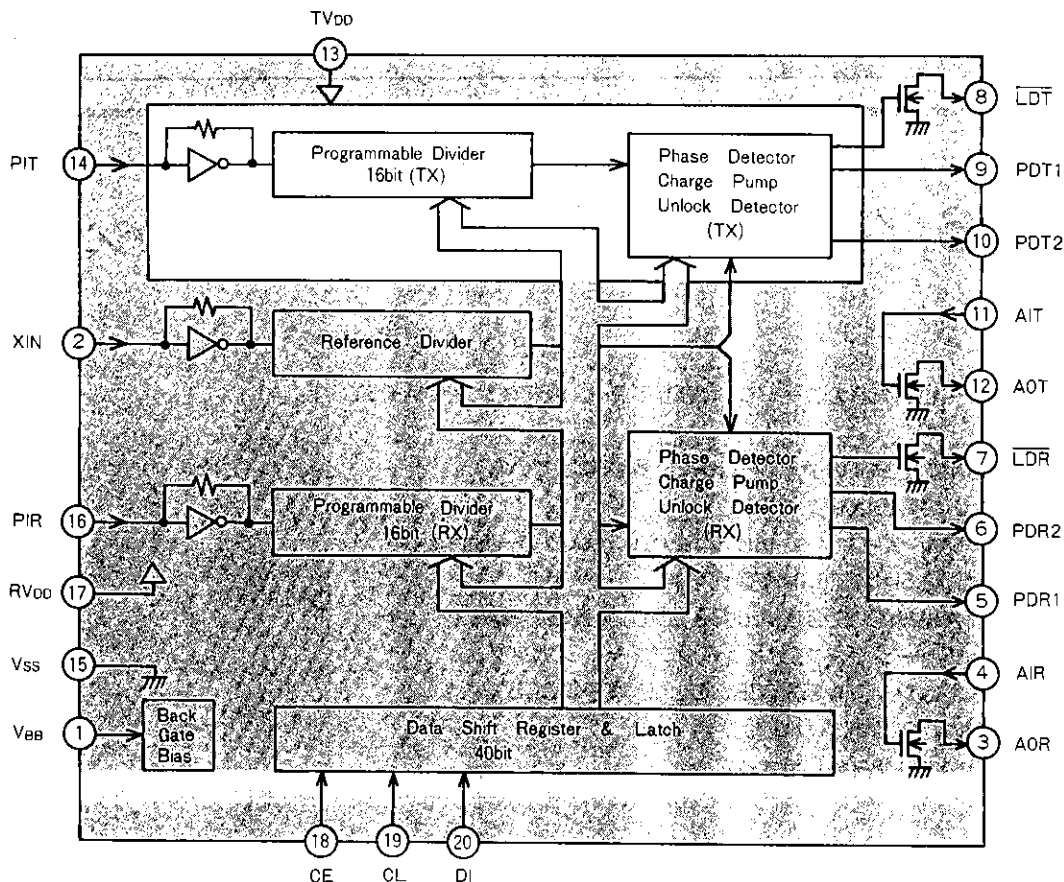
Package Dimensions 3021B-D20SIC

(unit : mm)



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Equivalent Circuit Block Diagram



PIT	: TX local OSC signal input	LDT	: TX unlock detection (open-drain)
XIN	: Reference OSC signal input (12.800MHz)	PDT1	: TX Charge pump output (main)
PIR	: RX local OSC signal input	PDT2	: TX Charge pump output (sub)
RV _{DD}	: Power supply other than TV _{DD}	AIT, AOT	: TX Tr for L.P.F amp
V _{SS}	: Ground	LDR	: RX unlock detection (open-drain)
V _{BB}	: Back gate bias pin	PDR1	: RX Charge pump output (main)
CE, CL, DI	: Serial data input	PDR2	: RX Charge pump output (sub)
TV _{DD}	: TX PLL supply (: <input type="checkbox"/>)	AIR, AOR	: RX Tr for L.P.F amp

Absolute Maximum Ratings at Ta = 25°C, V _{SS} = 0V				unit
Supply Voltage	V _{DD} max	RV _{DD} , TV _{DD}	-0.3 to +6.0	V
Back Gate Bias	V _{BB} max	V _{BB}	-4.0 to -2.0	V
Input Voltage	V _{IN(1)} max	CE, CL, DI, AIR, AIT	-0.3 to +7.0	V
	V _{IN(2)} max	All other input pins	-0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT(1)} max	AOR, AOT, LDR, LDT	-0.3 to +7.0	V
	V _{OUT(2)} max	All other output pins	-0.3 to V _{DD} + 0.3	V
Output Current	I _{OUT(1)} max	AOR, AOT, LDR, LDT	0 to 2.0	mA
Allowable Power Dissipation	Pd max	Ta ≤ 75°C	350	mW
Operating Temperature	T _{opr}		-40 to +75	°C
Storage Temperature	T _{stg}		-55 to +125	°C

Note : Pins PIR and PIT are susceptible to damage by static discharge. Appropriate precautions should be taken during handling and operation.

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Allowable Operating Conditions at $T_a = -40$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{V}$				min	typ	max	unit
Supply Voltage	V_{DD}	$R_{V_{DD}}, TV_{DD}$		4.0		5.5	V
Input 'H'-Level Voltage	V_{IH}	CE, CL, DI		2.5		5.5	V
Input 'L'-Level Voltage	V_{IL}	CE, CL, DI		0		0.5	V
Output Voltage	V_{OUT}	AOR, AOT, $\overline{\text{LDR}}, \overline{\text{LDT}}$		0		5.5	V
Input Frequency	$f_{IN(1)}$	XIN	Sine wave, capacitive coupling $V_{IN(1)} = 50\text{mVrms}$	3.0	12.8	13.5	MHz
	$f_{IN(2)}$	PIR, PIT	Sine wave, capacitive coupling $V_{IN(2)} = 70\text{mVrms}$	200		400	MHz
Input Voltage	$V_{IN(1)}$	XIN	Sine wave, capacitive coupling $f_{IN(1)} = 3.0$ to 13.5MHz	50		1000	mVrms
	$V_{IN(2)}$	PIR, PIT	Sine wave, capacitive coupling $f_{IN(2)} = 200$ to 400MHz	70		500	mVrms
Electrical Characteristics under Allowable Operating Conditions				min	typ	max	unit
Internal Feedback Resistor	R_f	XIN, PIR, PIT			500		k Ω
Hysteresis Width	V_h	CE, CL, DI		0.1	0.5		V
Input 'H'-Level Current	$I_{IH(1)}$	CE, CL, DI	$V_1 = 5.5\text{V}$			5.0	μA
	$I_{IH(2)}$	XIN, PIR, PIT	$V_1 = V_{DD}$			40	μA
	$I_{IH(3)}$	AIR, AIT	$V_1 = 5.5\text{V}$		0.01	10.0	nA
Input 'L'-Level Current	$I_{IL(1)}$	CE, CL, DI	$V_1 = V_{SS}$			5.0	μA
	$I_{IL(2)}$	XIN, PIR, PIT	$V_1 = V_{SS}$			40	μA
	$I_{IL(3)}$	AIR, AIT	$V_1 = V_{SS}$		0.01	10.0	nA
Output 'H'-Level Voltage	V_{OH}	PDR1, PDR2 PDT1, PDT2	$I_O = 0.1\text{mA}$	$0.6V_{DD}$			V
Output 'L'-Level Voltage	$V_{OL(1)}$	PDR1, PDR2 PDT1, PDT2	$I_O = 0.1\text{mA}$			0.3	V
	$V_{OL(2)}$	$\overline{\text{LDR}}, \overline{\text{LDT}}$	$I_O = 1.0\text{mA}$			1.0	V
	$V_{OL(3)}$	AOR, AOT	$I_O = 0.5\text{mA}$ $\text{AIR/AIT} = 1.2\text{V}$			0.5	V
Output OFF-State Leakage Current	$I_{OFF(1)}$	$\overline{\text{LDR}}, \overline{\text{LDT}}$	$V_O = 5.5\text{V}$			5.0	μA
	$I_{OFF(2)}$	AOR, AOT	$V_O = 5.5\text{V}$			1.0	μA
	$I_{OFF(3)}$	PDR1, PDR2 PDT1, PDT2	$V_O = 0.3\text{V}, V_O = 5.5\text{V}$		0.01	10.0	nA
Input Capacitance	C_{IN}	XIN, PIR, PIT			2.5		pF
Supply Current	$I_{DD(1)}$	$R_{V_{DD}}$	*1		23	32	mA
	$I_{DD(2)}$	$R_{V_{DD}} + TV_{DD}$	*2		45	62	mA
LM7006 and LM7006H Difference				min	typ	max	unit
LM7006	I_{DD}	$R_{V_{DD}} + TV_{DD}$	*2, $T_a = 25^\circ\text{C}$			50	mA
LM7006H	I_{DD}	$R_{V_{DD}} + TV_{DD}$	*2, $T_a = 25^\circ\text{C}$	50		55	mA

*1 XIN = 12.8MHz,
PIR = 400MHz (70mVrms),
other inputs : V_{SS} ,
outputs : open

*2 XIN = 12.8MHz,
PIR = 400MHz (70mVrms),
PIT = 400MHz (70mVrms),
other inputs : V_{SS} ,
outputs : open

Note : The LM7006H is distinguished by an orange marking. I_{DD} is the only difference between the two devices.

LM7006, 7006H

Pin Description

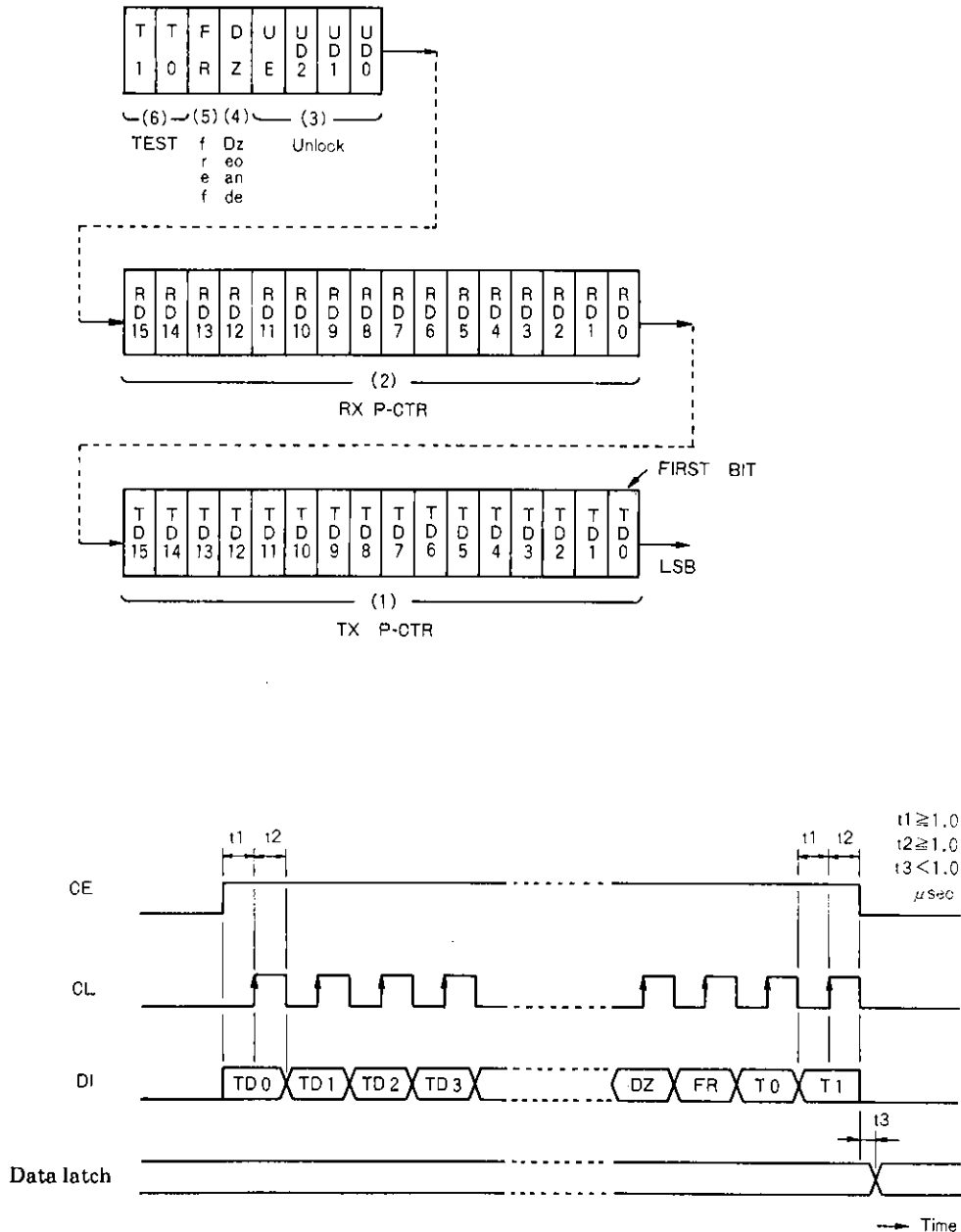
Pin Name	Pin No.	Input/Output	Description
XIN	2	Input	Reference OSC input 12.800MHz, 50mVrms minimum (TCX0)
PIT	14	Input	Transmit VCO input 200 to 400MHz, 70mVrms minimum. Division ratio of transmit programmable divider is set by the TD0 to TD15 control bits to between 256 and 65535.
PIR	16	Input	Receive VCO input 200 to 400MHz, 70mVrms minimum. Division ratio of receive programmable divider is set by the RD0 to RD15 control bits to between 256 and 65535.
RVDD	17	—	Receive section power supply 4.0 to 5.5V to data shift register latch, reference divider, RX programmable divider, RX phase detector, RX unlock detector.
TVDD	13	— ※1	Transmit section power supply 4.0 to 5.5V to TX programmable divider, TX phase detector, TX unlock detector.
VBB	1	Output	Back gate bias pin Requires a 0.01μF capacitor between VBB and ground.
VSS	15	—	Ground
LDT LDR	8 7	Output [N-channel Open drain]	N-channel open-drain lock/unlock outputs for transmit and receive PLLs Lock : High-impedance Unlock : LOW The lock/unlock phase boundary is set by the UD0 to UD2 control bits. Extension of the phase difference signal is selected by the UE control flag.
PDT1 PDR1	9 5	Output (Tri-state)	Tri-state main charge pump outputs for transmit and receive PLLs Driven by the phase error signal obtained by comparing PLL frequency divided by N (f_{osc}/N) with the reference frequency (f_{ref}) $f_{osc}/N > f_{ref}$ or leading: positive pulses $f_{osc}/N < f_{ref}$ or lagging: negative pulses $f_{osc}/N = f_{ref}$: high-impedance
PDT2 PDR2	10 6	Output (Tri-state)	Tri-state auxiliary charge pump outputs for transmit and receive PLLs Driven by the PLLs phase error outputs only while PLL is out of lock, and high-impedance while PLL is in the lock range set by UD0 to UD2. Same polarity as main charge pump outputs.
AIT AOR	11 12	Input Output	MOS N-channel transistor for TX PLL loop filter
AIR AOR	4 3	Input Output	MOS N-channel transistor for RX PLL loop filter
CE	18	Input ※2	Chip enable input A HIGH level enables serial data transfer into the LM7006.
CL	19	Input ※2	Serial input data clock
DI	20	Input ※2	Serial data input

※1 TVDD Pin is connected to VSS when transmit circuit is in power-off state (standby mode).
For instance, connect resistor (47kΩ to 100kΩ) between TVDD and VSS.

※2 High and Low input voltages on CE, CL, DI are held in the following range, respectively, regardless of the supply voltage (RVDD).
 $V_{IH} = 2.5$ to $5.5V$, $V_{IL} = 0$ to $0.5V$

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Device Control



※ As the state of output pins of the LM7006 is unsettled when power is applied to them, the data must be sent from microcontroller as soon as possible.

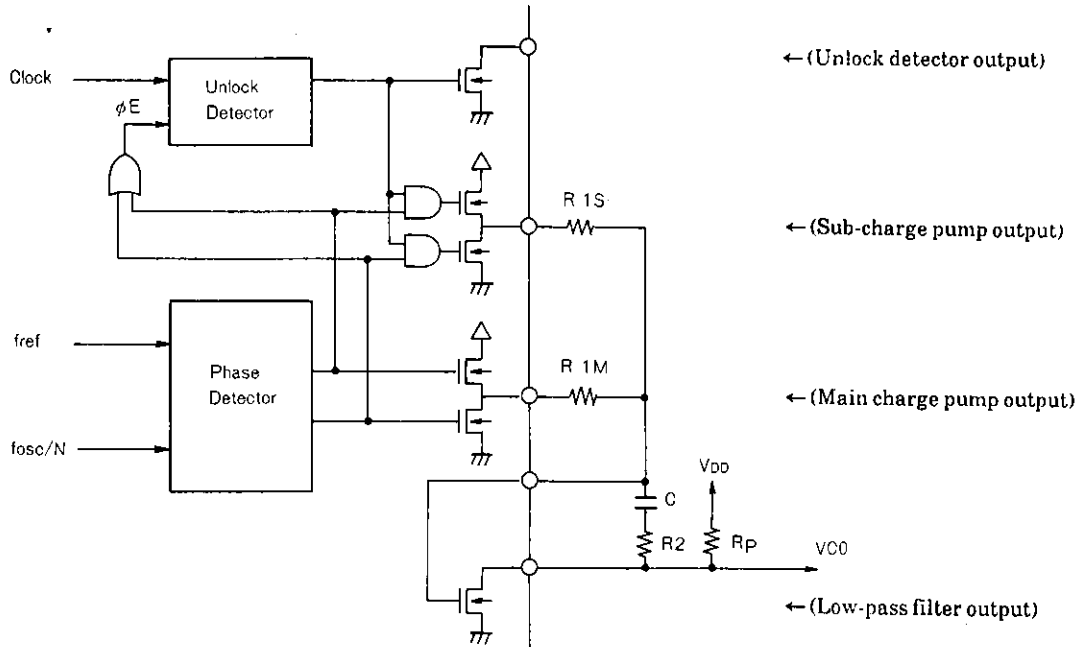
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No.	Data	Description	Associated data bits																																																								
(1)	TX Programmable Divider : TD0 to TD15	TD0 to TD15 form the TX side programmable divider ratio. TD0 is the least significant bit, and TD15 the most significant bit. The divider ratio must be between 256 and 65535, inclusive.	FR																																																								
(2)	RX Programmable Divider : RD0 to RD15	RD0 to RD15 form the RX side programmable divider ratio. RD0 is the least significant bit, and RD15 the most significant bit. The divider ratio must be between 256 and 65535, inclusive.	FR																																																								
(3)	UD0 UD1 UD2 Unlock Detector Control : UE	<p>UD0 to UD2 set the lock detector phase difference lock/unlock limit, as shown in the table below.</p> <table border="1"> <thead> <tr> <th>UD2</th> <th>UD1</th> <th>UD0</th> <th>Signal Name</th> <th>Phase Difference (ϕE) Detection Width (μsec)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>ULD0</td> <td>$\phi E > 0$</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>ULD1</td> <td>$\phi E > 1.25$</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>ULD2</td> <td>$\phi E > 0.30$</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>ULD3</td> <td>$\phi E > 5.00$</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>ULD4</td> <td>$\phi E > 0.15$</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>ULD5</td> <td>$\phi E > 2.50$</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>ULD6</td> <td>$\phi E > 0.60$</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>ULD7</td> <td>$\phi E > 10.00$</td> </tr> </tbody> </table> <p>UE controls the format of the lock detector $\overline{\text{LDT}}$ and $\overline{\text{LDR}}$ output signals. The figure below illustrates this operation.</p> <table border="1"> <thead> <tr> <th>Signal Name</th> <th>UE</th> <th>$\overline{\text{LDT}}/\overline{\text{LDR}}$ Outputs</th> </tr> </thead> <tbody> <tr> <td>ULD0</td> <td>0/1</td> <td>Directly output the phase error signal</td> </tr> <tr> <td rowspan="2">ULD0 to ULD7</td> <td>0</td> <td>The phase error signal is extended by 2.5ms</td> </tr> <tr> <td>1</td> <td>The phase error signal is extended by 5.0ms</td> </tr> </tbody> </table>	UD2	UD1	UD0	Signal Name	Phase Difference (ϕE) Detection Width (μsec)	0	0	0	ULD0	$\phi E > 0$	0	0	1	ULD1	$\phi E > 1.25$	0	1	0	ULD2	$\phi E > 0.30$	0	1	1	ULD3	$\phi E > 5.00$	1	0	0	ULD4	$\phi E > 0.15$	1	0	1	ULD5	$\phi E > 2.50$	1	1	0	ULD6	$\phi E > 0.60$	1	1	1	ULD7	$\phi E > 10.00$	Signal Name	UE	$\overline{\text{LDT}}/\overline{\text{LDR}}$ Outputs	ULD0	0/1	Directly output the phase error signal	ULD0 to ULD7	0	The phase error signal is extended by 2.5ms	1	The phase error signal is extended by 5.0ms	
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(4)	Dead Zone Control : DZ	Selects the width of the phase comparator insensitive region. DZ = 0 : narrow DZ = 1 : wide																																																									
(5)	Reference frequency Select : FR	FR = 0 : reference frequency = 25.0kHz FR = 1 : reference frequency = 12.5kHz	TD0 to TD15 RD0 to RD15																																																								
(6)	Device Test Flags : T0,T1	T0 and T1 are used to test the LM7006. They should both be set to "0" for normal operation.																																																									

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Dual Charge Pump



The dual charge pump circuit ensures good performance during normal tracking and fast lock-in shown input frequency changes. During normal operation, only the main charge pump is employed to keep the PLL in sync. The auxiliary charge pump output is high-impedance. The loop filter time constant is relatively high, thus ensuring good sideband and modulation characteristics. When channels are changed, the PLL will lose lock and the auxiliary charge pump is activated. The filter resistor now consists of both R1S and R1M in parallel, reducing the filter time constant. PLL lock-in is thus accelerated.

Sample Application Circuit

