National Semiconductor

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LM9800
8-Bit Greyscale/24-Bit Color Linear CCD Sensor Processor

General Description

The LM9800 is a high performance integrated signal processor/digitizer for linear CCD image scanners. The LM9800 performs all the analog processing (correlated double sampling for black level and offset compensation, pixel-by-pixel gain adjust, and 8-bit analog-to-digital conversion) necessary to maximize the performance of a wide range of linear CCD sensors.

The LM9800 can be digitally programmed to work with a wide variety of CCDs from different manufacturers. An internal configuration register sets CCD and sampling timing to maximize performance, simplifying the design and manufacturing processes.

The LM9800 can be used with sequential or parallel output color CCDs. Coarse gain switching brings weak Blue signals up to Red/Green levels for best performance. For complementary voltage reference see the LM4041.

Applications

- Color and Greyscale Flatbed and Sheetfed Scanners
- General Purpose CCD Imaging

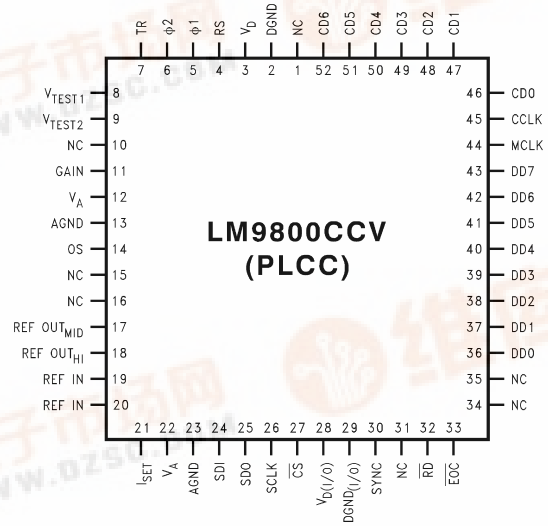
Features

- 2.5 million pixels/s conversion rate
- Implements Correlated Double Sampling for minimum noise and offset error
- Pixel-to-pixel gain correction for individual pixels maximizes dynamic range and resolution, even on "weak" pixels
- Reference and signal sampling points digitally controlled in 25ns increments for maximum performance
- Generates all necessary CCD clock signals
- Compatible with a wide range of linear CCDs
- TTL/CMOS input/output compatible

Key Specifications

■ Resolution	8 Bits
■ Pixel Conversion Rate	2.5MHz
■ Supply Voltage	+5V ±5%
■ Supply Voltage (Digital I/O)	+3.3V ±10% or +5V ±5%
■ Power Dissipation	210 mW (typ)

Connection Diagram



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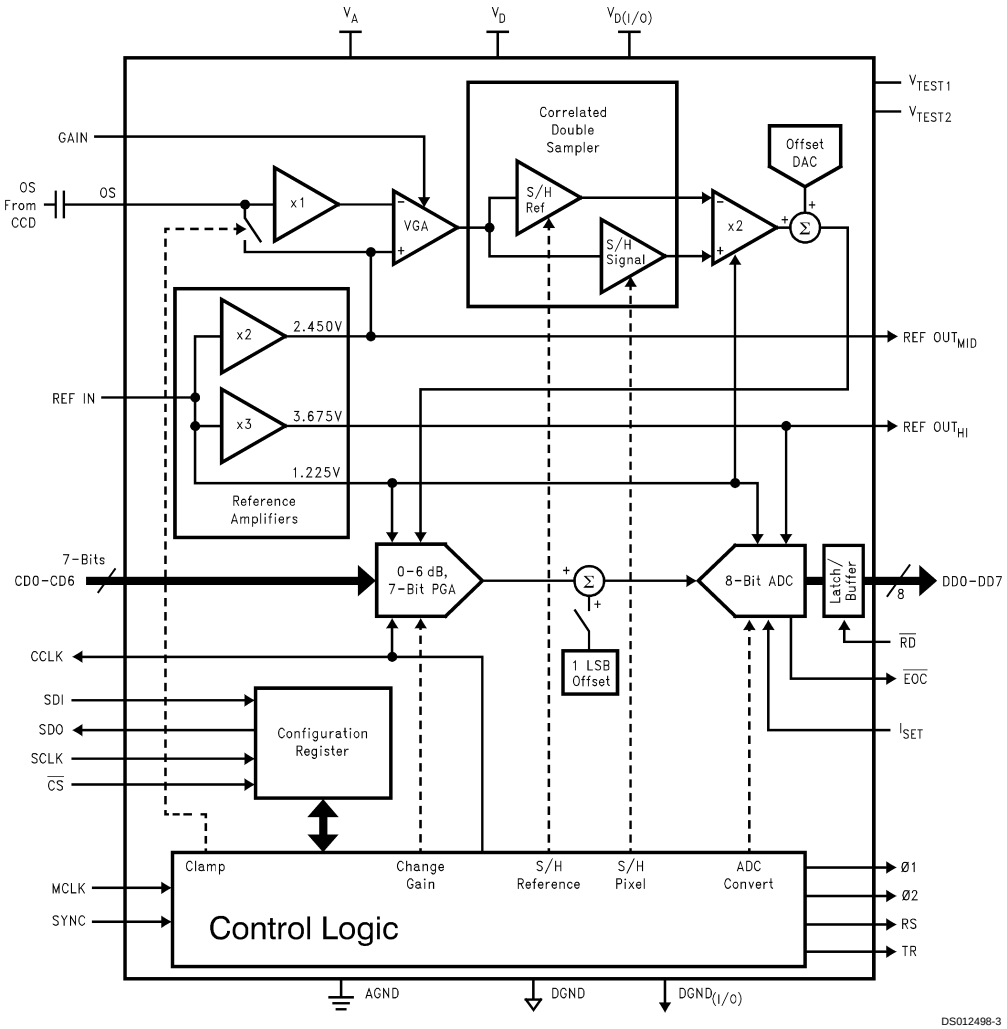
Block Diagram



Ordering Information

Commercial ($10^{\circ}C \leq T_A \leq +70^{\circ}C$)	Package
LM9800CCV	V52A 52 Pin Plastic Leaded Chip Carrier

Absolute Maximum Ratings (Notes 1, 2)

Positive Supply Voltage (V+ = V_A = V_D = $V_{D(I/O)}$)	
With Respect to GND = AGND = DGND = $DGND_{(I/O)}$	6.5V
Voltage On Any Input or Output Pin	0.3V to V^+ +0.3V
Input Current at any pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Package Dissipation at T_A = 25˚C (Note 4)	
ESD Susceptibility (Note 5)	
Human Body Model	3000V
Soldering Information	
Infrared, 10 seconds (Note 6)	300˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Note 1) (Note 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM9800CCV, LM9800CCVF	10˚C ≤ T_A ≤ +70˚C
V_A Supply Voltage	+4.75V to +5.25V
V_D Supply Voltage	+4.75V to +5.25V
$V_{D(I/O)}$ Supply Voltage	+2.7V to +5.25V
$\lvert V_A - V_D \rvert$	≤100 mW
$V_A - V_{D(I/O)}$	≥ −100 mV
OS, REF IN Voltage Range	−0.05V to V_A + 0.05V
CD0–CD6, MCLK, SYNC, SDI, SCLK, $\overline{CS}$, $\overline{RD}$ Voltage Range	−0.05V to $V_{D(I/O)}$ + 0.05V

Electrical Characteristics

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, V_A = V_D = +5.0V_{DC}, $V_{D(I/O)}$ = +5.0V or +3.0V_{DC}, REF IN = +1.225V_{DC}, f_{MCLK} = 20MHz, R_s = 25Ω. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25˚C (Note 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CCD Source Requirements for Full Specified Accuracy and Dynamic Range (Note 12)					
V_{WHITE}	Maximum Peak CCD Differential Signal Range	VGA Bypassed		**1.1**	V (min)
		VGA On (V_{GAIN} = 2.0V)		**0.5**	V (min)
	Correctable Range of CCD Pixel-to-Pixel V_{WHITE} Variation			**6**	dB (max)
V_{RFT}	CCD Reset Feed Through Amplitude		2		V (max)
ADC Characteristics					
	Resolution with No Missing Codes			**8**	Bits (min)
ILE	Integral Linearity Error (Note 11)		±0.5	**±1**	LSB (max)
DNL	Differential Non-Linearity		±0.5	**±1**	LSB (max)
PGA Characteristics					
	Monotonicity			**7**	bits (min)
	Gain Range	$Gain_{PGA} = 20\log_{10}\left(1 + \frac{PGA\ code}{128}\right)$		**0**	dB (min)
				6	dB (max)
	Gain Error at any gain			**1.0**	% (max)
VGA Characteristics					
	VGA Gain Error vs. Formula	$Gain_{VGA} = 1 + 2\left(\frac{V_{GAIN} + 0.12V}{REF\,OUT_{MID}}\right)$		**±6**	% (max)
Coarse Offset Trim Characteristics					
	Offset DAC LSB Size		1		LSB
System Characteristics					
	Full Channel Offset Error (Adjusted)	Offset DAC, Offset Add Adjusted		**±1**	LSB (max)
	Full Channel Gain Error	PGA Gain = 0 dB		**−5**	% (min)
				+10	% (max)
Reference and Analog Input Characteristics (Note 7)					
	OS Input Capacitance		5		pF
	OS Input Leakage Current	Measured with OS = 2.45V_{DC}	2	**20**	nA (max)
R_{REF}	ADC Reference Ladder (REF OUT_{HI} to REF IN) Impedance		1000	**500**	Ω (min)
				2000	Ω (max)
REF IN	Reference Voltage (Note 12)		1.225	**1.19**	V (min)
				1.26	V (max)

DC and Logic Electrical Characteristics

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, V_A = V_D = +5.0V_{DC}, $V_{D(I/O)}$ = +5.0 or +3.0V_{DC}, REF IN = +1.225V_{DC}, f_{MCLK} = 20MHz, R_s = 25Ω. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CD0–CD6, MCLK, SYNC, SDI, SCLK, $\overline{CS}$, $\overline{RD}$ Digital Input Characteristics					
$V_{IN(1)}$	Logical “1” Input Voltage	$V_{D(I/O)}$ = 5.25V		**2.0**	V (min)
		$V_{D(I/O)}$ = 3.6V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	$V_{D(I/O)}$ = 4.75V		**0.8**	V (max)
		$V_{D(I/O)}$ = 2.7V		**0.7**	V (max)
I_{IN}	Input Leakage Current	V_{IN} = V_D	0.1		µA
		V_{IN} = DGND	−0.1		µA
C_{IN}	Input Capacitance		5		pF
DD0–DD7, $\overline{EOC}$, CCLK, SDO Digital Output Characteristics					
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_{D(I/O)}$ = 4.75V, I_{OUT} = −360 µA		**2.4**	V (min)
		$V_{D(I/O)}$ = 4.75V, I_{OUT} = −10 µA		**4.4**	V (min)
		$V_{D(I/O)}$ = 2.7V, I_{OUT} = −360 µA		**2.1**	V (min)
		$V_{D(I/O)}$ = 2.7V, I_{OUT} = −10 µA		**2.5**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_{D(I/O)}$ = 5.25V, I_{OUT} = 1.6 mA		**0.4**	V (max)
		$V_{D(I/O)}$ = 3.6V, I_{OUT} = 1.6 mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	V_{OUT} = DGND	0.1		µA
	(DD0–DD7 only)	V_{OUT} = V_D	−0.1		µA
C_{OUT}	TRI-STATE Output Capacitance		5		pF
φ1, φ2, RS, TR Digital Output Characteristics					
$V_{OUT(1)}$	Logical “1” Output Voltage	V_D = 4.75V, I_{OUT} = −360 µA		**2.4**	V (min)
		V_D = 4.75V, I_{OUT} = −10 µA		**4.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	V_D = 5.25V, I_{OUT} = 1.6 mA		**0.4**	V (max)
Power Supply Characteristics					
I_A	Analog Supply Current	Operating	32	**42**	mA (max)
		Standby	20		µA
I_D	Digital Supply Current	Operating	6	**10**	mA (max)
		Standby	4		mA
$I_{D(I/O)}$	Digital I/O Supply Current	Operating, $V_{D(I/O)}$ = 5.0V	3.5	**6**	mA (max)
		Operating, $V_{D(I/O)}$ = 3.0V	1.6	**2**	mA (max)
		Standby, $V_{D(I/O)}$ = 5.0V or 3.0V	0.5		mA

AC Electrical Characteristics, MCLK Independent

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, V_A = V_D = $V_{D(I/O)}$ = +5.0V_{DC}, REF IN = +1.225V_{DC}, f_{MCLK} = 20MHz, t_{MCLK} = 1/f_{MCLK}, t_r = t_f = 5ns, R_s = 25Ω, C_L (databus loading) = 50 pF/pin. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
f_{MCLK}	Maximum MCLK Frequency			**20**	MHz (min)
	Minimum MCLK Frequency			**5**	MHz (max)
	MCLK Duty Cycle		30	**40**	% (min)
			70	**60**	% (max)
t_A	SYNC setup of MCLK		5	**10**	ns (min)
$t_{CDSETUP}$	Correction Data valid to CLK Setup		14	**20**	ns (min)
t_{CDHOLD}	Correction Data valid to CLK Hold		−12	**0**	ns (min)
t_{D1H}, t_{D0H}	$\overline{RD}$ High to DD0–DD7 TRI-STATE		7	**15**	ns (max)

AC Electrical Characteristics, MCLK Independent (Continued)

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, $V_A = V_D = V_{D(I/O)}$ = +5.0V_{DC}, REF IN = +1.225V_{DC}, f_{MCLK} = 20MHz, $t_{MCLK} = 1/f_{MCLK}$, $t_r = t_f$ = 5ns, R_s = 25Ω, C_L (databus loading) = 50 pF/pin. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
t_{DACC}	Access Time Delay from $\overline{RD}$ Low to DD0–DD7 Data Valid		20	**40**	ns (max)
f_{SCLK}	Maximum SCLK Frequency			**2.5**	MHz (max)
	SCLK Duty Cycle			**40**	% (min)
				60	% (max)
t_{SDI}	SDI Set-Up Time from SCLK Rising Edge		3	**10**	ns (min)
t_{HDI}	SDI Hold Time from SCLK Rising Edge		2	**15**	ns (min)
t_{DDO}	Delay from SCLK Falling Edge to SDO Data Valid		35	**55**	ns (max)
t_{HDO}	SDO Hold Time from SCLK	R_L = 3K, C_L = 25 pF	21	**55**	ns (max)
	Falling Edge			**5**	ns (min)
t_{DELAY}	DELAY from SCLK Falling Edge to $\overline{CS}$ Rising or Falling Edge		2	**5**	ns (min)
t_{SETUP}	Set-Up Time of $\overline{CS}$ Rising or Falling Edge to SCLK Rising Edge		−2	**10**	ns (min)
t_{SACC}	Access Time Delay from CS Falling Edge to SDO Data Valid		20	**40**	ns (max)
t_{S1H}, t_{S0H}	Delay from CS Rising Edge to SDO TRI-STATE	R_L = 3K, C_L = 50 pF	40	**100**	ns (max)
t_{RDO}	SDO Rise Time, TRI-STATE to High	R_L = 3K, C_L = 50 pF	20		ns
	SDO Rise Time, Low to High		20		ns
t_{FDO}	SDO Fall Time, TRI-STATE to Low	R_L = 3K, C_L = 50 pF	20		ns
	SDO Fall Time, High to Low		20		ns

AC Electrical Characteristics, MCLK Dependent

The following specifications apply for AGND = DGND = $DGND_{(I/O)}$ = 0V, V_A = V_D = $V_{D(I/O)}$ = +5.0 V_{DC}, REF IN = +1.225 V_{DC}, f_{MCLK} = 20MHz, t_{MCLK} = $1/f_{MCLK}$, t_r = t_f = 5ns, R_s = 25Ω, C_L (databus loading) = 50 pF/pin. Refer to *Table 2* **: Configuration Register Parameters** for limits labelled **C.R. Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
t_{START}	MCLK to first ϕ1 high		50ns	**1**	t_{MCLK}
t_{ϕ}	ϕ1, ϕ2 Clock Period	Standard CCD Mode	400ns	**8**	t_{MCLK}
		Even/Odd CCD Mode	800ns	**16**	t_{MCLK}
$t_{TRWIDTH}$	Transfer Pulse (TR) Width			**C.R.**	µs
t_{GUARD}	ϕ1 to TR, TR to ϕ1 Guardband			**C.R.**	ns
$t_{RSWIDTH}$	Reset Pulse (RS) Width			**C.R.**	ns
t_{RS}	Falling Edge of ϕ1 to RS	Standard CCD Mode		**C.R.**	ns
	Either Edge of ϕ1 to RS	Even/Odd CCD Mode			
$t_{S/HREF}$	Falling Edge of ϕ1 to Ref. Sample	Standard CCD Mode		**C.R.**	ns
	Either Edge of ϕ1 to Ref. Sample	Even/Odd CCD Mode			
$t_{S/HSIG}$	Falling Edge of ϕ1 to Sig. Sample	Standard CCD Mode		**C.R.**	ns
	Either Edge of ϕ1 to Sig. Sample	Even/Odd CCD Mode			
$t_{S/HWIDTH}$	Sample Pulse Width (Acquisition Time)		50ns	**1**	t_{MCLK}
$t_{SYNCLOW}$	SYNC Low Between Lines		100ns	**2**	t_{MCLK} (min)
t_B	SYNC Setup of ϕ1 to end line			**2**	t_{MCLK} (max)
$t_{CCLKWIDTH}$	CCLK Pulse Width		250ns	**5**	t_{MCLK}
$t_{DATAVALID}$	Data Valid Time from $\overline{EOC}$ Low			**300**	ns (min)
$t_{\overline{EOC}WIDTH}$	$\overline{EOC}$ Pulse Width		250ns	**5**	t_{MCLK}
	ϕ1 and ϕ2 Frequency	Standard CCD Mode	2.5MHz	$\mathbf{f_{MCLK}/8}$	Hz
		Even/Odd CCD Mode	1.25MHz	$\mathbf{f_{MCLK}/16}$	Hz
	ϕ1 and ϕ2 Duty Cycle			**50**	%

Electrical Characteristics (Notes)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = $DGND_{(I/O)}$ = 0V, unless otherwise specified.

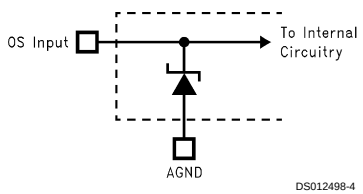
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is P_D = $(T_{Jmax}–T_A)/\theta_{JA}$. T_{Jmax} = 150˚C for this device. The typical thermal resistance θ_{JA} of this part when board mounted is 52˚C/W for the V52A PLCC package.

Note 5: Human body model, 100 pF capacitor discharged through a 1.5Ω resistor.

Note 6: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: A Zener diode clamps the OS analog input to AGND as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the CCD, prevents damage to the LM9800 from transients during power-up.



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Note 8: To guarantee accuracy, it is required that V_A and V_D be connected together to the same power supply with separate bypass capacitors at each supply pin.

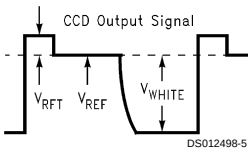
Note 9: Typicals are at T_J = T_A = 25˚C, f_{MCLK} = 20MHz, and represent most likely parametric norm.

Note 10: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Electrical Characteristics (Notes) (Continued)

Note 11: Integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that best fits the actual transfer function of the ADC.

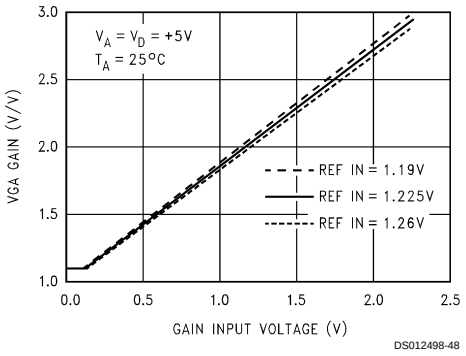
Note 12: V_{REF} is defined as the CCD OS voltage for the reference period following the reset feedthrough pulse. V_{WHITE} is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to the reference level, V_{REF}. V_{RFT} is defined as the peak positive deviation above V_{REF} of the reset feedthrough pulse. The maximum correctable range of pixel-to-pixel V_{WHITE} variation is defined as the maximum variation in V_{WHITE} (due to PRNU, light source intensity variation, optics, etc.) that the LM9800 can correct for using its internal PGA.



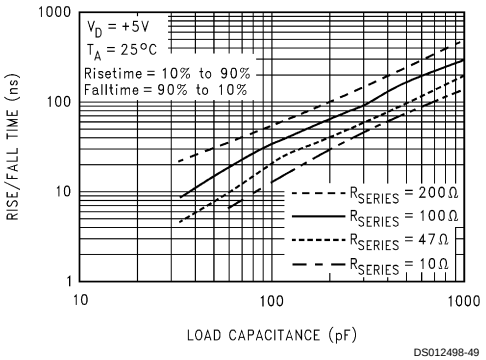
Note 13: Reference voltages below 1.19V may decrease SNR. Reference voltages above 1.26V may cause clipping errors inside the LM9800. The LM4041EIM3-1.2 (SOT-23 package) or the LM4041EIZ-1.2 (TO-92 package) bandgap voltage references are recommended for this application.

Typical Performance Characteristics

VGA Gain vs Voltage on GAIN Input



ϕ1, ϕ2, RS, TR Rise and Fall Times Through a Series Resistance vs. Load Capacitance



Pin Descriptions

CCD Driver Signals	
ϕ1	Digital Output. CCD clock signal, phase 1.
ϕ2	Digital Output. CCD clock signal, phase 2.
RS	Digital Output. Reset pulse for the CCD.
TR	Digital Output. Transfer pulse for the CCD.
Analog I/O	
OS	Analog Input. This is the OS (Output Signal) from the CCD. The maximum peak signal that can be accurately digitized is equal to the voltage at REF IN, typically 1.225V.
GAIN	Analog Input. The voltage on this pin determines the gain of the VGA when the VGA is enabled. This input should be bypassed to AGND using a 0.1 µF monolithic capacitor.
REF IN	Analog Inputs. These two pins are the system reference voltage inputs and should be tied together to a 1.225V voltage source and bypassed to AGND with a 0.1 µF monolithic capacitor.
$REF\ OUT_{HI}$	Analog Output. This reference voltage is developed internally by the LM9800, and is equal to 3 times REF IN. It should be bypassed to AGND with a 0.1 µF monolithic capacitor.
$REF\ OUT_{MID}$	Analog Output. This reference voltage is developed internally by the LM9800, and is equal to 2 times REF IN. It should be bypassed to AGND using a 0.1 µF monolithic capacitor. This pin can source up to 250 µA when used to power a voltage divider for setting the voltage at the GAIN input.
I_{SET}	Analog Input. This input is used to set internal bias currents inside the LM9800. It should be connected to V_A through a 75 kΩ resistor.

Pin Descriptions (Continued)

V_{TEST1}, V_{TEST2}	Analog Inputs/Outputs. These pins are used for testing the device during manufacture and should be left unconnected.
Configuration Register I/O	
SDI	Digital Input. Serial Data Input pin.
SDO	Digital Output. Serial Data Output pin.
SCLK	Digital Input. This is the serial data clock, used to clock data in through SDI and out through SDO. SCLK is asynchronous to MCLK. Input data is latched and output data is changed on the rising edge of SCLK.
$\overline{CS}$	Digital Input. This is the Chip Select signal for writing to the Configuration Register through the serial interface. This input must be low in order to communicate with the Configuration Register. This pin is used for serial I/O only–it has no effect on any other section of the chip. **Note: The SYNC pin must be high to read or write from the Configuration register.**
General Digital I/O	
MCLK	Digital Input. This is the 20 MHz (typical) master system clock.
SYNC	Digital Input. A low-to-high transition on this input begins a line scan operation. The line scan operation terminates when this input is taken low. A low-to-high transition on this input will also reset the serial I/O port to the Configuration Register. The SYNC pin must be high to read or write from the Configuration register.
Digital Coefficient I/O	
CD0 (LSB)–CD6 (MSB)	Digital Inputs. Correction Coefficient Databus. This is the 7-bit data path for the gain adjust PGA, used during line scan.
CCLK	Digital Output. This is the signal that is used to clock the Gain coefficients into the LM9800. Data is latched on the rising edge of CCLK.

Digital Output I/O	
DD0 (LSB)–DD7 (MSB)	Digital Outputs. Pixel Output Databus. This data bus outputs the 8-bit digital output data during line scan.
$\overline{EOC}$	Digital Output. This is the End of Conversion signal from the ADC indicating that new pixel data is available.
$\overline{RD}$	Digital Input. Taking this input low places the data stored in the output latch on the bus. When this input is high the DD0–DD7 bus is in TRI-STATE.
Analog Power	
V_A	This is the positive supply pin for the analog supply. It should be connected to a voltage source of +5V and bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF tantalum capacitor.
AGND	This is the ground return for the analog supply.
Digital Power	
V_D	This is the positive supply pin for the digital supply. It should be connected to a voltage source of +5V and bypassed to DGND with a 0.1 µF monolithic capacitor.
DGND	This is the ground return for the digital supply.
$V_{D(I/O)}$	This is the positive supply pin for the digital supply for the LM9800's I/O. It should be connected to a voltage source of +3V to +5V and bypassed to $DGND_{(I/O)}$ with a 0.1 µF monolithic capacitor. If the supply for this pin is different than the supply for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor.
$DGND_{(I/O)}$	This is the ground return for the digital supply for the LM9800's I/O.

Timing Diagrams

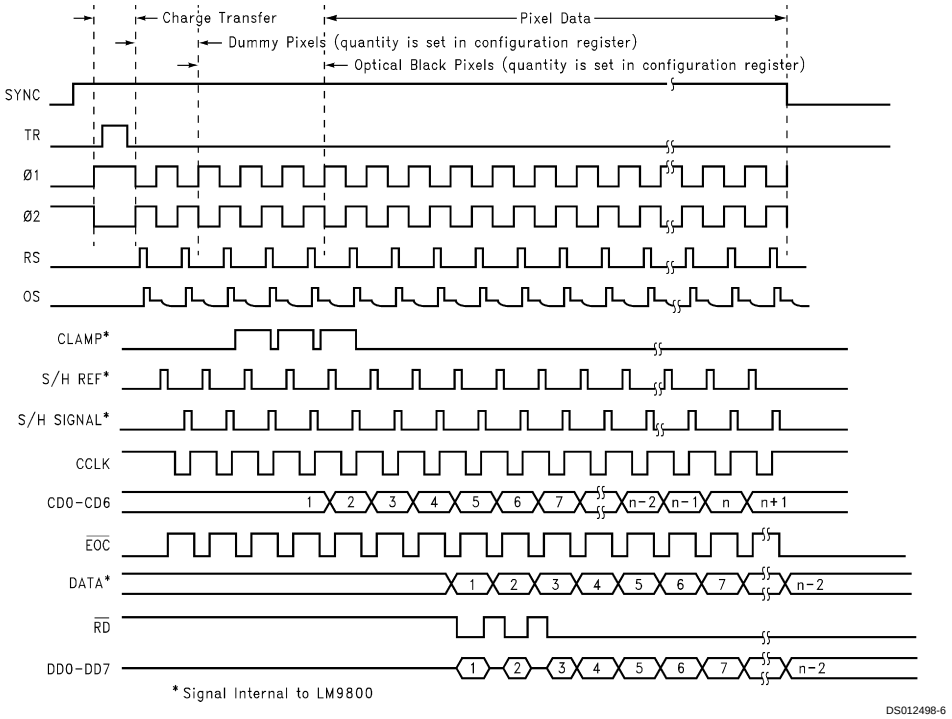


FIGURE 1. Line Scan Timing Overview

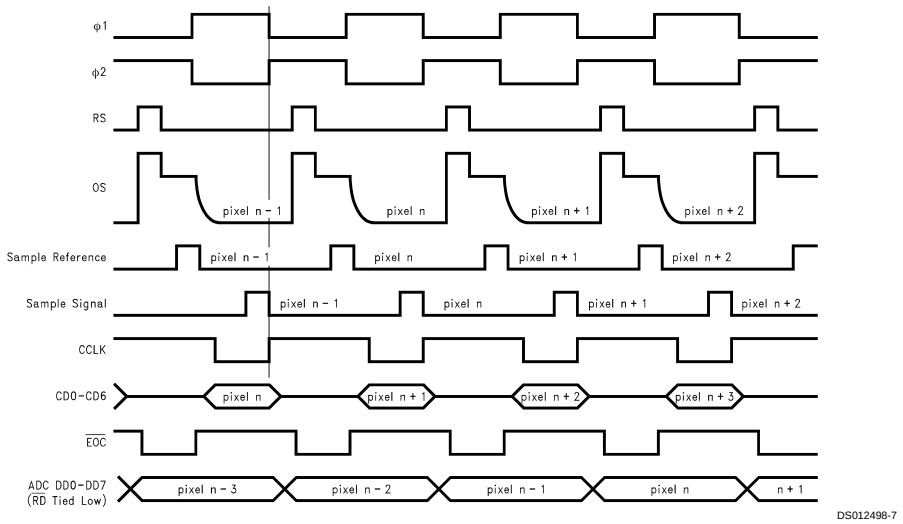
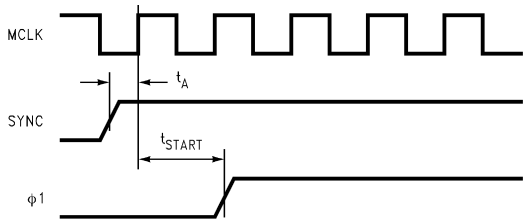


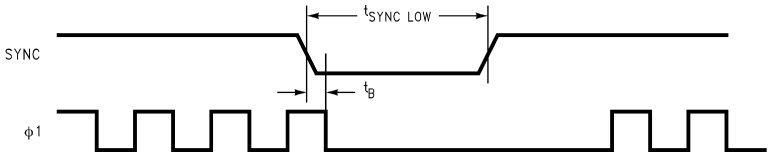
FIGURE 2. Pixel Pipeline Timing Overview

Timing Diagrams (Continued)



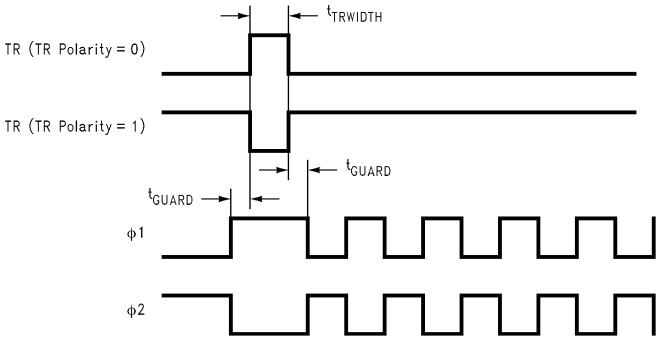
DS012498-8

FIGURE 3. Timing for Start of Line Scan



DS012498-9

FIGURE 4. Timing for End of Line/Start of Next Line



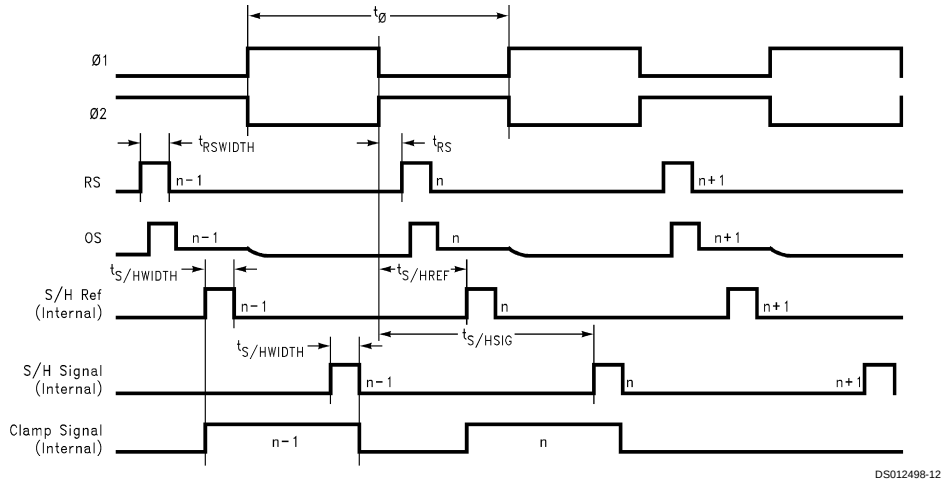
DS012498-10

FIGURE 5. TR Pulse

DS012498-11

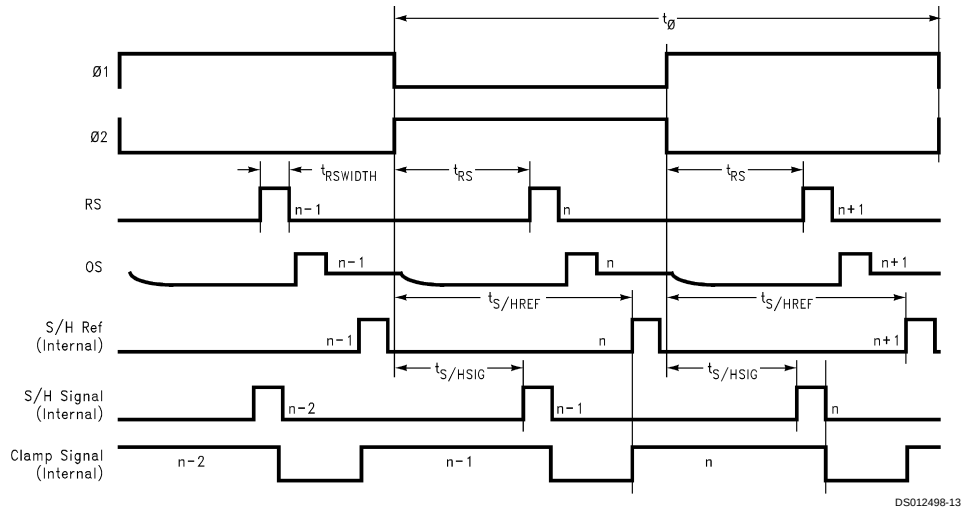
FIGURE 6. RS Pulse Polarity

Timing Diagrams (Continued)



Note: Clamp signal only active during optical black pixels at beginning of line.

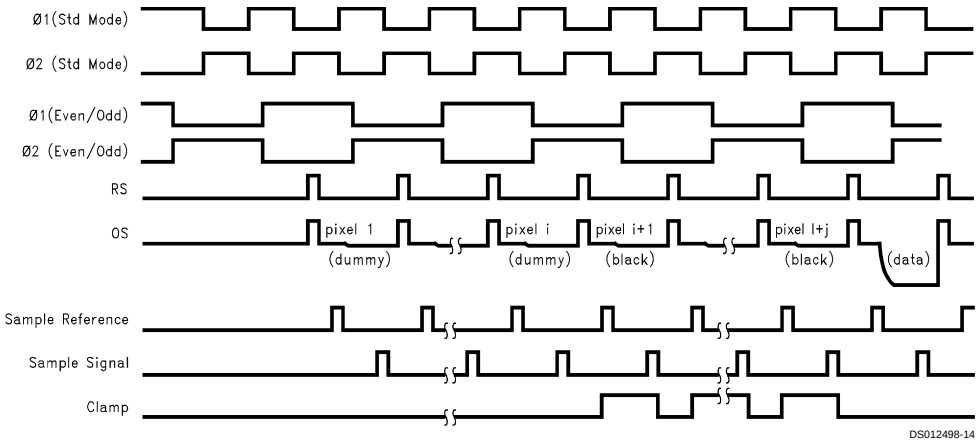
FIGURE 7. CCD Timing



Note: Clamp signal only active during optical black pixels at beginning of line.

FIGURE 8. CCD Timing (Even/Odd CCDs)

Timing Diagrams (Continued)



Note: j = value programmed in Optical Black Register.
i = value programmed in Dummy Pixel Register - 1 (for example: dummy pixel register = 1 ≥ i = 0 ≥ no dummy pixels).

FIGURE 9. Dummy Pixel and Optical Black Pixel Timing

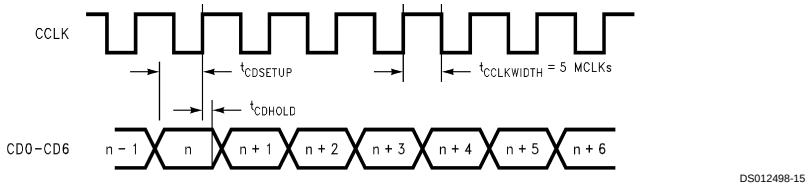


FIGURE 10. Coefficient Data Timing

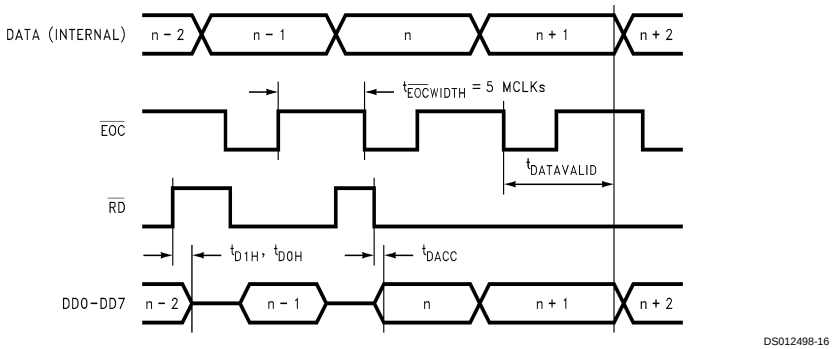


FIGURE 11. Output Data Timing

Timing Diagrams (Continued)

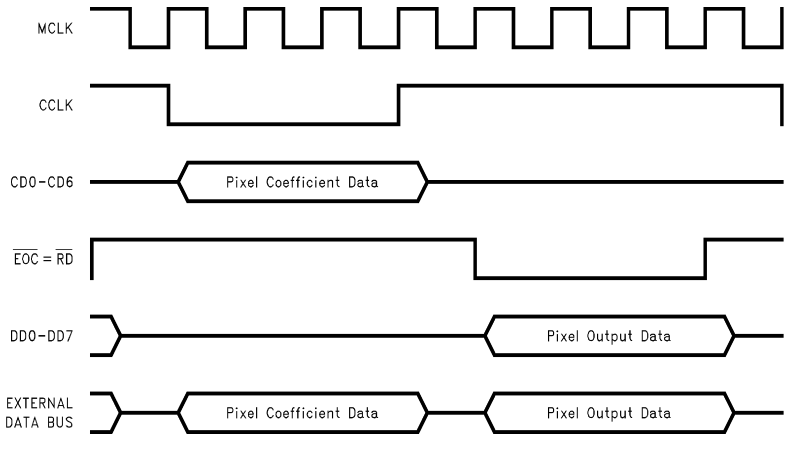
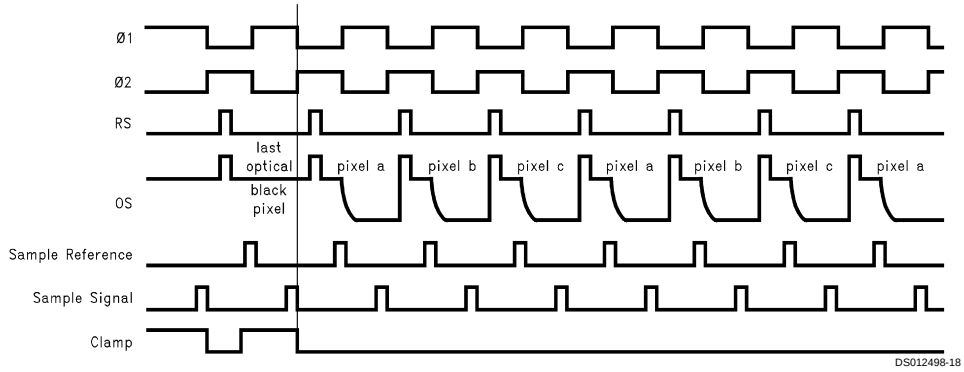


FIGURE 12. Data Timing (Output and Coefficient Data Sharing Same Bus)



Note: VGA operation (on or off) for "a" pixels, "b" pixels, and "c" pixels is set in the configuration register.
VGA is always *off* for first "a" pixel immediately following last optical black pixel.

FIGURE 13. VGA Gain Switching

Serial Configuration Register Timing Diagrams

Note: SYNC pin must be held HIGH (+5V) to read from or write to configuration register.

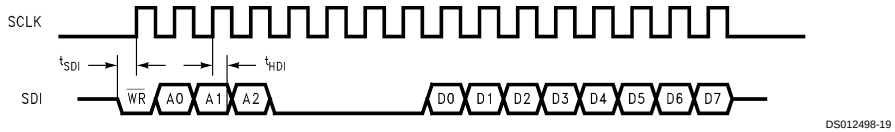


FIGURE 14. Configuration Register Write Timing with $\overline{CS}$ Continuously Low (16-bit Word)

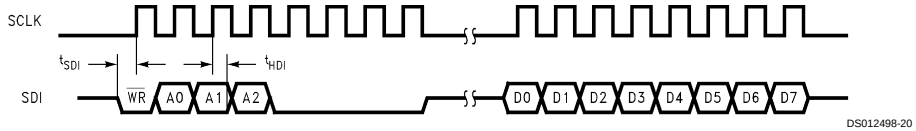


FIGURE 15. Configuration Register Write Timing with $\overline{CS}$ Continuously Low (Two 8-bit bytes)

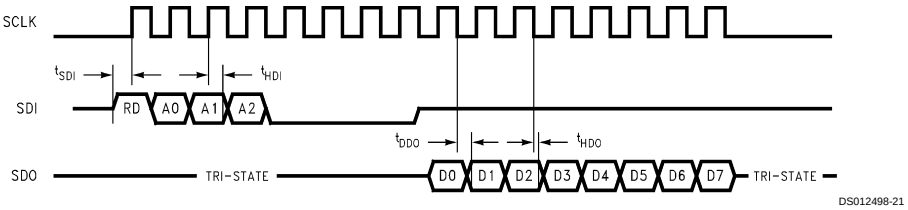


FIGURE 16. Configuration Register Read Timing with $\overline{CS}$ Continuously Low (16-bit Word)

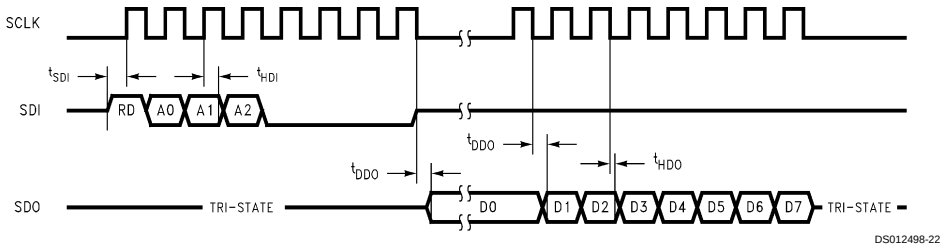
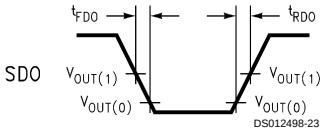


FIGURE 17. Configuration Register Read Timing with $\overline{CS}$ Continuously Low (Two 8-bit bytes)

SDO Falling and Rising Edge



SDO "TRI-STATE" Falling and Rising Edge

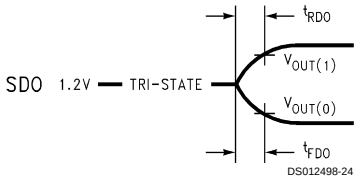


FIGURE 18. SDO Timing

Serial Configuration Register Timing Diagrams

Note: SYNC pin must be held HIGH (+5V) to read from or write to configuration register. (Continued)

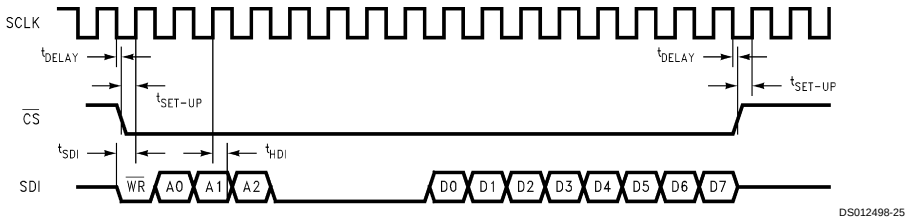


FIGURE 19. Configuration Register Write Timing using $\overline{CS}$, Continuous SCLK (16-bit Word)

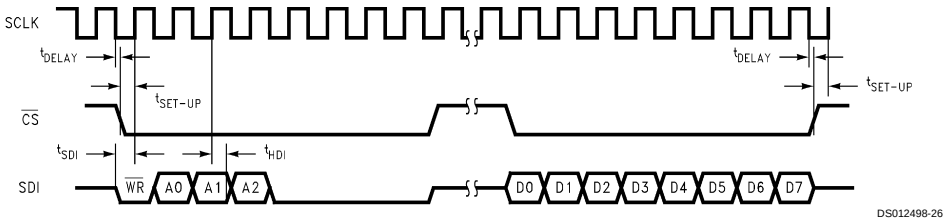


FIGURE 20. Configuration Register Write Timing using $\overline{CS}$, Continuous SCLK (Two 8-bit bytes)

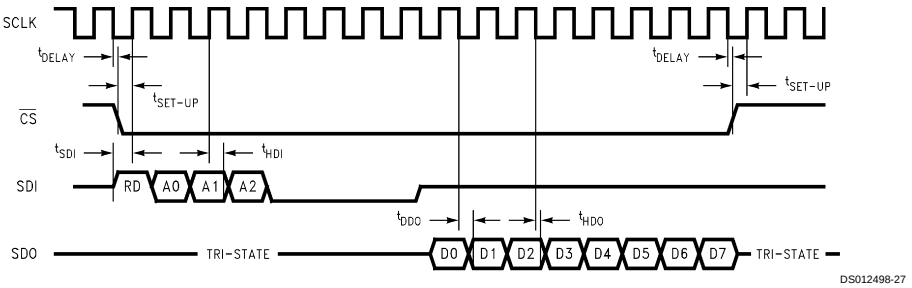


FIGURE 21. Configuration Register Read Timing using $\overline{CS}$, Continuous SCLK (16-bit Word)

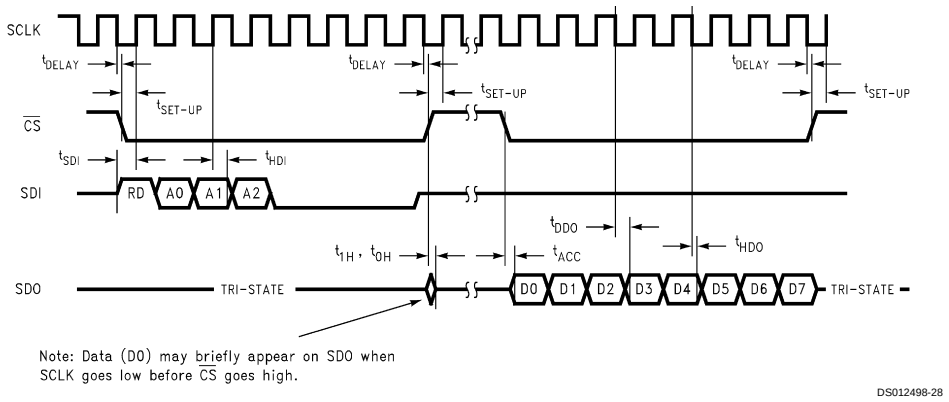
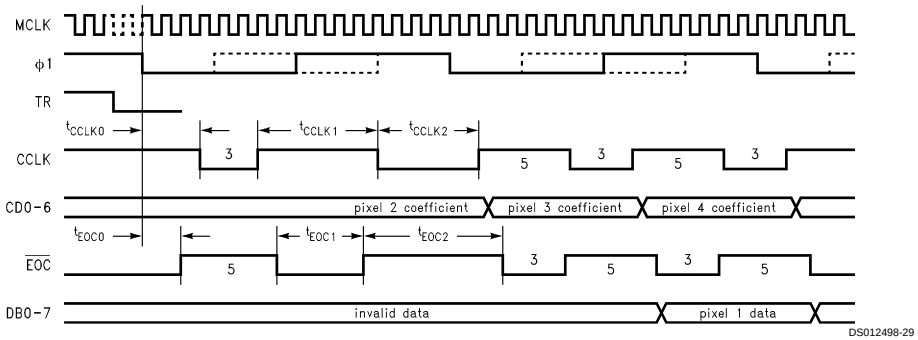


FIGURE 22. Configuration Register Read Timing using $\overline{CS}$, Continuous SCLK (Two 8-bit bytes)

EOC and CCLK Start of Line Timing Diagrams

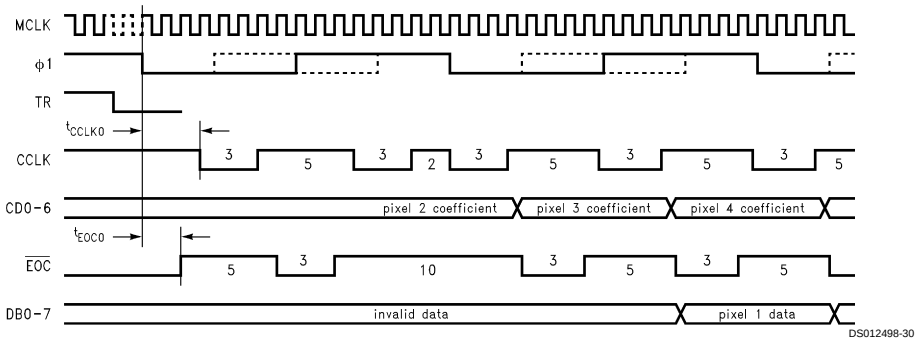
(See Section 2.4)

RS Even	RS Odd	t_{EOC1} (MCLKs)	t_{EOC2} (MCLKs)	t_{CCLK1} (MCLKs)	t_{CCLK2} (MCLKs)
SR = 0	SR = 0 or 1	2	5	4	3
SR = 1 or 2	SR = 2 or 3	3	5	5	3
SR = 3 or 4	SR = 4 or 5	3	6	6	3
SR = 5 or 6	SR = 6 or 7	3	7	5	5
SR = 7 or 8	SR = 8 or 9	3	8	5	6
SR = 9 or 10	SR = 10 or 11	3	9	5	7



RS Even, SR = 0 to 10: t_{EOC0} = 2 MCLKs, t_{CCLK0} = 3 MCLKs
RS Odd, SR = 0 to 11: t_{EOC0} = 2.5 MCLKs, $t_{CCLK0)}$ = 3.5 MCLKs

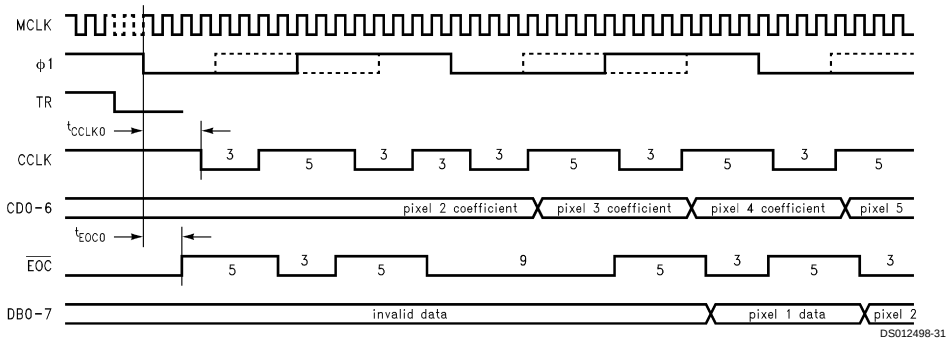
FIGURE 23. SR = 0 through 10 (RS Even), SR = 0 through 11 (RS Odd)



RS Even, SR = 11 or 12: t_{EOC0} = 2 MCLKs, t_{CCLK0} = 3 MCLKs
RS Odd, SR = 12 or 13: t_{EOC0} = 2.5 MCLKs, t_{CCLK0} = 3.5 MCLKs

FIGURE 24. SR = 11 or 12 (RS Even), SR = 12 or 13 (RS Odd)

EOC and CCLK Start of Line Timing Diagrams (Continued)



RS Even, SR = 13 or 14: t_{EOC0} = 2 MCLKs, t_{CCLK0} = 3 MCLKs
RS Odd, SR = 14 or 15: t_{EOC0} = 2.5 MCLKs, t_{CCLK0} = 3.5 MCLKs

FIGURE 25. SR = 13 or 14 (RS Even), SR = 14 or 15 (RS Odd)

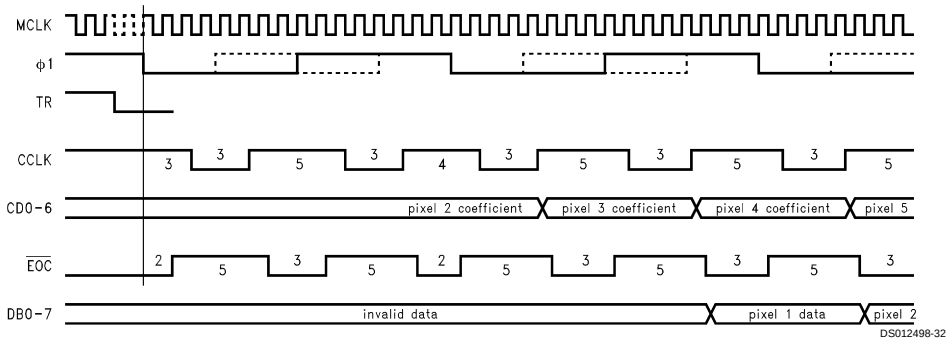


FIGURE 26. SR = 15 (RS Even)

Configuration Register

$t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20MHz (t_{MCLK} = 50ns).

TABLE 1. Configuration Register Address Table

A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Standard Mode or Even/Odd Mode	RS Pulse Width		RS Pulse Polarity	RS Pulse Position (Minimum Value is 1)			
			MODE	RSW1	RSW0	RSPOL	RSPOS3	RSPOS2	RSPOS1	RSPOS0
0	0	1	Sample Reference Position				Sample Signal Position			
			SR3	SR2	SR1	SR0	SS3	SS2	SS1	SS0
0	1	0	ϕ1 Enable	ϕ2 Enable	RS Enable	TR Enable	TR Pulse Width		TR–ϕ1 Guardband	TR Polarity
			ϕ1EN	ϕ2EN	RSEN	TREN	TRW1	TRW0	TRGRD	TRPOL
0	1	1	Dummy Pixels (Minimum Value is 1)							
			BLS7	BLS6	BLS5	BLS4	BLS3	BLS2	BLS1	BLS0
1	0	0	Optical Black Pixels (Minimum Value is 1)							
			BLL7	BLL6	BLL5	BLL4	BLL3	BLL2	BLL1	BLL0
1	0	1	PGA Gain Coefficient							
			0	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0
1	1	0	PGA Gain Source	Test Mode	Power-down	Offset Add	VGA On/Off	VGA State Pixel c	VGA State Pixel b	VGA State Pixel a
			PGASRC	0	PD	OFFADD	VGA	G3	G2	G1
1	1	1	Offset DAC Sign	Offset DAC MSB	Offset DAC	Offset DAC LSB	Test Modes			
			ODSIGN	VOS2	VOS1	VOS0	0	0	0	0

Configuration Register

$t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20MHz (t_{MCLK} = 50ns). (Continued)

TABLE 2. Configuration Register Parameters

Parameter	Control Bits				Result
MODE	MODE				
	0				Standard CCD (ϕ frequency = $f_{MCLK}/8$)
	1				Even/Odd CCD (ϕ frequency = $f_{MCLK}/16$)
RS Pulse Width ($t_{RSWIDTH}$)	RS1	RS0			
	0	0			1 t_{MCLK} (50ns)
	0	1			2 t_{MCLK} (100ns)
	1	0			3 t_{MCLK} (150ns)
	1	1			4 t_{MCLK} (200ns)
RS Pulse Polarity	RSPOL				
	0				RS
	1				$\overline{RS}$
RS Pulse Position (t_{RS}) **Note:** Minimum Value is 1	RSPOS3	RSPOS2	RSPOS1	RSPOS0	
	0	0	0	0	Not Valid
	0	0	0	1	0.5t_{MCLK} (25 ns)
	0	0	1	0	1.0t_{MCLK} (50ns)
	0	0	1	1	1.5t_{MCLK} (75ns)
	0	1	0	0	2.0t_{MCLK} (100ns)
	0	1	0	1	2.5t_{MCLK} (125ns)
	0	1	1	0	3.0t_{MCLK} (150ns)
	0	1	1	1	3.5t_{MCLK} (175ns)
	1	0	0	0	4.0t_{MCLK} (200ns)
	1	0	0	1	4.5t_{MCLK} (225ns)
	1	0	1	0	5.0t_{MCLK} (250ns)
	1	0	1	1	5.5t_{MCLK} (275ns)
	1	1	0	0	6.0t_{MCLK} (300 ns)
	1	1	0	1	6.5t_{MCLK} (325 ns)
	1	1	1	0	7.0t_{MCLK} (350 ns)
	1	1	1	1	7.5t_{MCLK} (375 ns)
Sample Reference Position ($t_{S/HREF}$)	SR3	SR2	SR1	SR0	
	0	0	0	0	0.0t_{MCLK} (0 ns)
	0	0	0	1	0.5t_{MCLK} (25 ns)
	0	0	1	0	1.0t_{MCLK} (50 ns)
	0	0	1	1	1.5t_{MCLK} (75 ns)
	0	1	0	0	2.0t_{MCLK} (100 ns)
	0	1	0	1	2.5t_{MCLK} (125 ns)
	0	1	1	0	3.0t_{MCLK} (150 ns)
	0	1	1	1	3.5t_{MCLK} (175 ns)
	1	0	0	0	4.0t_{MCLK} (200 ns)
	1	0	0	1	4.5t_{MCLK} (225 ns)
	1	0	1	0	5.0t_{MCLK} (250 ns)
	1	0	1	1	5.5t_{MCLK} (275 ns)
	1	1	0	0	6.0t_{MCLK} (300 ns)
	1	1	0	1	6.5t_{MCLK} (325 ns)
	1	1	1	0	7.0t_{MCLK} (350 ns)
	1	1	1	1	7.5t_{MCLK} (375 ns)

Configuration Register $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20MHz (t_{MCLK} = 50ns). (Continued)

TABLE 2. Configuration Register Parameters (Continued)

Parameter	Control Bits				Result
Sample Signal Position ($t_{S/HSIG}$)	SS3	SS2	SS1	SS0	
	0	0	0	0	$0.0t_{MCLK}$ (0 ns)
	0	0	0	1	$0.5t_{MCLK}$ (25 ns)
	0	0	1	0	$1.0t_{MCLK}$ (50 ns)
	0	0	1	1	$1.5t_{MCLK}$ (75 ns)
	0	1	0	0	$2.0t_{MCLK}$ (100 ns)
	0	1	0	1	$2.5t_{MCLK}$ (125 ns)
	0	1	1	0	$3.0t_{MCLK}$ (150 ns)
	0	1	1	1	$3.5t_{MCLK}$ (175 ns)
	1	0	0	0	$4.0t_{MCLK}$ (200 ns)
	1	0	0	1	$4.5t_{MCLK}$ (225 ns)
	1	0	1	0	$5.0t_{MCLK}$ (250 ns)
	1	0	1	1	$5.5t_{MCLK}$ (275 ns)
	1	1	0	0	$6.0t_{MCLK}$ (300 ns)
	1	1	0	1	$6.5t_{MCLK}$ (325 ns)
	1	1	1	0	$7.0t_{MCLK}$ (350 ns)
	1	1	1	1	$7.5t_{MCLK}$ (375 ns)
ϕ1 Enable	ϕ1EN				
	0				ϕ1 Output Off
	1				ϕ1 Output On
ϕ2 Enable	ϕ2EN				
	0				ϕ2 Output Off
	1				ϕ2 Output On
RS Enable	RSEN				
	0				RS Output Off
	1				RS Output On
TR Enable	TREN				
	0				TR Output Off
	1				TR Output On
TR Pulse Width ($t_{TRWIDTH}$)	TRW1	TRW0			
	0	0			20 t_{MCLK} (1.0 µs)
	0	1			30 t_{MCLK} (1.5 µs)
	1	0			40 t_{MCLK} (2.0 µs)
	1	1			50 t_{MCLK} (2.5 µs)
TR-ϕ1 Guardband (t_{GUARD})	TRGRD				
	0				1 t_{MCLK} (50 ns)
	1				2 t_{MCLK} (100 ns)
TR Polarity	TRPOL				
	0				TR
	1				$\overline{TR}$

Configuration Register $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20MHz (t_{MCLK} = 50ns). (Continued)

TABLE 2. Configuration Register Parameters (Continued)

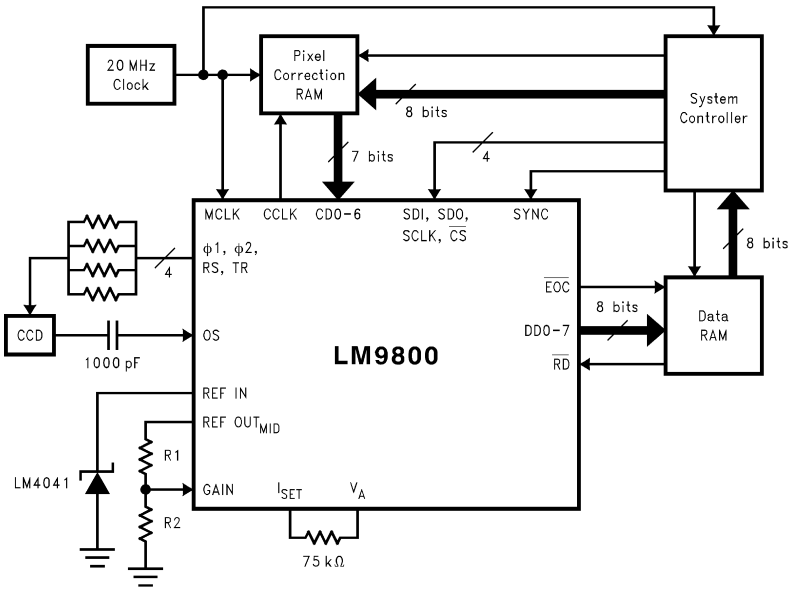
Parameter	Control Bits								Result
Dummy Pixels	BLS7	BLS6	BLS5	BLS4	BLS3	BLS2	BLS1	BLS0	
Note: Minimum Value is 1. Actual number of dummy pixels in CCD should be one less than number in this register.	0	0	0	0	0	0	0	0	Not Valid
	0	0	0	0	0	0	0	1	0
	0	0	0	0	0	0	1	0	1
	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•
	1	1	1	1	1	1	1	0	253
	1	1	1	1	1	1	1	1	254
Optical Black Pixels	BLL7	BLL6	BLL5	BLL4	BLL3	BLL2	BLL1	BLL0	
Note: Minimum Value is 1	0	0	0	0	0	0	0	0	Not Valid
	0	0	0	0	0	0	0	1	1
	0	0	0	0	0	0	1	0	2
	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•
	1	1	1	1	1	1	1	0	254
	1	1	1	1	1	1	1	1	255
Internal PGA Gain Coefficient	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0		
	0	0	0	0	0	0	0		0 [0 dB]
	0	0	0	0	0	0	1		1
	•	•	•	•	•	•	•		•
	•	•	•	•	•	•	•		•
	•	•	•	•	•	•	•		•
	1	1	1	1	1	1	0		126
	1	1	1	1	1	1	1		127 [6 dB]
PGA Gain Coefficient Source	PGASRC								
	0								Internal
	1								External
Power Down	PD								
	0								Operating
	1								Power Down
Offset Add	OFF ADD								
	0								Offset ~0 LSB
	1								Offset ~+1 LSB
Master VGA Control	VGA								
	0								VGA Disabled
	1								VGA Enabled
VGA State for Pixel "c"	VGA_c								
	0								VGA bypassed
	1								VGA on
VGA State for Pixel "b"	VGA_b								
	0								VGA bypassed
	1								VGA on

Configuration Register $t_{MCLK} = 1/f_{MCLK}$ = 1 MCLK period. Examples given in parenthesis are for f_{MCLK} = 20MHz (t_{MCLK} = 50ns). (Continued)

TABLE 2. Configuration Register Parameters (Continued)

Parameter	Control Bits				Result
VGA State for Pixel "a"	VGA_a				
	0				VGA bypassed
	1				VGA on
Offset DAC	Sign	VOS1	VOS1	VOS0	Offset (LSB)
	1	0	0	0	0
	1	0	0	1	+1
	1	0	1	0	+2
	1	0	1	1	+3
	1	1	0	0	+4
	1	1	0	1	+5
	1	1	1	0	+6
	1	1	1	1	+7
	0	0	0	0	0
	0	0	0	1	−1
	0	0	1	0	−2
	0	0	1	1	−3
	0	1	0	0	−4
	0	1	0	1	−5
	0	1	1	0	−6
	0	1	1	1	−7

Block Diagram of LM9800-Based System



Note: Power supplies and bypass capacitors not shown for clarity.

FIGURE 27. LM9800 System Block Diagram

Applications Information

1.0 THEORY OF OPERATION

The LM9800 removes errors from and digitizes a linear CCD pixel stream, while providing all the necessary clock signals to drive the CCD. Offset and gain errors are removed at the pixel rate, for individual pixels. Offset errors are removed through correlated double sampling (CDS). Gain errors (which may come from any combination of PRNU, uneven illumination, $\cos^4$ effect, RGB filter mismatch, etc.) are removed through the use of a 7-bit PGA in front of the ADC.

1.1 The Analog Signal Path (See Block Diagram)

The analog output signal from the CCD is connected to the OS Input of the LM9800 through a 0.001µF (typical, see section 4.2, *Clamp Capacitor Selection*) DC blocking capacitor. During the CCD's optical black pixel segment at the beginning of every line, this input is clamped to the REF OUT_{MID} voltage (approximately 2.45V). This DC restore operation fixes the reference level of the CCD pixel stream at REF OUT_{MID}.

The signal is then buffered and fed to a voltage-controlled VGA (variable gain amplifier). The VGA can be used to compensate for peak white CCD outputs less than the 1.225V full-scale required by the LM9800 for maximum dynamic range. It can also be used to increase the gain of the Blue signal in a sequential-output RGB CCD, since the VGA can be switched in and out of the circuit at the pixel rate. When used with parallel output CCDs the VGA can be used (in conjunction with an external multiplexer) to fine-tune the amplitude of the red, green, and blue signals. For a detailed explanation of the VGA, see section 4.3, *GAIN (VGA) Input.*

The output of the VGA goes into the CDS (Correlated Double Sampling) stage, consisting of two sample/hold amplifiers: S/H Ref (Reference) and S/H Signal. The Reference Level is sampled and held by the S/H Ref circuit and the active pixel data is sampled and held by the S/H Signal circuit. The output of S/H Ref is subtracted from the S/H Signal output and amplified by 2. The full-scale signal range at this point is approximately 2.45Vp-p. CDS reduces or eliminates many sources of noise, including reset noise, flicker noise, and both high and low frequency pixel-to-pixel offset variation. For more information on the CDS stage, see section 4.5, *Correlated Double Sampler (CDS)* .

At this point an offset voltage can be injected by the 4-bit Offset DAC. This voltage is designed to compensate for any small fixed DC offset introduced by the CDS S/Hs and the x2 amplifier. The LSB size of the DAC is approximately 1 LSB (10mV).The adjustment range is ±7 LSBs. For a detailed explanation of the Offset DAC, see section 4.6.

The next stage is the PGA. This is a programmable gain amplifier that changes the gain *at the pixel rate* to correct for gain errors due to PRNU, uneven illumination (such as $\cos^4$ effect), RGB filter mismatch, etc. The gain adjustment range is 0 to 6 dB (x1 to x2) with 7 bits of resolution. The gain data (correction coefficients) is provided on the CD0–CD6 bus. The gain may also be fixed at any value between 0 dB and 6 dB with the **PGA Gain Coefficient** configuration register. For further information on the PGA, see section 4.7.

An approximately 1 LSB (10mV) offset can be added at the output of the PGA stage if necessary to ensure that the offset is zero or positive. This eliminates the possibility of a negative offset clipping the darkest output pixels. For more information on the Offset Add Bit, see section 4.8.

Finally, the output of the PGA is digitized by the ADC and made available on the DD0–DD7 bus. For a detailed explanation of the ADC, see section 4.9.

Three reference voltages are used throughout the signal path: the externally supplied REF IN (1.225V), and the internally generated REF OUT_{MID} (2.45V) and REF OUT_{HI} (3.675V).

1.2 The CCD Clocking Signals

To maximize the flexibility of the LM9800, the CCD's ϕ1, ϕ2, RS, and TR pulses are internally generated, with a wide range of options, compatible with most commercial linear CCDs. In most cases, these output signals can drive most CCD clock inputs directly, with only series resistors (for slew rate control) between the LM9800's outputs and the CCD clock inputs.

1.3 The Digital Interface

There are three main sections to the digital interface of the LM9800: a serial interface to the Configuration Register, where all device programming is done, a 7 bit-wide input databus for gain correction coefficients with a synchronous clock output, and an 8-bit output databus for the final pixel output data with a synchronous $\overline{EOC}$ output signal and a $\overline{RD}$ input. Please note that $\overline{CS}$ affects only the serial I/O–it has no effect on the output databus, input coefficient bus, or any other section of the LM9800.

2.0 DIGITAL INTERFACE

2.1 Reading and Writing to the Configuration Register

Communication with the Configuration Register is done through a standard MICROWIRE™ serial interface. This interface is compatible with the Motorola SPI standard and is simple enough to easily be implemented in custom hardware if needed.

The serial interface timing is shown in *Figures 14, 15, 16, 17* and *Figures 19, 20, 21, 22*. **The SYNC pin must be pulled high to read or write to the configuration register.** Taking SYNC high resets the internal serial counters. Data is sent serially, LSB first. Input data is latched on the rising edge of SCLK, and output data changes on the falling edge of SCLK. $\overline{CS}$ must be low to enable serial I/O.

If SCLK is only clocked when sending or receiving data from the LM9800, and held low at all other times, then $\overline{CS}$ can be tied low permanently as shown in *Figures 14, 15, 16, 17*. If SCLK is continuous, then $\overline{CS}$ is used to determine the beginning and the end of a serial byte or word (see *Figures 19, 20, 21, 22*). Note that $\overline{CS}$ must make its high-to-low and low-to-high transitions when SCLK is low, otherwise the internal bit counter may receive an erroneous pulse, causing an error in the write or read operation.

Data may be transmitted and received in two 8-bit bytes (typical with microcontroller interfaces) or one 16-bit word (for custom serial controllers).

The Configuration Register is programmed by sending a control byte to the serial port. This byte indicates whether this is a read or a write operation, and gives the 3-bit address of the register bank to be read from or written to. If this is a read operation, the next 8 SCLKs will output the data at the requested location on the SDO pin. If this is a write operation, the data to be sent to the specified location should be clocked in on the SDI input during the next 8 SCLKs. Data is sent and received using the LSB (Least Significant Bit) first format.

Applications Information (Continued)

For maximum system reliability, each configuration register location can be read back and verified after a write.

If the serial I/O to the configuration register falls out of sync for any reason, it can be reset by a rising edge on the SYNC pin input.

2.2 Writing Correction Coefficient Data on the CD0–CD6 Bus

Correction coefficient data for each pixel is latched on the rising edge of the CCLK output signal (see *Figure 10*). Note that there is a 4 pixel latency between when the coefficient data is latched and when the output data is available. As *Figure 2*, **Pixel Pipeline Timing Overview** shows, coefficient data for pixel n is latched shortly before the output data for pixel n-2 becomes available on the output databus (DD0–DD7). *Figures 23, 24, 25, 26* show the timing for coefficient data and output data at the beginning of each line. Note that there is no way to provide a correction coefficient for pixel 1, the first pixel in the CCD array. This is usually not a problem since the first several pixels of most CCDs are not used. The timing at the beginning of a line is discussed in detail in section 2.4.

2.3 Reading Output Data on the DD0–DD7 Bus

The corrected digital output data representing each pixel is available on the DD0–DD7 databus. The data is valid after the falling edge of the $\overline{EOC}$ output. The $\overline{RD}$ input takes the databus in and out of TRI-STATE. $\overline{RD}$ can be held low at all times if there are no other devices needing the bus, or it can be used to TRI-STATE the bus between pixels, allowing other devices access to the bus. *Figure 12* shows how $\overline{EOC}$ can be tied to $\overline{RD}$ to automatically multiplex between coefficient data and conversion data.

2.4 $\overline{EOC}$ and CCLK at Startup

At the beginning of every line, the LM9800 internally synchronizes the $\overline{EOC}$ and CCLK signals with the user-programmed sample periods. The timing of $\overline{EOC}$ and CCLK during this adjustment period depends on the settings in the **RS Pulse Position** (RS) and **Sample Reference Position** (SR) registers, as shown in *Figures 23, 24, 25, 26*. The numbers inside the CCLK and $\overline{EOC}$ signals indicate the width (in MCLK periods) of that signal while it is in that state.

The EOC and CCLK pulse train is synchronized with the position of the Sample Reference pulse. For most RS and SR combinations (shown in table and timing of *Figure 23*), increasing SR simply stretches out the second $\overline{EOC}$ and CCLK cycle. When SR is greater than 10 (typically with even/odd CCDs), the timing gets more complex, and should be considered when building any systems that rely on the $\overline{EOC}$ and/or CCLK signals for counting, or expect them to never be low simultaneously.

2.5 MCLK

This is the master clock input that controls the LM9800. The pixel conversion rate is fixed at 1/8 of this frequency. Many of the timing parameters are also relative to the frequency of this clock.

2.6 SYNC

This input signals the beginning of a line. When SYNC goes high, the LM9800 generates a TR pulse, then begins converting pixels until the SYNC line is brought low again. Since there is no pixel counter in the LM9800, it will work with CCDs of any length.

SYNC must be high to read from or write to the Configuration Register. The rising edge of SYNC resets the serial I/O's internal shift register, so any noise or sporadic signals on the SCLK input prior to SYNC going high will be ignored.

3.0 DIGITAL CCD INTERFACE

3.1 Buffering ϕ1, ϕ2, RS, and TR

The LM9800 can drive the ϕ1, ϕ2, RS, and TR inputs of many CCDs directly, without the need for external buffers between the LM9800 and the CCD. Most linear CCDs designed for scanner applications require 0V to 5V signal swings into 20pF to 500pF input loading. Series resistors are typically inserted between the driver and the CCD to control slew rate and isolate the driver from the large load capacitances. The values of these resistors are usually given in the CCD's datasheet.

4.0 ANALOG INTERFACE

4.1 Voltage Reference

The two REF IN pins should be connected to a 1.225V ±2% reference voltage capable of sinking between 2mA and 8mA of current coming from the 400Ω–900Ω resistor string between REF OUT_{HI} and REF IN. The LM4041-1.2 1.225V bandgap reference is recommended for this application as shown in *Figure 28*. The inexpensive "E" grade meets all the requirements of the application and is available in a TO-92 (LM4041EIZ-1.2) package as well as a SOT-23 package (LM4041EIM3-1.2) to minimize board space.

Due to the transient currents generated by the LM9800's ADC, PGA, and CDS circuitry, the REF IN pins, the REF OUT_{MID} pin and the REF OUT_{HI} pin should all be bypassed to AGND with 0.1µF monolithic capacitors.

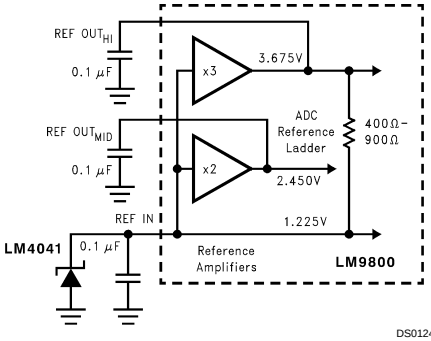


FIGURE 28. Voltage Reference Generation

4.2 Clamp Capacitor Selection

The output signal of most CCDs rides on a large DC offset (typically 8V to 10V) which is incompatible with the LM9800's 5V operation. To eliminate this offset without resorting to additional higher voltage components, the output of the CCD is AC coupled to the LM9800 through a DC blocking capacitor, C_{CLAMP} (the CCD's DOS output is not used). The value of this capacitor is determined by the leakage current of the

Applications Information (Continued)

LM9800's OS input and the output impedance of the CCD. The leakage through the OS input determines how quickly the capacitor value will drift from the clamp value of REF OUT_{MID}, which then determines how many pixels can be processed before the droop causes errors in the conversion (±0.1V is the recommended limit). The output impedance of the CCD determines how quickly the capacitor can be charged to the clamp value during the black reference period at the beginning of every line.

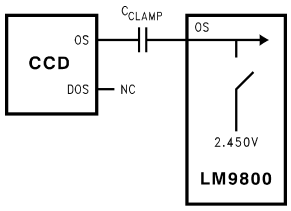


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FIGURE 29. OS Clamp Capacitor and Internal Clamp

The minimum clamp capacitor value is determined by the maximum droop the LM9800 can tolerate while converting one CCD line. The following equation takes the maximum leakage current into the OS input, the maximum allowable droop (100mV), the number of pixels on the CCD, and the pixel conversion rate (f_{MCLK}/8) and provides the minimum clamp capacitor value:

$$C_{CLAMP\ MIN} = \frac{i}{dV} dt$$

$$= \frac{\text{leakage current (A)}}{\text{max droop (V)}} \frac{\text{number of pixels}}{\text{conversion rate (Hz)}}$$

For example, if the OS input leakage current is 20nA worst-case, the CCD has 2200 active pixels, the conversion rate is 2.5MHz (f_{MCLK} = 20MHz), and the max droop desired is 0.05V, the minimum clamp capacitor value is:

$$C_{CLAMP\ MIN} = \frac{20nA}{0.05V} \frac{2200}{2.5MHz}$$

$$= 352pF$$

The maximum size of the clamp capacitor is determined by the amount of time available to charge it to the desired value during the optical black portion of the CCD output. The internal clamp is on for each pixel from the rising edge of the S/H ref pulse to the falling edge of the S/H signal pulse (see *Figures 7, 8*). This time can be calculated using the values stored in the Sample Signal and Sample Reference configuration registers and the MCLK frequency. For normal CCDs:

$$t_{DARK}(s) = \frac{2 + SS - SR}{2f_{MCLK}(Hz)}$$

And for even/odd CCDs:

$$t_{DARK}(s) = \frac{18 + SS - SR}{2f_{MCLK}(Hz)}$$

Where SS is the value in the Sample Signal Position register (0–15), SR is the value in the Sample Reference Position register (0–15), f_{MCLK} is the MCLK frequency, and t_{DARK} is the amount of time (per pixel) that the clamp is on.

The following equation takes the number of optical black pixels, the amount of time (per pixel) that the clamp is closed, the CCD's output impedance, and the desired accuracy of the final clamp voltage and provides the maximum clamp capacitor value:

$$C_{CLAMP\ MAX} = \frac{t}{R} \frac{1}{\ln(\text{accuracy})}$$

$$= \frac{n}{R_{OUT}(\Omega)} \frac{t_{DARK}(s)}{\ln(\text{accuracy})}$$

Where n = the number of optical black pixels, t_{DARK} is the amount of time (per pixel) that the clamp is on, R_{OUT} is the output impedance of the CCD, and accuracy is the ratio of the worst-case initial capacitor voltage to the desired final capacitor voltage. For example, if a CCD has 18 black reference pixels, the output impedance of the CCD is 1000Ω, the LM9800 is configured to clamp for 300ns, the worst case initial voltage across the capaoitor is 10V, and the desired voltage after clamping is 0.05V (accuracy = 10/0.05 = 200), then:

$$C_{CLAMP\ MAX} = \frac{18}{1000\Omega} \frac{300ns}{\ln(200)}$$

$$= 1020pF$$

The final value for C_{CLAMP} should be equal to or slightly less than $C_{CLAMP\ MAX}$, but no less than $C_{CLAMP\ MIN}$.

The LM9800 has been designed to work with most of the single output CCDs in use, but it is possible that some CCDs could have a combination of high output impedance and low optical black pixel count that would cause $C_{CLAMP\ MIN}$ to be greater than $C_{CLAMP\ MAX}$. In this case the LM9800 can be "short cycled" as shown in *Figure 30*, by bringing the sync pin low and then high again shortly after clamping the black reference pixels. This starts the line over, effectively increasing the number of black reference pixels, giving the capacitor more time to charge up through the output impedance of the CCD. This "short cycling" can be repeated as many times as necessary in order to guarantee that the capacitor is charged up to the required accuracy. Short cycling, if needed at all, is only necessary on power up and at the beginning of new scans where the OS coupling capacitor may have drooped since the previous scan. If the SYNC input is continuously being cycled at the line rate, short cycling is usually not necessary.

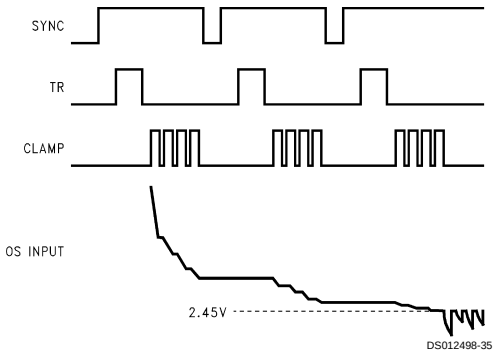

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FIGURE 30. Example of Short Cycling

Applications Information (Continued)

4.3 GAIN (VGA) Input

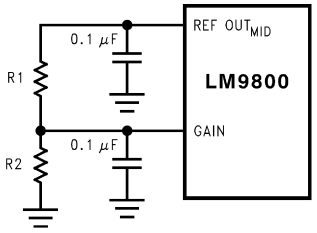
The LM9800 has a VGA (Variable Gain Amplifier) that can be used to increase the amplitude of the CCD signal prior to sampling, correction, and digitization. In a greyscale system, the VGA can provide gain for all the pixels. The VGA is activated or bypassed by setting or resetting the **VGA** bit in the configuration register. For greyscale systems using the VGA, the VGA bit and all 3 **Pixel Gain** bits (VGA_a, VGA_b, and VGA_c) should be set to "1".

The gain of the VGA is determined by the voltage on the GAIN input as given by the equation:

$$Gain_{VGA} = 1 + 2\left(\frac{V_{GAIN} + 0.12V}{REF\,OUT_{MID}}\right)\frac{V}{V}$$

Where V_{GAIN} is the voltage at the GAIN input of the LM9800. A detailed graph of this function is provided in the **Typical Performance Characteristics** section of the datasheet. This equation is accurate for the V_{GAIN} voltage range of 0.5V to 2.0V, corresponding to a gain range of x1.5 to x2.7 (typical).

The voltage at the GAIN input may be supplied by a resistive divider between $REF\,OUT_{HI}$ and AGND or by a voltage output DAC. The divider provides a low cost fixed gain suitable for many applications. The DAC allows fine, closed-loop adjustment of the gain which can eliminate system-to-system CCD gain and light source intensity variations to maximize dynamic range. The DAC0854 has the ideal output voltage range for this application and requires no additional external components.



Note : 10 kΩ ≤ R1 + R2 ≤ 50 kΩ

FIGURE 31. GAIN Control with Voltage Divider

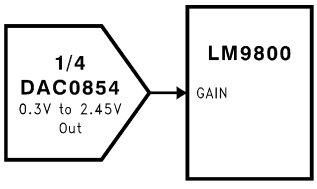


FIGURE 32. GAIN Control with DAC

If the VGA is not going to be used, the GAIN input should be tied to AGND.

4.4 Color Gain Switching

The VGA can also be used in color LM9800-based systems with sequential (serial) color CCD outputs (RGBRGBRGB. . .). Sequential RGB color CCDs typically have a Blue signal that is substantially lower (30%–70%) in amplitude than the Red and Green signals. The LM9800 can compensate for this by allowing the VGA to be turned on and off at the pixel rate, allowing each pixel in a three pixel triad to have one of two different gains (see *Figure 13*, VGA Gain Switching). When the VGA is bypassed, the gain through the VGA stage is 1. When the VGA is activated, the gain through the VGA stage is determined by the external voltage on the GAIN input. The Configuration Register controls whether or not gain switching is implemented, and which pixels are routed through the VGA.

Gain switching is controlled by the VGA On/Off bit and the three Pixel Gain bits in the Configuration Register. If the VGA On/Off bit is set to 0, then the VGA is bypassed (a gain of 1) for all pixels. If the VGA On/Off bit is set to 1, then the gain for each pixel inside every three pixel "triad" is set by the **VGA State for Pixel "n"** bits. For example, if the CCD output data is RGBRGBRGB, then the VGA state bits in the configuration register should be 001 (Pixel "a" = 0, Pixel "b" = 0, Pixel "c" = 1). The VGA would then be bypassed for the Red and Green pixels (for an effective gain of 1), and the Blue pixels would be routed through the VGA for amplification (as determined by the voltage on the GAIN input). Note that the VGA is always off (for an effective gain of 1) for the first pixel immediately following the last optical black pixel, regardless of the setting of the gain bit.

Other color configurations are described in section 5.0.

4.5 Correlated Double Sampler (CDS)

Figure 33 shows the output stage of a typical CCD and the resulting output waveform:

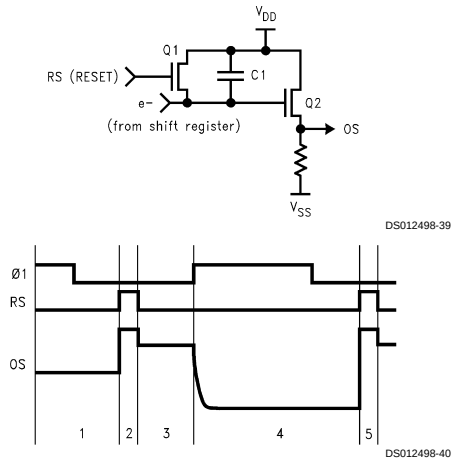


FIGURE 33. CDS

Capacitor C1 converts the electrons coming from the CCD's shift register to an analog voltage. The source follower output stage (Q2) buffers this voltage before it leaves the CCD. Q1 resets the voltage across capacitor C1 in between every pixel at intervals 2 and 5. When Q1 is on, the output signal (OS) is at its maximum. After Q1 turns off (period 3), the OS level represents the residual voltage across C1 ($V_{RESIDUAL}$). $V_{RESIDUAL}$ includes charge injection from Q1, thermal noise from the ON resistance of Q1, and other sources of error. When the shift register clock (ϕ1) makes a low to high transition (period 4), the electrons from the next pixel flow into C1. The charge across C1 now contains the voltage proportional to the number of electrons plus $V_{RESIDUAL}$, an error

Applications Information (Continued)

term. If OS is sampled at the end of period 3 and that voltage is subtracted from the OS at the end of period 4, the $V_{RESIDUAL}$ term is canceled and the noise on the signal is reduced. ($[V_{SIGNAL}+V_{RESIDUAL}]-V_{RESIDUAL} = V_{SIGNAL}$). This is the principal of Correlated Double Sampling.

The LM9800 implements CDS with two switched-capacitor S/H amplifiers. The S/Hs acquire a signal within a 50 ns window which can be placed anywhere in the pixel period with 25 ns precision. See *Figures 7, 8* for more detailed timing information.

4.6 Offset DAC

The offset DAC is used to compensate for DC offsets due to the correlated double sampling stage. The offset can be corrected in 15 steps of 1 LSB size between −7 LSB and +7 LSB. Note that the DAC comes betore the PGA, so any offset errors at this stage are multiplied by the gain of the PGA. The calibration procedure described in section 6.0 demonstrates how to use the DAC to eliminate offset errors before scanning begins.

Note that this DAC is programmed during LM9800 calibration/configuration and is not meant to compensate for pixel-to-pixel CCD offset errors. (CDS cancels the pixel-rate offset errors.)

4.7 Programmable Gain Amplifier (PGA)

The PGA provides 7 bits of pixel-to-pixel gain correction over a 0 dB to 6 dB (x1 to x2) range. After the input signal is sampled and held by the CDS stage, it is amplified by the gain indicated by the data (“PGA Code”) on the CD0–CD6 databus using the formula:

$$\text{Gain (dB)} = 20\log_{10}\left(1 + \frac{\text{PGA code}}{128}\right)$$

4.8 Offset Add Bit

In addition to the Offset DAC, there is a bit in the configuration register which, when set, adds a positive 1 LSB offset at the output of the PGA. This offset ensures that any offset between the output of the PGA and the ADC is positive, so that no dark level information is lost due to negative offsets. The calibration procedure described in section 6.0 demonstrates how to set this bit.

4.9 ADC

The ADC converts the normalized analog output signal to an 8-bit digital code. The $\overline{EOC}$ output goes from high to low to indicate that a new conversion is ready. ADC data can be latched by external memory on the rising edge of $\overline{EOC}$. The $\overline{RD}$ input takes the ADC's output buffer in and out of TRI-STATE. $\overline{RD}$ may be tied to $\overline{EOC}$ in many applications, putting the data on the bus only when EOC is low, and allowing other data on the bus (such as CD0–CD6 correction data) at other times. In this way the output data and correction coefficient data can share the same databus (see *Figure 12*).

4.10 I_{SET} Input

This input is used to set internal bias currents inside the LM9800. It should be tied to V_A through a 75kΩ resistor.

5.0 COLOR

There are several ways to apply the LM9800 in a color system:

5.1 Sequential RGB Output CCD

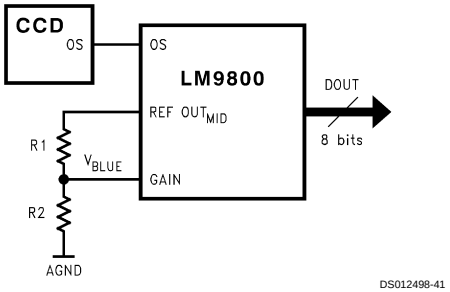


FIGURE 34. Sequential RGB Output CCD

The solution shown in *Figure 34* provides a 2.5Mpixels/sec (830k RGB pixels/sec) pixel rate using a single LM9800 and no additional external components. It requires a sequential RGB output CCD, and provides inexpensive color at the expense of some resolution and registration.

5.2 Parallel Output CCD, One LM9800

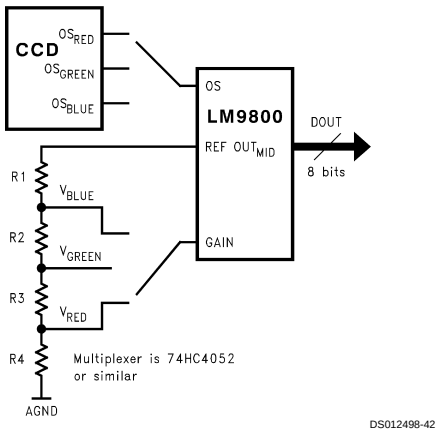


FIGURE 35. Parallel Output CCD, One LM9800

Figure 35 gives an example of how to use a single LM9800 with a triple-output RGB CCD. In this case an entire line of red is digitized, followed by an entire line of green, then blue. This solution provides the same 2.5Mpixels/sec (for an effective 830k RGB pixels/sec after de-interleaving) pixel rate as the previous solution but uses a higher performance color CCD. The multiplexers select the color to be digitized and the resistor tap voltage corresponding to the desired gain for that color. The resistor ladder and its multiplexer can be replaced with a voltage output DAC (such as the DAC0854) for precision digital control of the gain for each color. Almost any multiplexer can be used since the multiplexer switches at the line rate, not the pixel rate, and goes into a high impedance input. The 74HC4052 is a good choice.

Applications Information (Continued)

5.3 Parallel Output CCD, Three LM9800s

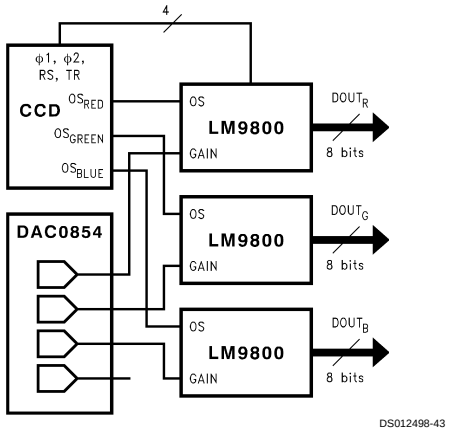


FIGURE 36. Parallel Output CCD, Three LM9800s

Figure 36 uses three LM9800s to achieve a 7.5Mpixel/sec (2.5M RGB pixels/sec) pixel rate. The three LM9800s are synchronized by applying the same MCLK and SYNC signals to all three devices. One LM9800 provides the clock signals required for the CCD. Since the coefficient data for all three LM9800s will be latched simultaneously on the rising edge of CCLK, the correction coefficient bus should either be at least 21 bits wide (7 correction coefficient bits by 3 LM9800s) or run at a 7.5MHz rate and latched into a buffer between the correction coefficient databus and each LM9800. Similarly, the output data for all three LM9800s will be available simultaneously at the 3 output databusses.

6.0 CALIBRATION

To calibrate a LM9800-based system, follow these steps:

6.1 Offset Calibration

This procedure corrects for offsets generated inside the LM9800. Because the LM9800 uses CDS to eliminate the pixel-to-pixel offset errors of the CCD, very good results can be obtained even if this procedure is not implemented. In this case the Offset DAC and Offset Add bit are simply set to 0.

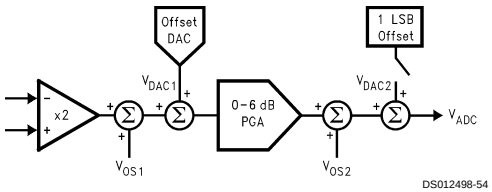


FIGURE 37. Offset Calibration

To use the Offset DAC and Offset Add bit for offset correction, the offset errors must first be determined. This is done be measuring the voltage at the PGA output, using the ADC. If this voltage is known with a PGA gain of x1 (0 dB) and x2 (6 dB), then the offset errors (V_{OS1} and V_{OS2}) can be determined from the following two equations:

$V_{ADC1} = 1(V_{OS1} + V_{DAC1}) + V_{OS2} + V_{DAC2}$
(PGA gain = x1)

$V_{ADC2} = 2(V_{OS1} + V_{DAC1}) + V_{OS2} + V_{DAC2}$
(PGA gain = x2)

Solving for V_{OS1} and V_{OS2}:

$V_{OS1} = (V_{ADC2} – V_{ADC1}) – V_{DAC1}$

$V_{OS2} = (2V_{ADC1} – V_{ADC2}) – V_{DAC2}$

These equations were used to produce this procedure for cancelling the LM9800's offset errors:

1. Turn off the VGA.
2. Set the Offset DAC to +7 LSB. (This is done to ensure the total offset is positive and therefore measurable by the ADC.)
3. Set the Offset Add bit to 0.
4. Set the PGA Gain to x1 (PGA code = 0).
5. Digitize a black line.
6. Calculate the average (in ADC LSBs) of all the valid pixels in the black line and store that number as "B1" (equivalent to V_{ADC1}).
7. Set the PGA Gain to x2 (PGA code = 127).
8. Digitize a black line.
9. Calculate the average (in ADC LSBs) of all the valid pixels in the black line and store that number as "B2" (equivalent to V_{ADC2}).
10. Program the Offset DAC using the formula:
    Offset DAC code = 7+B1–B2.
11. If 2B1 > B2, then set the Offset Add bit to 0. If 2B1 < B2, set the Offset Add bit to 1.

6.2 Coarse Gain Calibration

The LM9800's PGA corrects for up to 6 dB of varIation in the CCD output signal's white level intensity. That 6 dB range has to be centered inside the 6 dB window of correction.

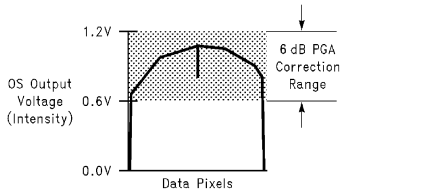


FIGURE 38. CCD Input Signal In Range

With the VGA off and the PGA set to a gain of 0 dB, the LM9800 expects the maximum CCD white level output to be below 1.2V ($V_{REF\ IN}$) corresponding to strong pixels, and the minimum white level output voltage to be above 0.6V ($V_{REF\ IN}/2$), corresponding to weaker CCD pixels or pixels further from the light source. If the variation for a white input is inside this range, as shown in *Figure 38*, the PGA can correct for it and linearize it.

If the maximum white level voltage (the voltage from the strongest pixels) is greater than 1.2V *(Figure 39)*, the LM9800 will be unable to linearize the CCD's output.

Applications Information (Continued)

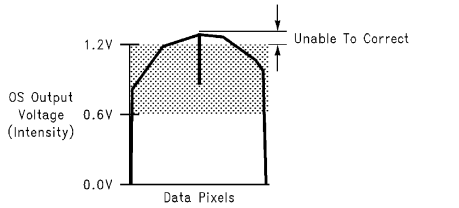


FIGURE 39. CCD Input Signal Too Strong

In this case it is necessary to decrease the maximum amplitude of the CCD output. Typically this is done by reducing the light source intensity, or decreasing the light integration time of the CCD.

If the minimum white level output voltage (the voltage from the weakest pixels) is less than 0.6V, then a similar situation occurs, as shown in *Figure 40*.

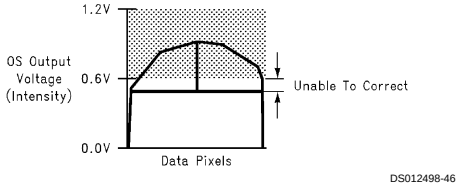


FIGURE 40. CCD Input Signal Too Weak

In this case the amplitude for some of the weak pixels is too low, and cannot be corrected for by the 6 dB PGA alone. The amplitude of the CCD's output signal must be increased. This can be accomplished by increasing the intensity of the light source, increasing the integration time of the CCD, or using the LM9800's VGA feature to add gain to the signal prior to the PGA.

If the minimum white level is less than 0.6V and the maximum white level is greater than 1.2V, then the LM9800 cannot correct for this amount of pixel-to-pixel variation — the variation is greater than 6dB *(Figure 41)*. In this case the system should be examined and steps taken to bring the variation within a 6dB window. Typically this can be done by using more even illumination, higher quality CCDs, or better optics.

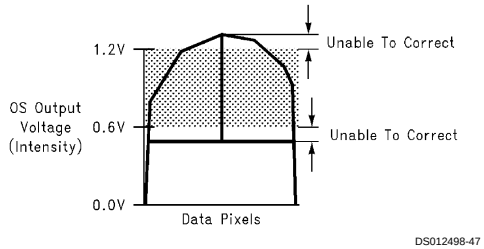


FIGURE 41. CCD Input Signal Range Too Wide

The coarse gain calibration procedure follows. In scanner systems with low unit-to-unit variations in light intensity and CCD efficiency, this calibration can be done once and fixed for all the systems. Other systems, where the light intensity varies from unit-to-unit or the pixel-to-pixel variation is very close to 6dB, should do this procedure for every system, either once during manufacture or as part of the calibration routine the scanner does on power-up or before a scan.

1. Set the PGA gain to 0dB.
2. If using the VGA, turn it on and set the gain voltage to provide the approximate gain required.
3. If not using the VGA, turn it off.
4. Scan a reference line corresponding to the maximum white input the scanner should ever have to digitize.
5. Find the minimum and the maximum (in ADC LSBs) of the valid pixels in the reference line.
6. The reference line should correspond to a desired output code. For example, if the reference is 100% white, the desired output code might be 240 LSBs. If the reference was 80% white (light grey), then the desired output code might be (240)(0.8) = 192. If the maximum code obtained after scanning the reference line is less than the desired output code, and the minimum output code is greater than half the desired output code, the signal is in range. Go to section 6.3.
7. If the maximum code obtained after scanning the reference line is greater than the desired output code, and the minimum output code is less than half the desired output code, then there is more than 6dB of variation on the input signal and the LM9800 will not be able to correct for the variations. The pixel-to-pixel variation must be reduced to less than 6dB before the LM9800 can correct for variations.
8. If the maximum code obtained after scanning the reference line is greater than the desired output code for that reference, the CCD output is too large. Reduce the light intensity, shorten the integration time, or (if using the VGA) reduce the voltage on the GAIN input. Go back to Step 4.
9. If the minimum code obtained after scanning the reference line is smaller than half the desired output code for that reference, the CCD output is too weak. Increase the light intensity, lengthen the integration time, or (if using the VGA) increase the voltage on the GAIN input. Go back to Step 4.

6.3 PGA Correction Coefficients (Shading Calibration)

Once the input signal has been centered inside the range the LM9800 can correct for, correction coefficients must be generated for each pixel to compensate for the gain error of that pixel.

1. Set the PGA gain to 0dB.
2. If using the VGA, turn it on and set the gain voltage to provide the required gain (determined by the procedure in Section 6.2).
3. If not using the VGA, turn it off (set the VGA On/Off bit to "0").
4. Scan a reference line corresponding to all white or light grey and store it in memory.
5. Calculate the required gain correction coefficients for each pixel using the formula:

$$\text{Correction Coefficient}_n = 128\left(\frac{\text{Desired Code}}{\text{Uncorrected Code}_n} - 1\right)$$

Where **Uncorrected Code$_n$** is the ADC output code for pixel *n* with the PGA gain = 0dB, **Desired Code** is the number that corresponds to the desired output from the ADC with the given reference line input, and **Correction Coefficient$_n$** is

Applications Information (Continued)

the gain correction number that is sent to the CD0–CD6 correction databus to provide gain correction for pixel *n* when digitizing a line with the LM9800's PGA gain correction operating.

All the Correction Coefficients must be stored and sent to the LM9800 through the CD0–CD6 databus for every line scanned.

7.0 POWER SUPPLY CONSIDERATIONS

7.1 General

The LM9800 should be powered by a single +5V source (unless 3V-compatible digital I/O is required — see section 7.2). The analog supplies (V_A) and the digital supplies (V_D and $V_{D(I/O)}$) are brought out individually to allow separate bypassing for each supply input. They should *not* be powered by two or more different supplies.

In systems with separate analog and digital +5V supplies, all the supply pins of the LM9800 should be powered by the cleaner analog +5V supply. Each supply input should be bypassed to its respective ground with a 0.1µF capacitor located as close as possible to the supply input pin. A single 10µF tantalum should be placed near the V_A supply pin to provide low frequency bypassing.

To minimize noise, keep the LM9800 and all analog components as far as possible from noise generators, such as switching power supplies and high frequency digital busses. If possible, isolate all the analog components and signals (OS, GAIN, reference inputs and outputs, VA, AGND, I_{SET}) on an analog ground plane, separate from the digital ground plane. The two ground planes should be tied together at a single point, preferably the point where the power supply enters the PCB.

7.2 3V Compatible Digital I/O

If 3V digital I/O operation is desired, the $V_{D(I/O)}$ pin may be powered by a separate 3V ± 10% or 3.3V ± 10% supply. In this case all the digital I/O pins (CD0–CD6, CCLK, MCLK, DD0–DD7, $\overline{EOC}$, $\overline{RD}$, SYNC, $\overline{CS}$, SCLK, SDO, and SDI) will be 3V compatible. (The CCD clock signals (ϕ1, ϕ2, RS, and TR) remain 5V outputs, powered by V_D.) In this case the $V_{D(I/O)}$ input should be bypassed to $DGND_{(I/O)}$ with a parallel combination of a 0.1µF capacitor and a 10µF tantalum capacitor.

7.3 Power Down Mode

Setting the Power Down bit to a "1" puts the device in a low power standby mode. The CCD outputs (ϕ1, ϕ2, RS, and TR) are pulled low and the analog sections are turned off to conserve power. The digital logic will continue to operate if MCLK continues and SYNC is held high, so for minimum power dissipation MCLK should be stopped when the LM9800 enters the Power Down mode. Recovery from Power Down typically takes 50µs (the time required for the reference voltages to settle to 0.5 LSB accuracy).

8.0 TYPICAL APPLICATION

Figure 42 shows the interface between the LM9800 and a typical even/odd output CCD, the TCD1250. The interface for most other CCDs will be similar, the only differences being the values for the clamp capacitor and the values for the series resistors, if needed. The clamp capacitor value is determined as shown in section 4.2. The resistor values are usually given in the CCD's datasheet. If the datasheet's requirement is given as a particular rise/fall time, the resistor can be chosen using the graph of **ϕ1, ϕ2, RS and TR Rise Times Through A Series Resistance vs. Load Capacitance** graph in the **Typical Performance Characteristics**

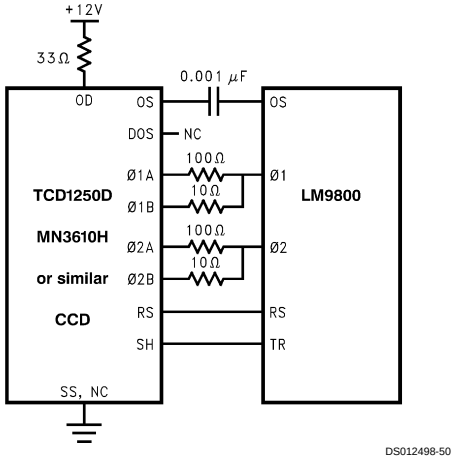


FIGURE 42. CCD Interface Example

section. Given the required rise time and the input capacitance of the input being driven, the resistor value can be estimated from the graph.

Table 3 shows the Configuration Register parameters recommended for use as a starting point for most even/odd CCDs. The Mode is set to Even/Odd, RS Pulse Width is set to its minimum value, and RS polarity is positive. The timing, shown in *Figure 43*, is determined by the RS, SR, and SS registers. The RS pulse position (RS) is set to 10, dividing the pixel period so that the *signal* portion is available for the first 5 MCLKs following a ϕ1 clock edge and the *black reference* portion appears during the last 2 MCLKs (following the 1 MCLK wide reset pulse). Sample Reference (SR) is set to 14, so it samples the black reference just before the next ϕ1 clock edge. Sample Signal (SS) is set to 8, so it samples the black reference just before the next reset pulse. These values can be adjusted to account for differences in CCDs, CCD data delays, settling time, etc., but this is often not necessary.

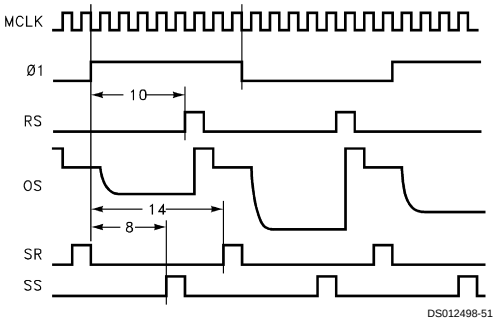


FIGURE 43. Typical Even/Odd Timing

Applications Information (Continued)

All 4 digital outputs (ϕ1, ϕ2, RS, and TR) are enabled. The TR pulse width is set to the minimum, 20 MCLKs, as is the guardband between ϕ1 and TR. Either of these settings can be increased if necessary.

The TR polarity is positive, as is the RS polarity. Some CCDs may require one or both of these signals to be inverted, in which case the corresponding bit can be set to a "1". If there is an inverting buffer between the LM9800 and the CCD, these bits can be also used to correct the output polarity at the CCD. Note that if ϕ1 and ϕ2 are inverted, then $\overline{\phi 2}$ should be used as ϕ1 at the CCD, and $\overline{\phi 1}$ should be used as ϕ2 at the CCD *(Figure 44).*

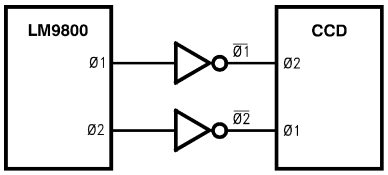


FIGURE 44. ϕ1 and ϕ2 After Inversion

The number of dummy pixels and optical black reference pixels are given in the CCD's datasheet. The dummy pixel register should be programmed with the number of dummy pixels in the CCD + 1 (for example, if the CCD has 16 dummy pixels then the register should contain 17). The optical black reference register should be programmed with the number of optical black pixels in the CCD.

The PGA gain coefficient register and PGA Gain Source bit are used during calibration (see section 6.0). The Power Down bit should be set to 0 for normal operation. The Offset Add bit is also programmed durIng calibration.

The VGA settings should be all zeros (0 0 0 0) if the VGA is not going to be used, or all ones (1 1 1 1) if the VGA will be used to provide additional input signal gain. If using a sequential color CCD, see section 4.4).

The Offset DAC bits are programmed during calibration (section 6.0). The Test Mode bits should always be set to "0".

9.0 HINTS AND COMMON SYSTEM DESIGN PROBLEMS

9.1 Reading and Writing to the Configuration Register

The Configuration Register sends and receives data LSB (Least Significant Byte) first. Some microcontrollers send out data MSB (Most Significant Byte) first.

The SYNC pin must be high to send/receive data to/from the Configuration Register.

9.2 Examine the CCLK and EOC Timing

As explained earlier, this timing depends on the position of the Sample Reference (SR) pulse, and for some values of SR it is not what you would expect. Pay close attention to Timing Diagrams (*Figures 23, 24, 25, 26*).

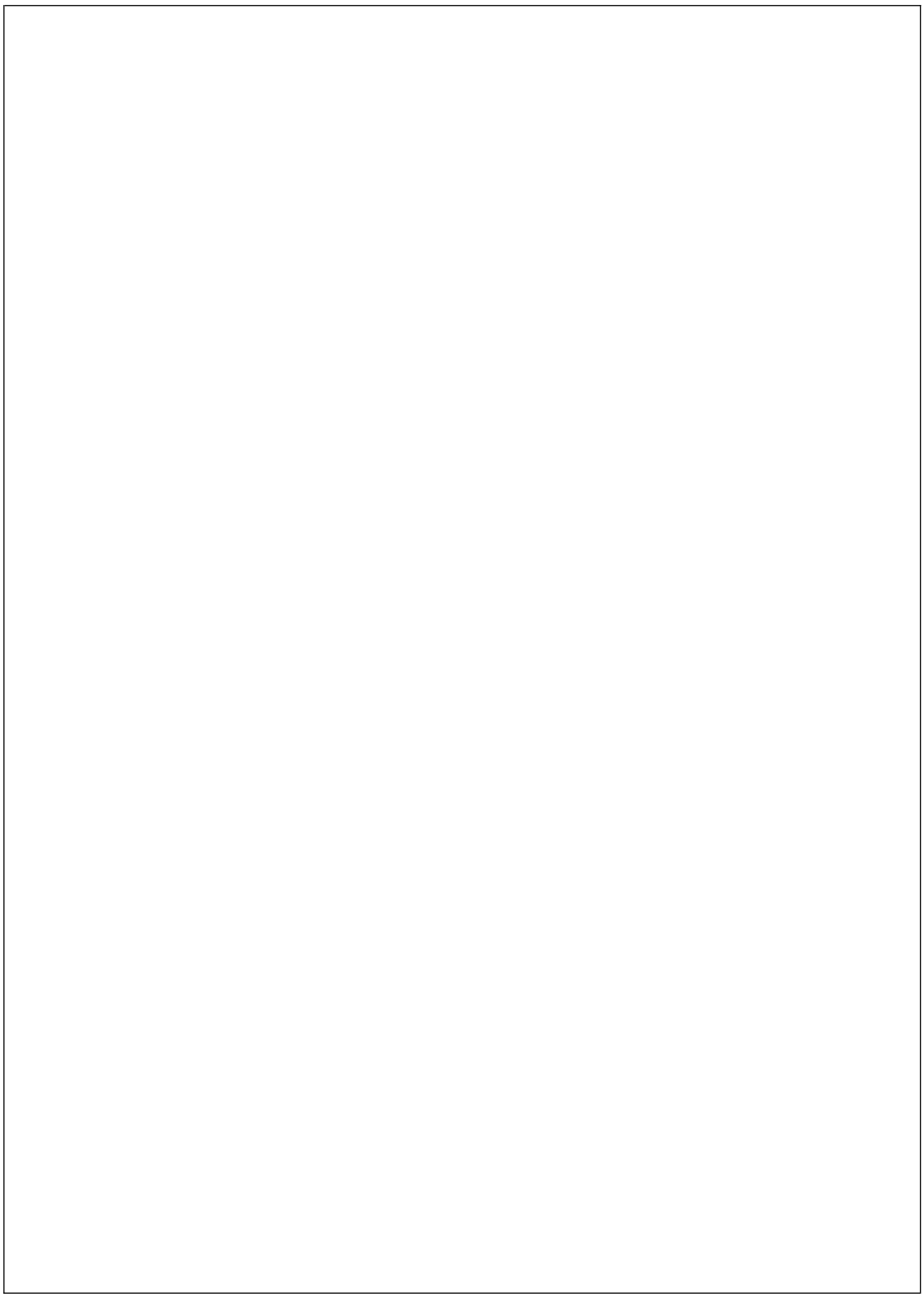
9.3 Setting the Dummy and Optical Black Pixel Registers

The minimum value in the Dummy Pixels register is 1. Note that the value in this register should be equal to 1 plus the actual number of dummy pixels in the CCD. For example, if the CCD being used with the LM9800 has 12 dummy pixels, this register should be set to 13. The minimum number in the Optical Black Pixels register is 1.

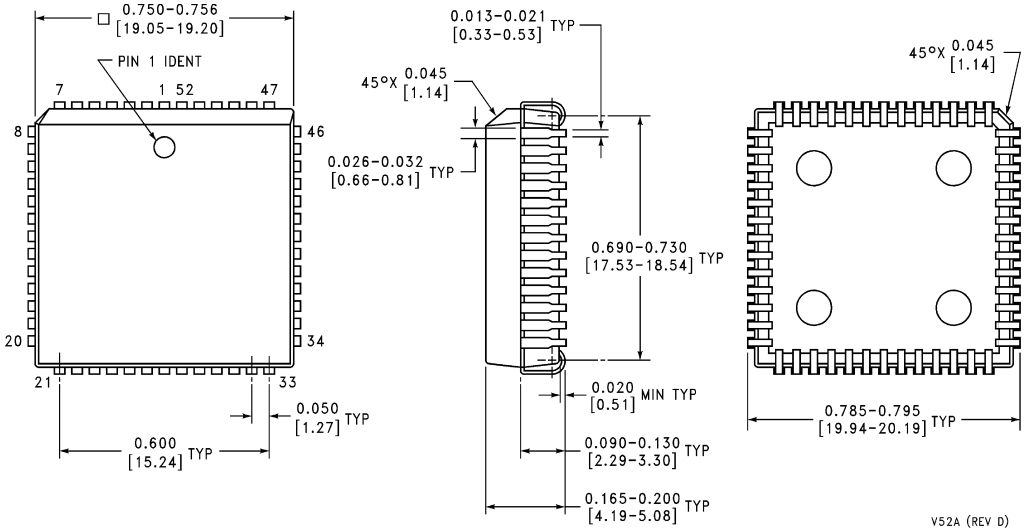
Applications Information (Continued)

TABLE 3. Configuration Register Example Data

A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Standard Mode or Even/Odd Mode	RS Pulse Width		RS Pulse Polarity	RS Pulse Position (Minimum Value is 1)			
			1	0	0	0	1	0	1	0
0	0	1	Sample Reference Position				Sample Signal Position			
			1	1	1	0	1	0	0	0
0	1	0	ϕ1 Enable	ϕ2 Enable	RS Enable	TR Enable	TR Pulse Width		TR–ϕ1 Guardband	TR Polarity
			1	1	1	1	0	0	0	0
0	1	1	Dummy Pixels (Minimum Value is 1)							
			Set to 1 + Number of Dummy Pixels Given in CCD Datasheet							
1	0	0	Optical Black Pixels (Minimum Value is 1)							
			Set to Number of Optical Black Pixels Given in CCD Datasheet							
1	0	1	PGA Gain Coefficient							
			0	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0
1	1	0	PGA Gain Source	Test Mode	Power-down	Offset Add	VGA On/Off	VGA State Pixel c	VGA State Pixel b	VGA State Pixel a
			PGASRC	0	0	OFFADD	0 1	0 1	0 1	0 1
1	1	1	Offset DAC Sign	Offset DAC MSB	Offset DAC	Offset DAC LSB	Test Modes			
			ODSIGN	VOS2	VOS1	VOS0	0	0	0	0



Physical Dimensions inches (millimeters) unless otherwise noted



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