



November 1994

LMC6022

Low Power CMOS Dual Operational Amplifier

General Description

The LMC6022 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V^- , low input bias current, and voltage gain (into 100k and 5 k Ω loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6024 datasheet for a CMOS quad operational amplifier with these same features.

Features

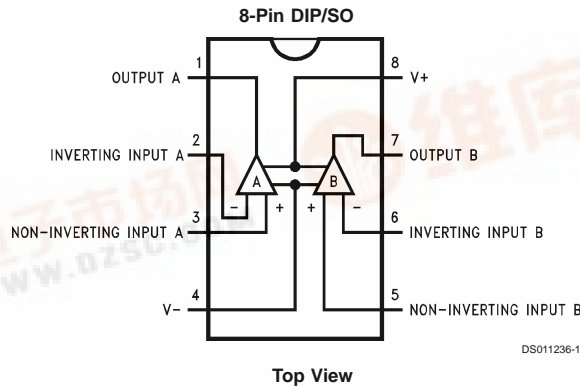
- Specified for 100 k Ω and 5 k Ω loads
- High voltage gain: 120 dB
- Low offset voltage drift: 2.5 $\mu\text{V}/^\circ\text{C}$

- Ultra low input bias current: 40 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- Low distortion: 0.01% at 1 kHz
- Slew rate: 0.11 V/ μs
- Micropower operation: 0.5 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram



Ordering Information

Temperature Range	Package	NSC Drawing	Transport Media
Industrial $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$			
LMC6022IN	8-Pin Molded DIP	N08E	Rail
LMC6022IM	8-Pin Small Outline	M08A	Rail Tape and Reel

LMC6022 Low Power CMOS Dual Operational Amplifier



Absolute Maximum Ratings (Note 1)

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	1000V
Voltage at Output/Input Pin	(V^+) +0.3V, (V^-) -0.3V
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)

Current at Input Pin	±5 mA
Output Short Circuit to V^-	(Note 2)
Output Short Circuit to V^+	(Note 12)

Operating Ratings

Temperature Range	-40°C ≤ T_J ≤ +85°C
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Bold-face** limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 11	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		$\mu V/^\circ C$
I_B	Input Bias Current		0.04	200	pA max
I_{OS}	Input Offset Current		0.01	100	pA max
R_{IN}	Input Resistance		>1		Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 12V$ $V^+ = 15V$	83	63 61	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \leq V^+ \leq 15V$	83	63 61	dB min
-PSRR	Negative Power Supply Rejection Ratio	$0V \leq V^- \leq -10V$	94	74 73	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & $15V$ For CMRR ≥ 50 dB	-0.4	-0.1 0	V max
			$V^+ - 1.9$	$V^+ - 2.3$ $V^+ - 2.5$	V min
A_V	Large Signal Voltage Gain	$R_L = 100$ k Ω (Note 7) Sourcing Sinking	1000	200 100	V/mV min
			500	90 40	V/mV min
		$R_L = 5$ k Ω (Note 7) Sourcing Sinking	1000	100 75	V/mV min
			250	50 20	V/mV min

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Bold-face** limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 100\text{ k}\Omega$ to 2.5V	4.987	4.40 4.43	V min
			0.004	0.06 0.09	V max
		$V^+ = 5V$ $R_L = 5\text{ k}\Omega$ to 2.5V	4.940	4.20 4.00	V min
			0.040	0.25 0.35	V max
		$V^+ = 15V$ $R_L = 100\text{ k}\Omega$ to 7.5V	14.970	14.00 13.90	V min
			0.007	0.06 0.09	V max
		$V^+ = 15V$ $R_L = 5\text{ k}\Omega$ to 7.5V	14.840	13.70 13.50	V min
			0.110	0.32 0.40	V max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$ Sinking, $V_O = 5V$ (Note 2)	22	13 9	mA min
			21	13 9	mA min
		$V^+ = 15V$ Sourcing, $V_O = 0V$ Sinking, $V_O = 13V$ (Note 12)	40	23 15	mA min
			39	23 15	mA min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	86	140 165	μA max

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.11	0.05 0.03	V/ μ s min
GBW	Gain-Bandwidth Product		0.35		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		nV/ \sqrt{Hz}
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		pA/ \sqrt{Hz}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of $150^\circ C$. Output currents in excess of ± 30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. $V^+ = 15V$ and $R_L = 100$ k Ω connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 13$ V_{PP}.

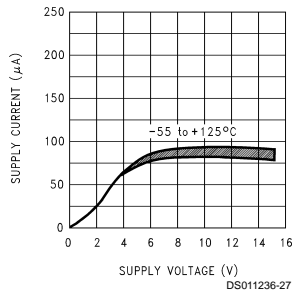
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

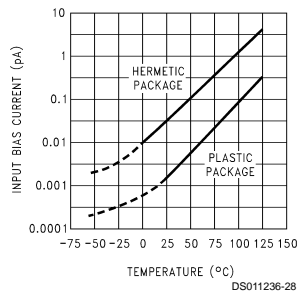
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified

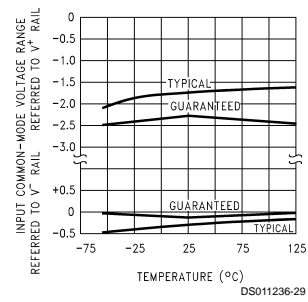
Supply Current vs Supply Voltage



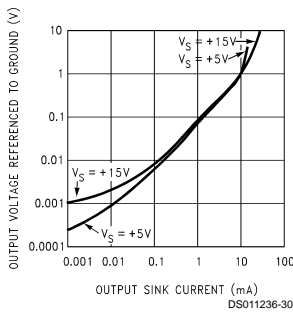
Input Bias Current vs Temperature



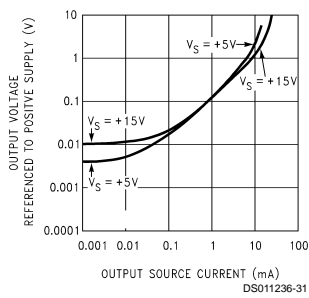
Input Common-Mode Voltage Range vs Temperature



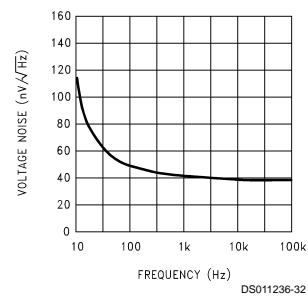
Output Characteristics Current Sinking



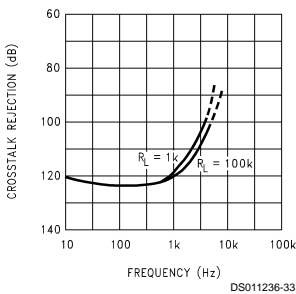
Output Characteristics Current Sourcing



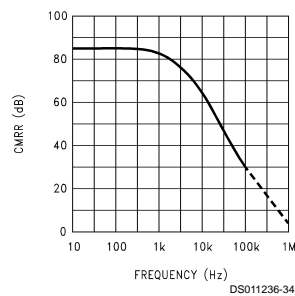
Input Voltage Noise vs Frequency



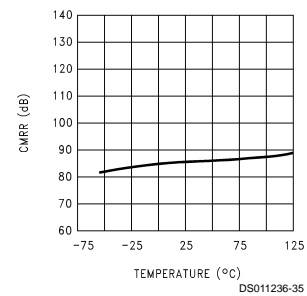
Crosstalk Rejection vs Frequency



CMRR vs Frequency

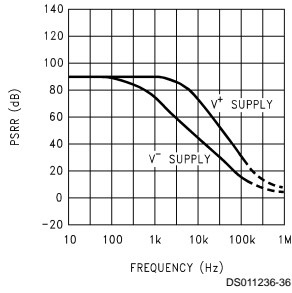


CMRR vs Temperature

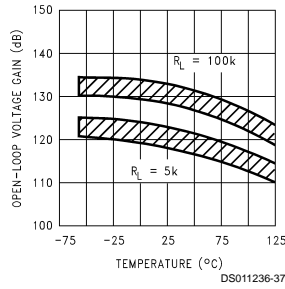


Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

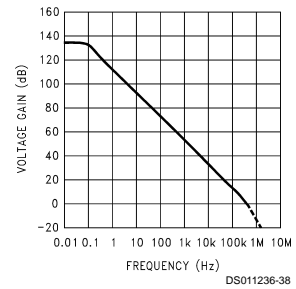
Power Supply Rejection Ratio vs Frequency



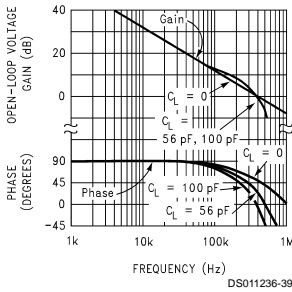
Open-Loop Voltage Gain vs Temperature



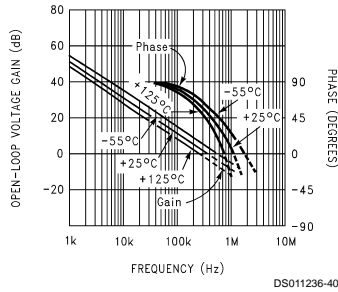
Open-Loop Frequency Response



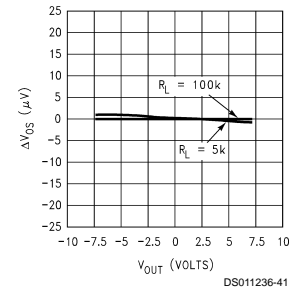
Gain and Phase Responses vs Load Capacitance



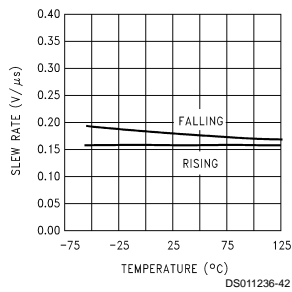
Gain and Phase Responses vs Temperature



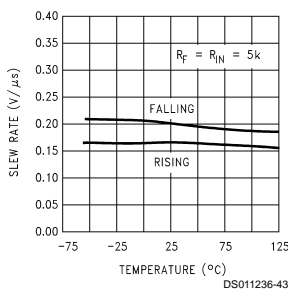
Gain Error (V_{OS} vs V_{OUT})



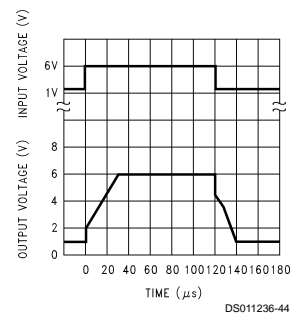
Non-Inverting Slew Rate vs Temperature



Inverting Slew Rate vs Temperature

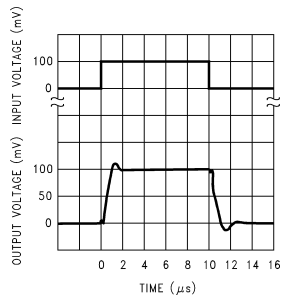


Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



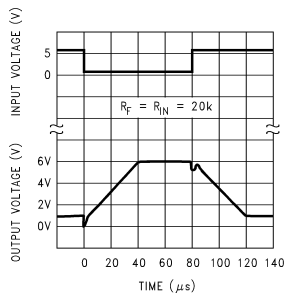
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

Non-Inverting Small Signal Pulse Response ($A_V = +1$)



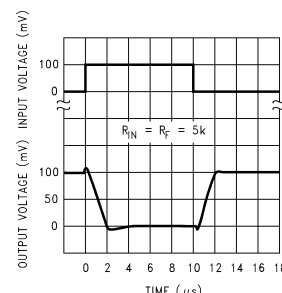
DS011236-45

Inverting Large-Signal Pulse Response



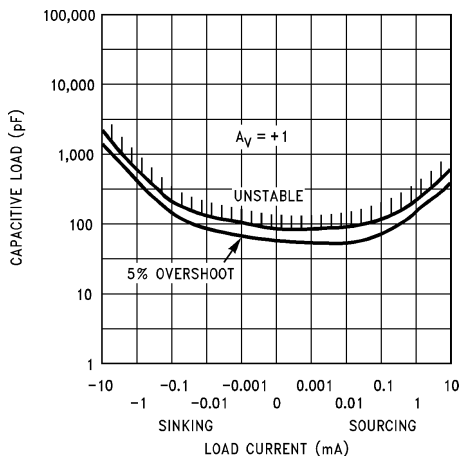
DS011236-46

Inverting Small-Signal Pulse Response



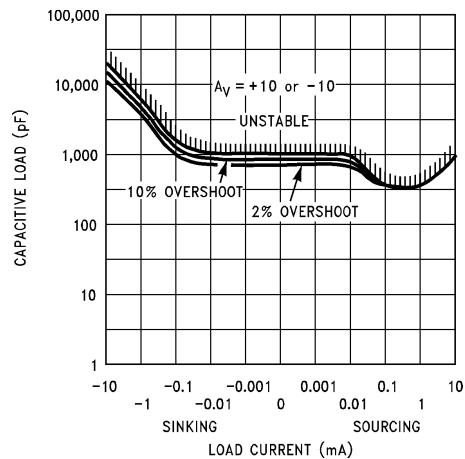
DS011236-47

Stability vs Capacitive Load



DS011236-4

Stability vs Capacitive Load



DS011236-5

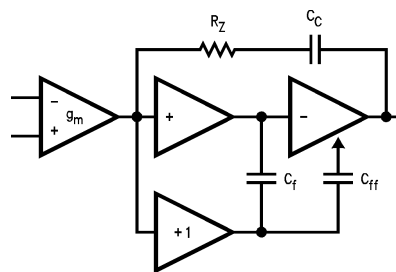
Note: Avoid resistive loads of less than 500Ω , as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6022 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



DS011236-6

FIGURE 1. LMC6022 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least $5k\Omega$. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driv-

Application Hints (Continued)

ing load resistance of 5 k Ω or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500 Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6022 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50 Ω to 100 Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

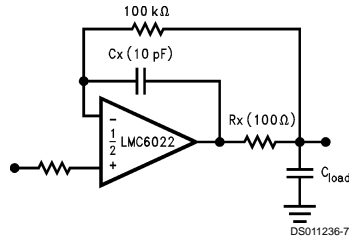


FIGURE 2. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V⁺ (Figure 3). Typically a pull up resistor conducting 50 μ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be de-

termined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

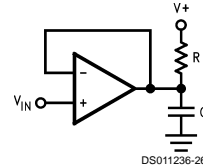


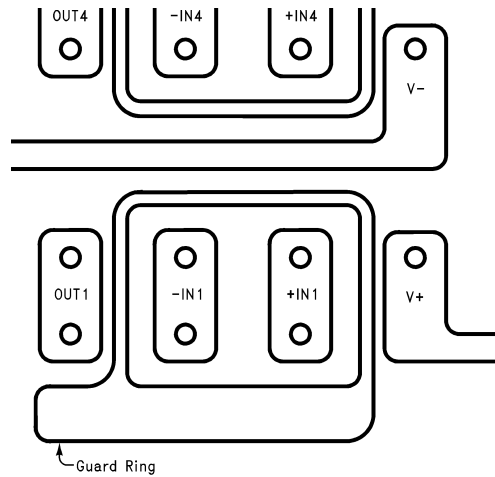
FIGURE 3. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6022, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

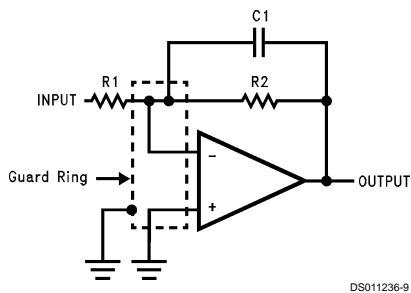
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6022's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 4. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10¹² Ω , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6022's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10¹¹ Ω would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 5a, Figure 5b, Figure 5c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 5d.

Application Hints (Continued)



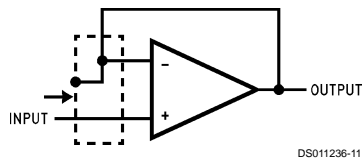
DS011236-8

FIGURE 4. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)



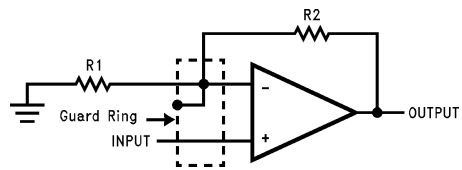
DS011236-9

(a) Inverting Amplifier



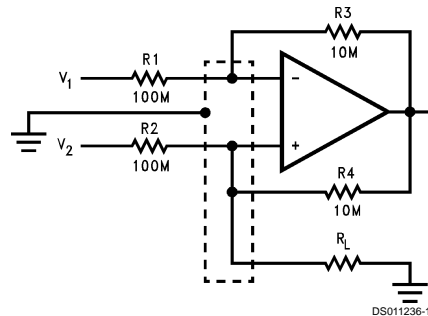
DS011236-11

(c) Follower



DS011236-10

(b) Non-Inverting Amplifier



DS011236-12

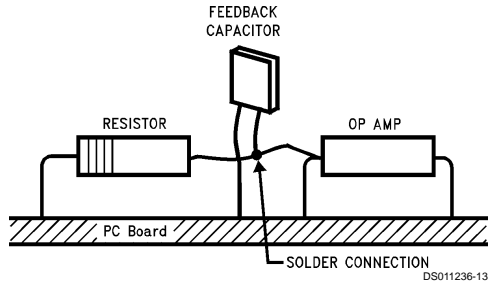
(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board con-

struction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 6.

Application Hints (Continued)



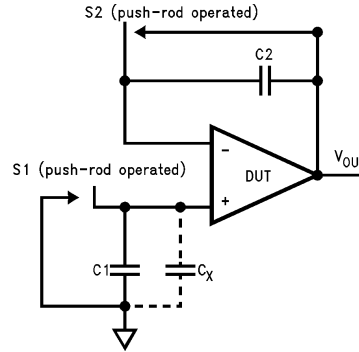
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$



DS011236-14

FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^- , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

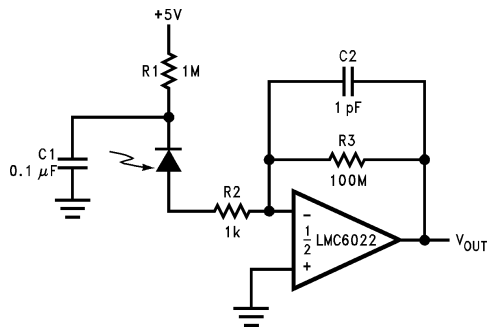
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

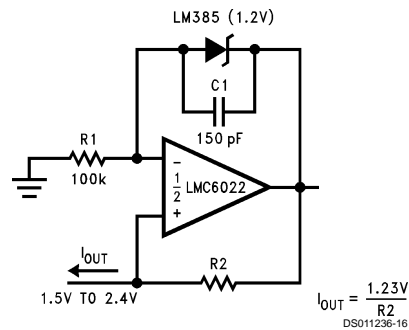
Photodiode Current-to-Voltage Converter



DS011236-15

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Micropower Current Source



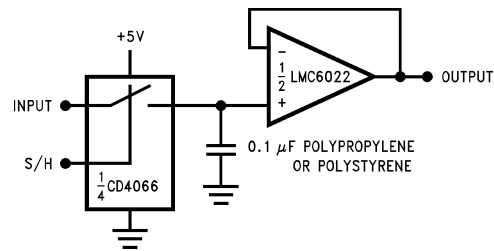
$$I_{OUT} = \frac{1.23V}{R2}$$

DS011236-16

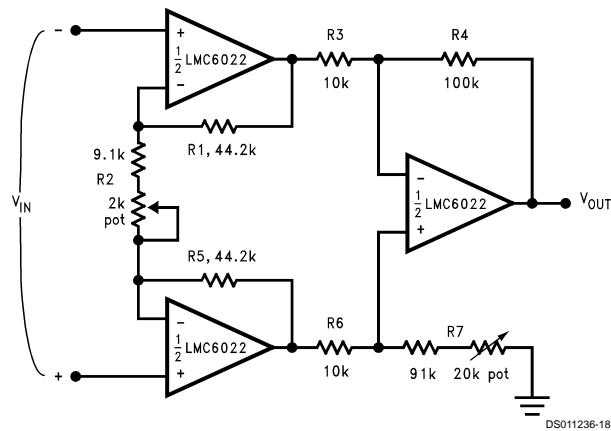
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Typical Single-Supply Applications (V₊ = 5.0 V_{DC}) (Continued)

Low-Leakage Sample-and-Hold



Instrumentation Amplifier



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$;
Then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

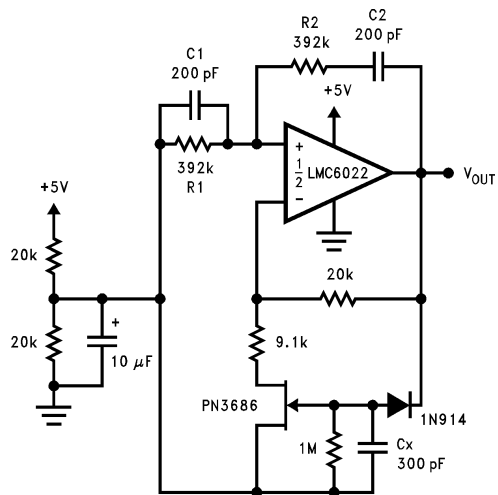
$\therefore A_v = 100$ for circuit shown

For good CMRR over temperature, low drift resistors should be used. Matching of R_3 to R_6 and R_4 to R_7 affects CMRR. Gain may be adjusted through R_2 . CMRR may be adjusted through R_7 .

Typical Single-Supply Applications

(V+ = 5.0 V_{DC}) (Continued)

Sine-Wave Oscillator



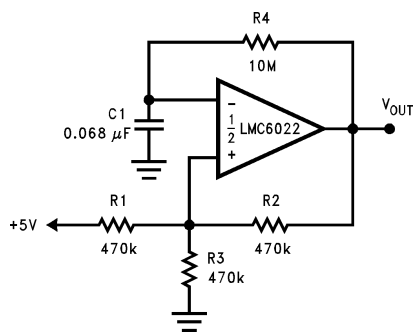
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{\text{OSC}} = 1/2\pi RC$$

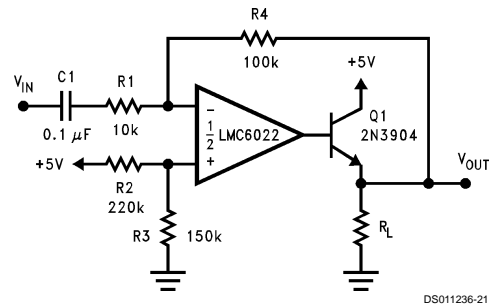
where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator

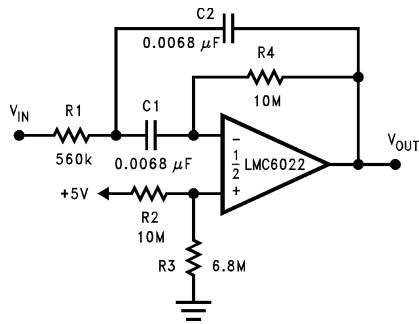


Power Amplifier



Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

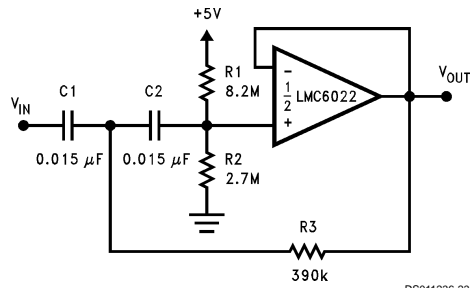
10 Hz Bandpass Filter



DS011236-22

$f_0 = 10 \text{ Hz}$
 $Q = 2.1$
 Gain = -8.8

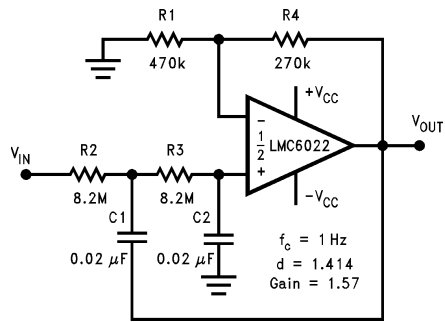
10 Hz High-Pass Filter (2 dB Dip)



DS011236-23

$f_c = 10 \text{ Hz}$
 $d = 0.895$
 Gain = 1

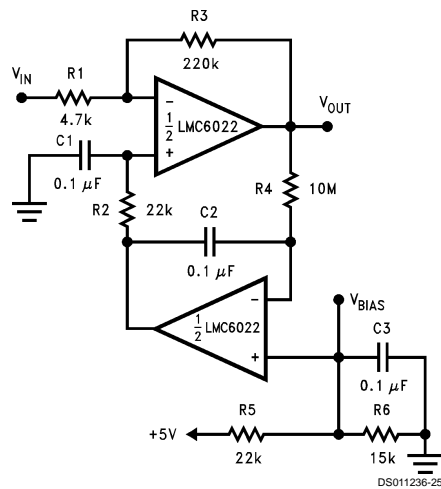
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



DS011236-24

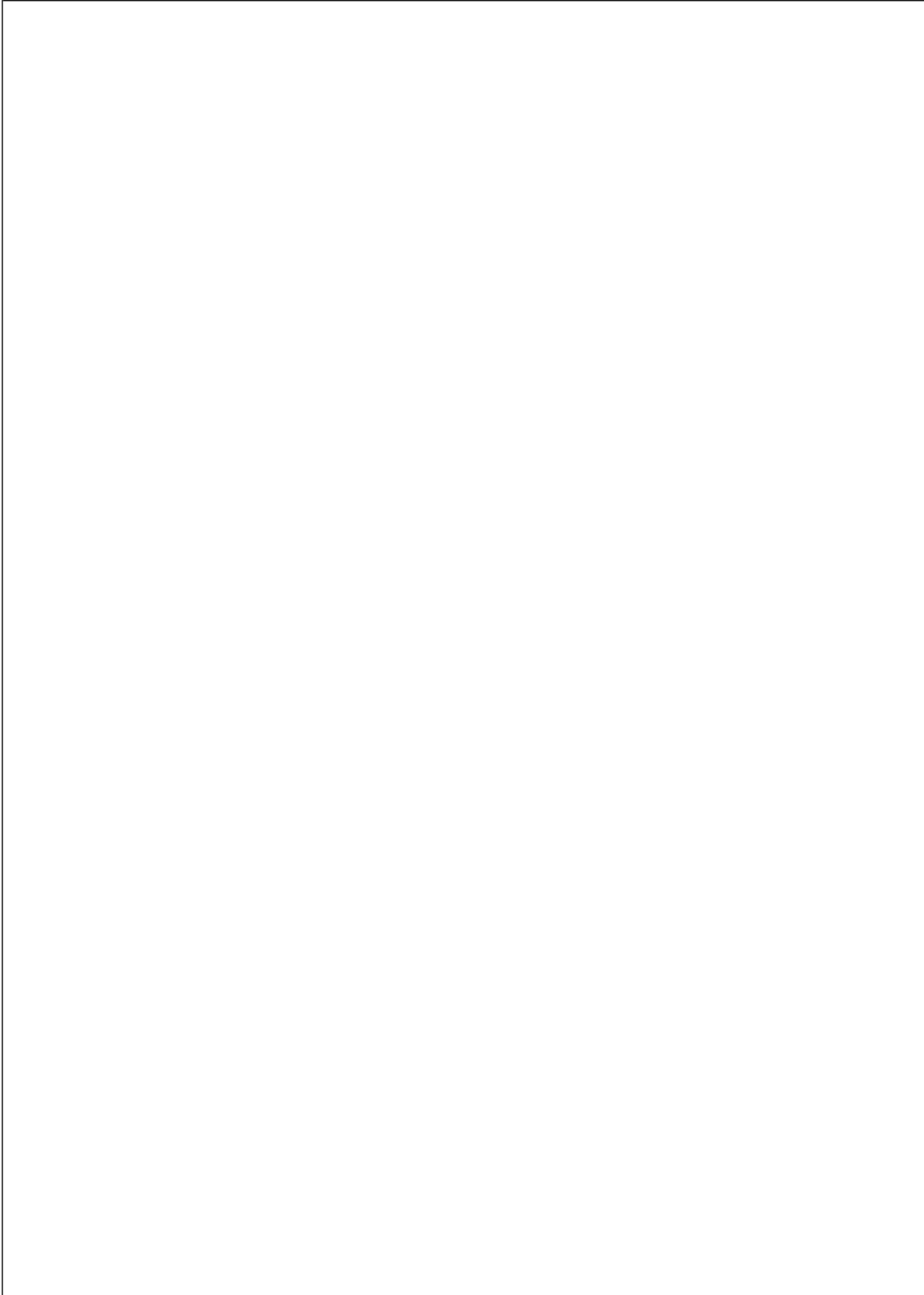
$f_c = 1 \text{ Hz}$
 $d = 1.414$
 Gain = 1.57

High Gain Amplifier with Offset Voltage Reduction



DS011236-25

Gain = -46.8
 Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS} .



LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507