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National Semiconductor

December 1994

LMF90
4th-Order Elliptic Notch Filter

General Description

The LMF90 is a fourth-order elliptic notch (band-reject) filter based on switched-capacitor techniques. No external components are needed to define the response function. The depth of the notch is set using a two-level logic input, and the width is programmed using a three-level logic input. Two different notch depths and three different ratios of notch width to center frequency may be programmed by connecting these pins to V^+, ground, or V^-. Another three-level logic pin sets the ratio of clock frequency to notch frequency.

An internal crystal oscillator is provided. Used in conjunction with a low-cost color TV crystal and the internal clock frequency divider, a notch filter can be built with center frequency at 50 Hz, 60 Hz, 100 Hz, 120 Hz, 150 Hz, or 180 Hz for rejection of power line interference. Several LMF90s can be operated from a single crystal. An additional input is provided for an externally-generated clock signal.

Features

- Center frequency set by external clock or on-board clock oscillator
- No external components needed to set response characteristics
- Notch width, attenuation, and clock-to-center-frequency ratio independently programmable
- 14 pin 0.3″ wide package

Key Specifications

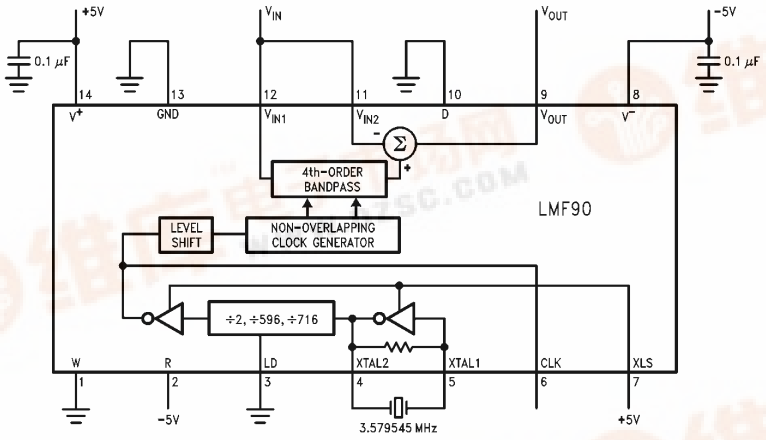
- f_0 Range 0.1 Hz to 30 kHz
- f_0 accuracy over full temperature range (max) 1.5%
- Supply voltage range ±2V to ±7.5V or 4V to 15V
- Passband Ripple (typ) 0.25 dB
- Attenuation at f_0 (typ) 39 dB or 48 dB (selectable)
- f_{CLK}: f_0 100:1, 50:1, or 33.3:1
- Notch Bandwidth (typ) 0.127 f_0, 0.26 f_0, or 0.55 f_0
- Output offset voltage (max) 120 mV

Applications

- Automatic test equipment
- Communications
- Power line interference rejection

Typical Connection

60 Hz Notch Filter



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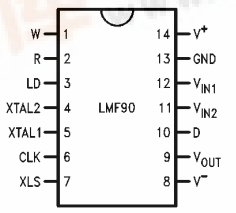
Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/10354–2

Top View

Order Number LMF90CCN, LMF90CIWM, LMF90CCWM, LMF90CIJ, LMF90CCJ, LMF90CIN, LMF90CMJ or LMF90CMJ/883
See NS Package Number J14A, M14B or N14A

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Absolute Maximum Ratings (Notes 1 & 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_S = V^+ - V^-$)	−0.3V to +16V
Voltage at any Input or Output	V^- −0.3V to V^+ +0.3V
Input Current at any Pin (Note 10)	5 mA
Package Input Current (Note 10)	20 mA
Power Dissipation (Note 5)	500 mW
ESD Susceptability (Note 6)	
Pin 9	1800V
All Other Pins	2000V
Soldering Information (Note 4)	
N Package (Soldering, 10 sec.)	260°C
J Package (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Operating Ratings (Notes 2 & 3)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LMF90CCN, LMF90CCWM, LMF90CCJ	$0°C \le T_A \le +70°C$
LMF90CIJ, LMF90CIWM, LMF90CIN	$-40°C \le T_A \le +85°C$
LMF90CMJ, LMF90CMJ/883	$-55°C \le T_A \le +125°C$
Supply Voltage Range	4.0V to 15.0V

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
			Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
f_O	Center Frequency Range		0.1			0.1			Hz (Min)
				30	**30**		**30**		kHz (Max)
f_{CLK}	Clock Frequency Range	Pin 6	10			10			Hz (Min)
		Pin 6		1.5	**1.5**		**1.5**		MHz (Max)
		Pins 4 and 5		4.0	**4.0**		**4.0**		MHz (Max)
f_{CLK}/f_{O1}	Clock-to-Center-Frequency Ratio	$W = D = V^-$, $R = V^+$, $f_{CLK} = 167$ kHz		33.5 ±1%	**33.5 ±1.5%**		**33.5 ±1.5%**		(Max)
f_{CLK}/f_{O2}		$W = D = R = GND$, $f_{CLK} = 250$ kHz		50.25 ±1%	**50.25 ±1.5%**		**50.25 ±1.5%**		(Max)
f_{CLK}/f_{O3}		$W = V^+$, $D = GND$, $R = V^-$, $f_{CLK} = 500$ kHz		100.5 ±1%	**100.5 ±1.5%**		**100.5 ±1.5%**		(Max)
H_{ON}	Passband Gain	DC and 20 kHz, $W = D = V^-$, $R = V^+$, $f_{CLK} = 167$ kHz	0	±0.2	**±0.2**	0	**±0.2**		dB (Max)
		$W = D = R = GND$, $f_{CLK} = 250$ kHz	0	±0.2	**±0.2**	0	**±0.2**		dB (Max)
		$W = V^+$, $D = GND$, $R = V^-$, $f_{CLK} = 500$ kHz	0	±0.2	**±0.2**	0	**±0.2**		dB (Max)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
			Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
PBW	Ratio of Passband Width to Center Frequency	W = D = V^-, R = V^+, f_{CLK} = 167 kHz		0.1275 ±0.0175	**0.1275 ±0.0175**		**0.1275 ±0.0175**		(Max)
		W = D = R = GND, f_{CLK} = 250 kHz		0.265 ±0.025	**0.265 ±0.025**		**0.265 ±0.025**		(Max)
		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz		0.550 ±0.05	**0.550 ±0.05**		**0.550 ±0.05**		(Max)
$A_{Min1}@f_{O1}$	Gain at Center Frequency	W = D = V^-, R = V^+, f_{CLK} = 167 kHz	−39	−30	**−30**	−39	**−30**		dB (Max)
$A_{Min2}@f_{O2}$		W = D = R = GND, f_{CLK} = 250 kHz	−48	−36.5	**−36.5**	−48	**−36.5**		dB (Max)
$A_{Min3}@f_{O3}$		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz	−48	−36.5	**−36.5**	−48	**−36.5**		dB (Max)
	Additional Center Frequency Gain Tests at f_{O1}	W = GND, D = V^-, R = V^+, f_{CLK} = 167 kHz	−36	−30	**−30**	−36	**−30**		dB (Max)
		W = V^+, D = V^-, R = V^+, f_{CLK} = 167 kHz	−36	−30	**−30**	−36	**−30**		dB (Max)
		W = V^-, D = GND, R = V^+, f_{CLK} = 167 kHz	−42	−30	**−30**	−42	**−30**		dB (Max)
		W = D = GND, R = V^+, f_{CLK} = 167 kHz	−48	−35	**−35**	−48	**−35**		dB (Max)
		W = V^+, D = GND,R = V^+, f_{CLK} = 167 kHz	−48	−35	**−35**	−48	**−35**		dB (Max)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions		LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
				Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
	Additional Center Frequency Gain Tests at f_{O2}	$W = V^-$, $D = V^-$, $R = GND$, $f_{CLK} = 250$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = GND$, $D = V^-$, $R = GND$, $f_{CLK} = 250$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = V^+$, $D = V^-$, $R = GND$, $f_{CLK} = 250$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = V^-$, $D = R = GND$, $f_{CLK} = 250$ kHz		−42	−30	**−30**	−42	**−30**		dB (Max)
		$W = V^+$, $D = R = GND$, $f_{CLK} = 250$ kHz		−48	−35	**−35**	−48	**−35**		dB (Max)
	Additional Center Frequency Gain Tests at f_{O3}	$W = D = R = V^-$, $f_{CLK} = 500$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = GND$, $D = V^-$, $R = V^-$, $f_{CLK} = 500$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = V^+$, $D = V^-$, $R = V^-$, $f_{CLK} = 500$ kHz		−36	−30	**−30**	−36	**−30**		dB (Max)
		$W = V^-$, $D = GND$, $R = V^-$, $f_{CLK} = 500$ kHz		−42	−30	**−30**	−42	**−30**		dB (Max)
		$W = D = GND$, $R = V^-$, $f_{CLK} = 500$ kHz		−48	−35	**−35**	−48	**−35**		dB (Max)
A_{3a}	Gain at $f_3 = 0.995\ f_{O1}$	$W = D = V^-$, $R = V^+$, $f_{CLK} = 167$ kHz		−41	−30	**−30**	−41	**−30**		dB (Max)
A_{4a}	Gain at $f_4 = 1.005\ f_{O1}$			−41	−30	**−30**	−41	**−30**		dB (Max)
A_{3b}	Gain at $f_3 = 0.992\ f_{O2}$	$W = D = R = GND$, $f_{CLK} = 250$ kHz		−40	−35	**−35**	−40	**−35**		dB (Max)
A_{4b}	Gain at $f_4 = 1.008\ f_{O2}$			−40	−35	**−35**	−40	**−35**		dB (Max)
A_{3c}	Gain at $f_3 = 0.982\ f_{O3}$	$W = V^+$, $D = GND$, $R = V^-$ $f_{CLK} = 500$ kHz		−41	−35	**−35**	−41	**−35**		dB (Max)
A_{4c}	Gain at $f_4 = 1.018\ f_{O3}$			−41	−35	**−35**	−41	**−35**		dB (Max)
A_{max1}	Passband Ripple	$W = D = V^-$, $R = V^+$, $f_{CLK} = 167$ kHz	$f_5 = 0.914\ f_{O1}$	0.25 0.25	0.9 0	**0.9** **0**	0.25 0.25	**0.9** **0**		dB (Max) dB (Min)
			$f_6 = 1.094\ f_{O1}$	0.25 0.25	0.9 0	**0.9** **0**	0.25 0.25	**0.9** **0**		dB (Max) dB (Min)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions		LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
				Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
A_{Max2}	Passband Ripple	W = D = R = GND, f_{CLK} = 250 kHz	$f_5 = 0.830\ f_{O2}$	0.25 0.25	0.9 0	**0.9** **0**	0.26 0.25	**0.9** **0**		dB (Max) dB (Min)
			$f_6 = 1.205\ f_{O2}$	0.25 0.25	0.9 0	**0.9** **0**	0.25 0.25	**0.9** **0**		dB (Max) dB (Min)
A_{Max3}	Passband Ripple	W = V^+, D = GND, R = V^- f_{CLK} = 500 kHz	$f_5 = 0.700\ f_{O3}$	0.25 0.25	0.9 0	**0.9** **0**	0.25 0.25	**0.9** **0**		dB (Max) dB (Min)
			$f_6 = 1.428\ f_{O3}$	0.25 0.25	0.9 0	**0.9** **0**	0.25 0.25	**0.9** **0**		dB (Max) dB (Min)
E_n	Output Noise	20 kHz Bandwidth W = D = V^-, R = V^+, f_{CLK} = 167 kHz W = D = R = GND, f_{CLK} = 250 kHz W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz		670 370 250			670 370 250			μVrms μVrms μVrms
	Clock Feedthrough			50			50			mVp−p
GBW	Output Buffer Gain Bandwidth			1			1			MHz
SR	Output Buffer Slew Rate			3			3			V/μs
C_L	Maximum Capacitive Load			200			200			pF

DC Electrical Characteristics

The following specifications apply for $V^+ = +5V$ and $V^- = -5V$ unless otherwise specified. **Boldface Limits Apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LMF90CCJ, LMF90CCN, LMF90CCWM			LMF90CIJ, LMF90CIWM, LMF90CIN, LMF90CMJ			Units (Limit)
			Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	Typ (Note 7)	Tested Limit (Note 8)	Design Limit (Note 9)	
I_S	Power Supply Current	$f_{CLK} = 500$ kHz, $V_{IN1} = V_{IN2} = GND$	2.35	5.0	**5.0**	2.35	**5.0**		mA (Max)
V_{OS}	Output Offset Voltage	W = D = V^-, R = V^+, $f_{CLK} = 167$ kHz W = D = R = GND, $f_{CLK} = 250$ kHz W = V^+, D = GND, R = V^-, $f_{CLK} = 500$ kHz	±50 ±60 ±80	±120 ±140 ±170	**±120** **±140** **±170**	±50 ±60 ±80	**±120** **±140** **±170**		mV (Max) mV (Max) mV (Max)
V_{OUT}	Output Voltage Swing	$R_L = 5$ kΩ	+4.2, −4.7	±4.0	**±4.0**	+4.2, −4.7	**±4.0**		V (Min)
V_{I1}	Logical "Low" Input Voltage	Pins 1, 2, 3, 7, and 10		−4.0	**−4.0**		**−4.0**		V (Max)
V_{I2}	Logical "GND" Input Voltage	Pins 1, 2, 3, 7, and 10		+1.0 −1.0	**+1.0** **−1.0**		**+1.0** **−1.0**		V (Max) V (Min)
V_{I3}	Logical "High" Input Voltage	Pins 1, 2, 3, and 7		+4.0	**+4.0**		**+4.0**		V (Min)
I_{IN}	Input Current	Pins 1, 2, 3, 7, and 10		±10	**±10**		**±10**		μA (Max)
V_{IL}	Logical "0" Input Voltage, Pins 5 and 6	Pin 5, XLS = V^+ or Pin 6, XLS = GND		−4.0	**−4.0**		**−4.0**		V (Max)
V_{IH}	Logical "1" Input Voltage, Pins 5 and 6			+4.0	**+4.0**		**+4.0**		V(Min)
V_{IL}	Logical "0" Input Voltage, Pin 6	$V^+ - V^- = 10V$, XLS = V^- or $V^+ = +5V$, $V^- = 0V$, XLS = +2.5V		+0.8	**+0.8**		**+0.8**		V (Max)
V_{IH}	Logical "1" Input Voltage, Pin 6			+2.0	**+2.0**		**+2.0**		V (Min)
V_{OL}	Logical "0" Output Voltage, Pin 6	XLS = V^+, $\|I_{OUT}\| = 4$ mA		−4.0	**−4.0**		**−4.0**		V (Max)
V_{OH}	Logical "1" Output Voltage, Pin 6			+4.0	**+4.0**		**+4.0**		V (Min)

DC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is intended to be functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND unless otherwise specified.

Note 4: See AN450 ''Surface Mounting Methods and Their Effect on Product Reliability'' or the section titled ''Surface Mount'' found in any current Linear Data Book for other methods of soldering surface mount devices.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 150°C$, and the typical thermal resistance (Θ_{JA}) when board mounted is 61°C/W for the LMF90CCN and CIN, 134°C/W for the LMF90CCWM and CWIM and 59°C/W for the LMF90CCJ, CIJ and CMJ.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typicals are at $T_J = 25°C$ and represent the most likely parametric norm.

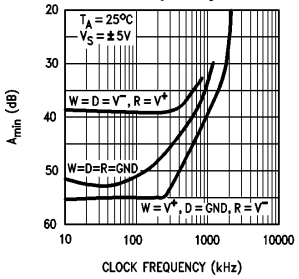
Note 8: Tested Limits are guaranteed and 100% tested.

Note 9: Design Limits are guaranteed, but not 100% tested.

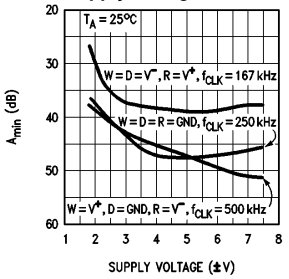
Note 10: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < V^-$ or $V_{IN} > V^+$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Typical Performance Characteristics

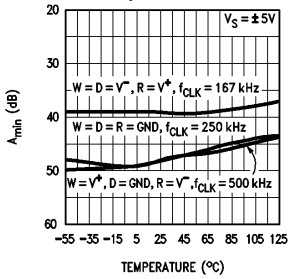
Notch Depth vs Clock Frequency



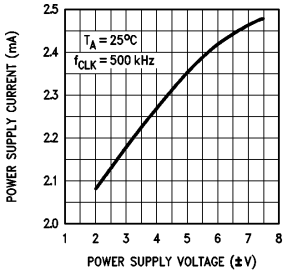
Notch Depth vs Supply Voltage



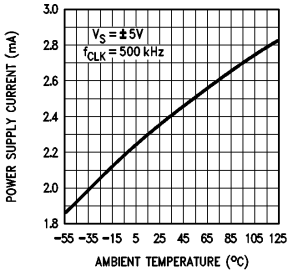
Notch Depth vs Temperature



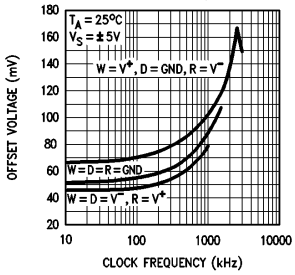
Power Supply Current vs Power Supply Voltage



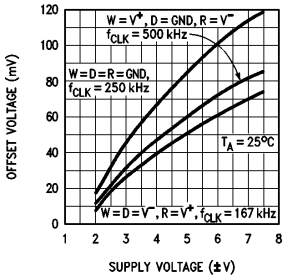
Power Supply Current vs Temperature



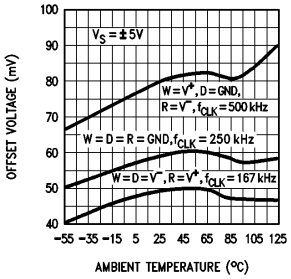
Offset Voltage vs Clock Frequency



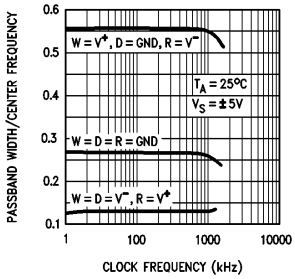
Offset Voltage vs Supply Voltage



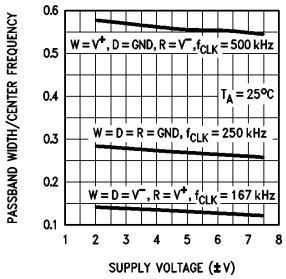
Offset Voltage vs Temperature



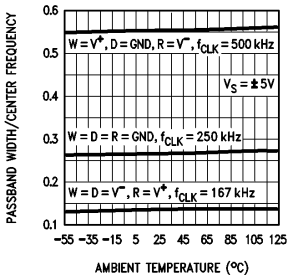
Passband Width vs Clock Frequency



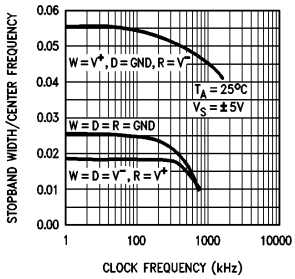
Passband Width vs Supply Voltage



Passband Width vs Temperature



Stopband Width vs Clock Frequency



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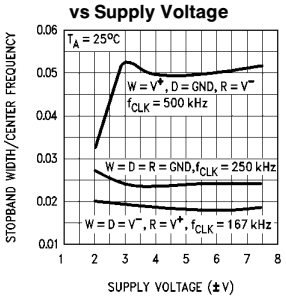
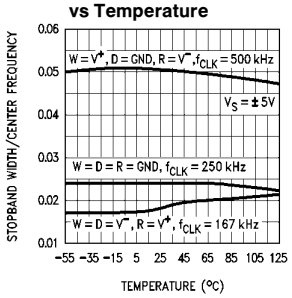
Typical Performance Characteristics (Continued)

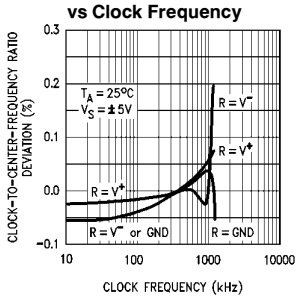
Stopband Width vs Supply Voltage



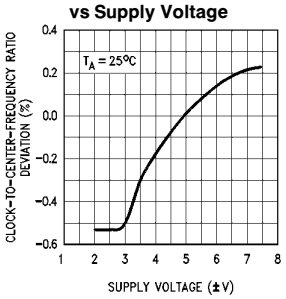
Stopband Width vs Temperature



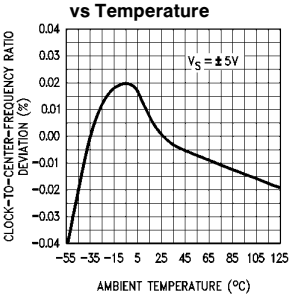
Clock-to-Center-Frequency Ratio Deviation vs Clock Frequency



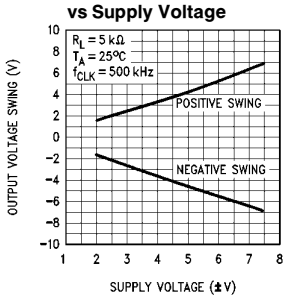
Clock-to-Center-Frequency Ratio Deviation vs Supply Voltage



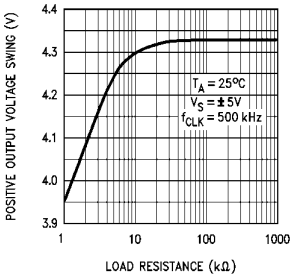
Clock-to-Center-Frequency Ratio Deviation vs Temperature



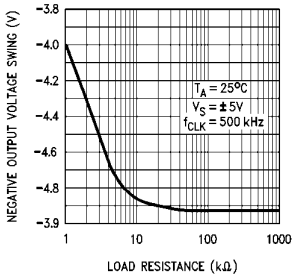
Output Swing vs Supply Voltage



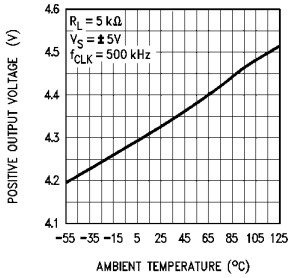
Positive Output Voltage Swing vs Load Resistance



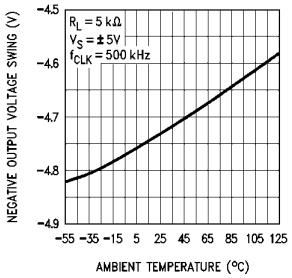
Negative Output Voltage Swing vs Load Resistance



Positive Output Swing vs Temperature



Negative Output Swing vs Temperature



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Pin Descriptions

W (Pin 1) This three-level logic input sets the width of the notch. Notch width is $f_{c2}-f_{c1}$ (see *Figure 1*). When W is tied to V^+ (pin 14), GND (pin 13), or V^- (pin 8), the notch width is 0.55 f_0, 0.26 f_0, or 0.127 f_0, respectively.

R (Pin 2) This three-level logic input sets the ratio of the clock frequency (f_{CLK}) to the center frequency (f_0). When R is tied to V^+, GND, or V^-, the clock-to-center-frequency ratio is 33.33:1, 50:1, or 100:1, respectively.

LD (Pin 3) This three-level logic input sets the division factor of the clock frequency divider. When LD is tied to V^+, GND, or V^-, the division factor is 716, 596, or 2, respectively.

XTAL2 (Pin 4) This is the output of the internal crystal oscillator. When using the internal oscillator, the crystal should be tied between XTAL2 and XTAL1. (The capacitors are internal—no external capacitors are needed for the oscillator to operate.) When not using the internal oscillator this pin should be left open.

XTAL1 (Pin 5) This is the crystal oscillator input. When using the internal oscillator, the crystal should be tied between XTAL1 and XTAL2. XTAL1 can also be used as an input for an external clock signal swinging from V^+ to V^-. The frequency of the crystal or the external clock will be divided internally by the clock divider as determined by the programming voltage on pin 3.

CLK (Pin 6) This is the filter clock pin. The clock signal appearing on this pin is the filter clock (f_{CLK}). When using the internal crystal oscillator or an external clock signal applied to pin 5 while pin 7 is tied to V^+, the CLK pin is the output of the divider and can be used to drive other LMF90s with its rail-to-rail output swing. When not using the internal crystal oscillator or an external clock on pin 5, the CLK pin can be used as a CMOS or TTL clock input provided that pin 7 is tied to GND or V^-. For best performance, the duty cycle of a clock signal applied to this pin should be near 50%, especially at higher clock frequencies.

XLS (Pin 7) This is a three-level logic pin. When XLS is tied to V^+, the crystal oscillator and frequency divider are enabled and CLK (pin 6) is an output. When XLS is tied to GND (pin 13), the crystal oscillator and frequency divider are disabled and pin 6 is an input for a clock swinging between V^- and V^+. When XLS is tied to V^-, the crystal oscillator and frequency divider are disabled and pin 6 is a TTL level clock input for a clock signal swinging between GND and V^+ or between V^- and GND.

V^- (Pin 8) This is the negative power supply pin. It should be bypassed with at least a 0.1 μF capacitor. For single-supply operation, connect this pin to system ground.

V_{OUT} (Pin 9) This is the filter output.

D (Pin 10) This two-level logic input is used to set the depth of the notch (the attenuation at f_0). When D is tied to GND or V^-, the typical notch depth is 48 dB or 39 dB, respectively. Note, however, that the notch depth is also dependent on the width setting (pin 1). See the Electrical Characteristics for tested limits.

V_{IN2} (Pin 11) This is the input to the difference amplifier section of the notch filter.

V_{IN1} (Pin 12) This is the input to the internal bandpass filter. This pin is normally connected to pin 11. For wide bandwidth applications, an anti-aliasing filter can be inserted between pin 11 and pin 12.

GND (Pin 13) This is the analog ground reference for the LMF90. In split supply applications, GND should be connected to the system ground. When operating the LMF90 from a single positive power supply voltage, pin 13 should be connected to a "clean" reference voltage midway between V^+ and V^-.

V^+ (Pin 14) This is the positive power supply pin. It should be bypassed with at least a 0.1 μF capacitor.

1.0 Definition of Terms

A_{max}: the maximum amount of gain variation within the filter's passband (See *Figure 1*). For the LMF90, A_{Max} is nominally equal to 0.25 dB.

A_{min}: the minimum attenuation within the notch's stopband. (See *Figure 1*). This parameter is adjusted by programming voltage applied to pin 10 (D).

Bandwidth (BW) or Passband Width: the difference in frequency between the notch filter's two cutoff frequencies.

Cutoff Frequency: for a notch filter, one of the two frequencies, f_{C1} and f_{C2} that define the edges of the passband. At these two frequencies, the filter has a gain equal to the passband gain.

f_{CLK}: the frequency of the clock signal that appears at the CLK pin. This frequency determines the filter's center frequency. Depending on the programming voltage on pin 2 (R), f_{CLK} will be either 33.33, 50, or 100 times the center frequency of the notch.

f_0 or f_{Notch}: the center frequency of the notch filter. This frequency is measured by finding the two frequencies for which the gain -3 dB relative to the passband gain, and calculating their geometrical mean.

Passband: for a notch filter, frequencies above the upper cutoff frequency (f_{C2} in *Figure 1*) and below the lower cutoff frequency (f_{C1} in *Figure 1*).

1.0 Definition of Terms (Continued)

Passband Gain: the notch filter's gain for signal frequencies near dc or $f_{CLK}/2$. The passband gain of a notch filter is also called "H_{ON}". For the LMF90, the passband gain is nominally 0 dB.

Passband Ripple: the variation in gain within the filter's passband.

Stopband: for a notch filter, the range of frequencies for which the attenuation is at least A_{min} (f_{S1} to f_{S2}) in *Figure 1*).

Stop Frequency: one of the two frequencies (f_{S1} and f_{S2}) at the edges of the notch's stopband.

Stopband Width (SBW): the difference in frequency between the two stopband edges ($f_{S2}-f_{S1}$).

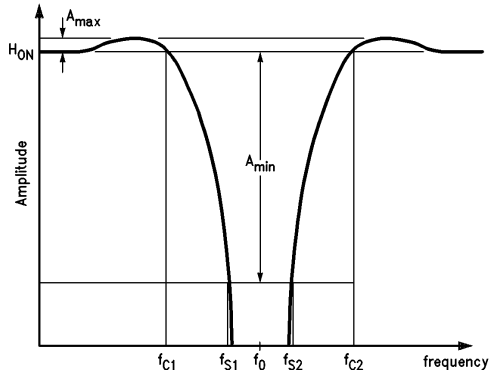

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FIGURE 1. General Form of Notch Response

2.0 Applications Information

2.1 FUNCTIONAL DESCRIPTION

The LMF90 uses switched-capacitor techniques to realize a fourth-order elliptic notch transfer function with 0.25 dB passband ripple. No external components other than supply bypass capacitors and a clock (or crystal) are required.

As is evident from the block diagram, the analog signal path consists of a fourth-order bandpass filter and a summing amplifier. The analog input signal is applied to the input of the bandpass filter, and to one of the summing amplifier inputs. The bandpass filter's output drives the other summing amplifier input. The output of the summing amplifier is the difference between the input signal and the bandpass output, and has a notch filter characteristic. Notch width and depth are controlled by the dc programming voltages applied to two pins (1 and 10), and the center frequency is proportional to the clock frequency, which may be generated externally or internally with the aid of an external crystal. The clock-to-center-frequency ratio can be one of three different values, and is selected by the voltage on a three-level logic input (pin 2).

The clock signal passes through a digital frequency divider circuit that can divide the clock frequency by any of three different factors before it reaches the filters. This divider can also be disabled, if desired. Pin 7 enables and disables the frequency divider and also configures the clock inputs for operation with an external CMOS or TTL clock or with the internal oscillator circuit.

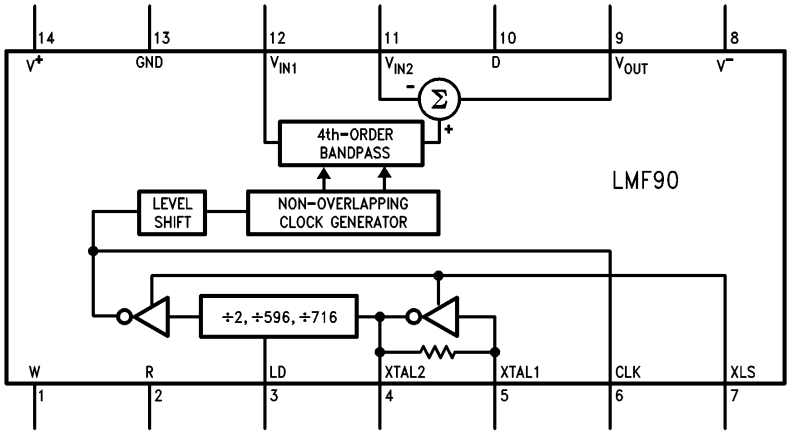

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FIGURE 2. LMF90 Block Diagram

2.0 Applications Information (Continued)

2.2 PROGRAMMING PINS

The LMF90 has five control pins that are used to program the filter's characteristics via a three-level logic scheme. In dual-supply applications, these inputs are tied to either V^+, V^-, or GND in order to select a particular set of characteristics. For example, the W input (pin 1) sets the filter's passband width to 0.55 f_0, 0.26 f_0 or 0.127 f_0 when the W input is connected to V^+, GND, or V^-, respectively. Applying V^- and GND to the D input (pin 10) will set the notch depth to 40 dB or 30 dB, respectively.

The R input (pin 2) is another three-level logic input, and it sets the clock-to-center-frequency ratio to 33.33:1, 50:1, or 100:1 for input voltages equal to V^+, GND, or V^-, respectively. Note that the clock frequency referred to here is the frequency at the CLK pin and at the frequency divider output (if used). This is different from the frequency at the divider's input. LD (pin 3) sets the frequency divider's division factor to either 716, 596, or 2 for input voltages equal to V^+, GND, or V^-, respectively. XLS (pin 7) enables and disables the crystal oscillator and clock divider. When XLS is connected to the positive supply, the oscillator and divider are enabled, and CLK is the output of the divider and can drive the clock inputs of other LMF90s. When XLS is connected to GND, the oscillator and divider are disabled, and the CLK pin becomes a clock input for CMOS-level signals. Connecting XLS to the negative supply disables the oscillator and divider and causes CLK to operate as a TTL-level clock input.

Using an external 3.579545 MHz color television crystal with the internal oscillator and divider, it is possible to build a power line frequency notch for 50 Hz or 60 Hz line frequencies or their second and third harmonics using the LMF90. A 60 Hz notch is shown in the Typical Application circuit on the first page of this data sheet. Connecting LD to V^+ changes the notch frequency to 50 Hz. Changing the clock-to-center-frequency ratio to 50:1 results in a second-harmonic notch, and a 33:1 ratio causes the LMF90 to notch the third harmonic.

Table I illustrates 18 different combinations of filter bandwidth, depth, and clock-to-center-frequency ratio obtained by choosing the appropriate W, D, and R programming voltages.

2.3 DIGITAL INPUTS AND OUTPUTS

As mentioned above, the CLK pin can serve as either an input or an output, depending on the programming voltage on XLS. When CLK is operating as a TTL input, it will operate properly in both dual-supply and single-supply applications, because it has two logic thresholds—one referred to V^-, and one referred to GND. When operating as an output, CLK swings rail-to-rail (CMOS logic levels).

XTAL1 and XTAL2 are the input and output pins for the internal crystal oscillator. When using the internal oscillator (XLS connected to V^+), the crystal is connected between these two pins. When the internal oscillator is not used, XTAL2 should be left open. XTAL1 can be used as an input for an external CMOS-level clock signal swinging from V^- to V^+. The frequency of the crystal or the external clock applied to XTAL1 will be divided by the internal frequency divider as determined by programming voltage on the LD pin.

2.4 SAMPLED-DATA SYSTEM CONSIDERATIONS OUTPUT STEPS

Because the LMF90 uses switched-capacitor techniques, its performance differs in several ways from non-sampled (continuous) circuits. The analog signal at the input to the internal bandpass filter (pin 12) is sampled during each clock cycle, and, since the output voltage can change only once every clock cycle, the result is a discontinuous output signal. The bandpass output takes the form of a series of voltage ''steps'', as shown in *Figure 3*. The steps are smaller when the clock frequency is much greater than the signal frequency.

Switched-capacitor techniques are used to set the summing amplifier's gain. Its input and feedback ''resistors'' are actually made from switches and capacitors. Two sets of these ''resistors'' are alternated during each clock cycle. Each time these gain-setting components are switched, there will be no feedback connected to the op amp for a short period of time (about 50 ns). This generates very low-amplitude output signals at $f_{CLK} + f_{IN}$, $f_{CLK} - f_{IN}$, $2\,f_{CLK} + f_{IN}$, etc. The amplitude of each of these intermodulation components will typically be at least 70 dB below the input signal amplitude and well beyond the spectrum of interest.

TABLE I. Operation of LMF90 Programming Pins. Values given are for nominal levels of attenuation.

R		V^- ($f_{CLK}/f_0 = 100$)			GND ($f_{CLK}/f_0 = 50$)			V^+ ($f_{CLK}/f_0 = 33.33$)		
D	W	A_{min} (dB)	BW/f_0	SBW/f_0	A_{min} (dB)	BW/f_0	SBW/f_0	A_{min} (dB)	BW/f_0	SBW/f_0
V^-	V^-	−30	0.12	0.019	−30	0.12	0.019	−30	0.12	0.019
	GND	−30	0.26	0.040	−30	0.26	0.040	−30	0.26	0.040
	V^+	−30	0.55	0.082	−30	0.55	0.082	−30	0.55	0.082
GND	V^-	−35	0.12	0.010	−35	0.12	0.010	−35	0.12	0.010
	GND	−40	0.26	0.024	−40	0.26	0.024	−40	0.26	0.024
	V^+	−40	0.55	0.050	−40	0.55	0.050	−40	0.55	0.050

2.0 Applications Information (Continued)

ALIASING

Another important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The LMF90's sampling frequency is the same as the filter's clock frequency. This is the frequency at the CLK pin). If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled-data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_S/2 + 10$ Hz will cause the system to respond as though the input frequency was $f_s/2 - 10$ Hz. This phenomenon is known as "aliasing". Aliasing can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$.

In some cases, it may be necessary to use a bandwidth limiting filter (often a simple passive RC low-pass) ahead of the bandpass input. Although the summing amplifier uses switched-capacitor techniques, it does not exhibit aliasing behavior, and the anti-aliasing filter need not be in its input signal path. The filter can be placed ahead of pin 12 as shown in *Figure 4*, with the non-band limited input signal applied to pin 11. The output spectrum will therefore be wideband, although limited by the bandwidth of the summing amplifier's output buffer amplifier (typically 1 MHz), even if f_{CLK} is less than 1 MHz. Phase shift in the anti-aliasing filter will affect the accuracy of the notch transfer function, however, so it is best to use the highest available clock-to-center-frequency ratio (100:1) and set the RC filter cutoff frequency to about 15 to 20 times the notch frequency. This will provide reasonable attenuation of high-frequency input signals, while avoiding degradation of the overall notch response. If the anti-aliasing filter's cutoff frequency is too low, it will introduce phase shift and gain errors large enough to shift the frequency of the notch and reduce its depth. A cutoff frequency that is too high may not provide sufficient attenuation of unwanted high-frequency signals.

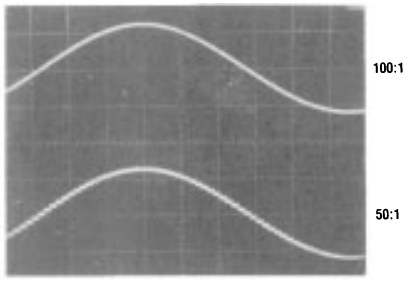

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FIGURE 3. Output waveform of a switched-capacitor filter. Note the voltage steps caused by sampling at the clock frequency.

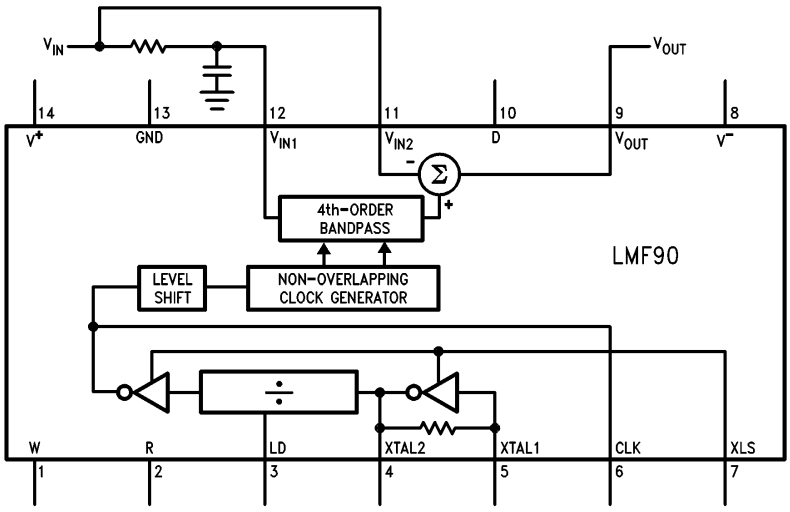

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FIGURE 4. Using a simple passive low-pass filter to prevent aliasing in the presence of high-frequency input signals.

2.0 Applications Information (Continued)

NOISE

Switched-capacitor filters have two kinds of noise at their outputs. There is a random, ''thermal'' noise component whose level is typically on the order of hundreds of microvolts. The other kind of noise is digital clock feedthrough. This will have an amplitude in the vicinity of 50 mV peak-to-peak. In some applications, the clock noise frequency is so high compared to the signal frequency that it is unimportant. In other cases, clock noise may have to be removed from the output signal with, for example, a passive low-pass filter at the LMF90's output pin.

CLOCK FREQUENCY LIMITATIONS

The performance characteristics of a switched-capacitor filter depend on the switching (clock) frequency. At very low clock frequencies (below 10 Hz), the time between clock cycles is relatively long, and small parasitic leakage currents cause the internal capacitors to discharge sufficiently to affect the filter's offset voltage and gain. This effect becomes more pronounced at elevated operating temperatures.

At higher clock frequencies, performance deviations are primarily due to the reduced time available for the internal operational amplifiers to settle. Best performance with high clock frequencies will be obtained when the filter clock's duty cycle is 50%. The clock frequency divider, when used, provides a 50% duty cycle clock to the filter, but when an external clock is applied to CLK, it should have a duty cycle close to 50% for best performance.

Input Impedance

The input to the bandpass section of the LMF90 (V_{IN1}) is similar to the switched-capacitor circuit shown in *Figure 5*. During the first half of a clock cycle, the θ_1 switch closes, charging C_{IN} to the input voltage V_{IN}. During the second half-cycle, the θ_2 switch closes, and the charge on C_{IN} is transferred to the feedback capacitor. At frequencies well below the clock frequency, the input impedance approximates a resistor whose value is

$$R_{IN} = \frac{1}{C_{IN}\, f_{CLK}}.$$

At the bandpass filter input, C_{IN} is nominally 3.0 pF. For a worst-case calculation of effective R_{IN}, assume C_{IN} = 3.0 pF and f_{CLK} = 1.5 MHz. Thus,

$$R_{IN}\,(\text{Min}) = \frac{1}{4.5 \times 10^{-6}} = 222\ \text{k}\Omega.$$

At the maximum clock frequency of 1.5 MHz, the lowest typical value for the effective R_{IN} at the V_{IN1} input is therefore 222 kΩ. Note that R_{IN} increases as f_{CLK} decreases, so the input impedance will be greater than or equal to this value. Source impedance should be low enough that this input impedance doesn't significantly affect gain.

The summing amplifier input impedance at V_{IN2} is calculated in a similar manner, except that C_{IN} = 5.0 pF. This yields a minimum input impedance of 133 kΩ at V_{IN2}. When both inputs are connected together, the combined input impedance will be 83.3 kΩ with a 1.5 MHz filter clock.

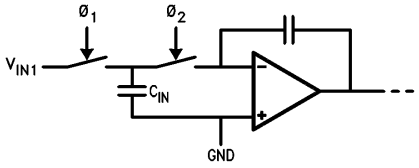

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FIGURE 5. Simplified LMF90 bandpass section input stage. At frequencies well below the center frequency, the input impedance appears to be resistive.

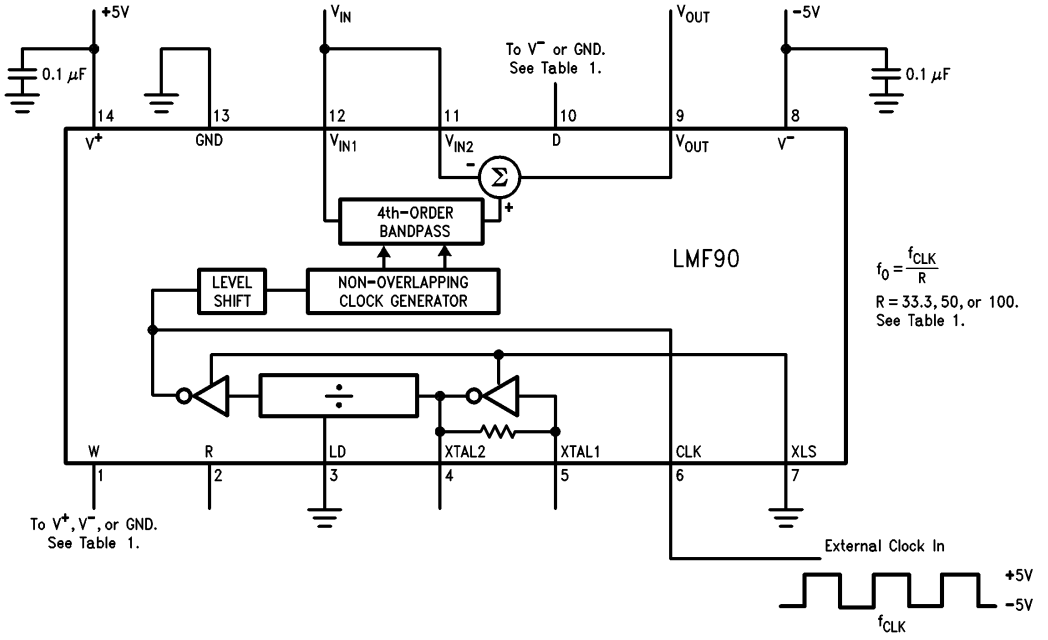
2.5 POWER SUPPLY AND CLOCK OPTIONS

The LMF90 is designed to operate from either single or dual power supply voltages from 5V to 15V. In either case, the supply pins should be well-bypassed to minimize any feedthrough of power supply noise into the filter's signal path. Such feedthrough can significantly reduce the depth of the notch. For operation from dual supply voltages, connect V^- (pin 8) to the negative supply, GND (pin 13) to the system ground, and V^+ to the positive supply.

For single supply operation, simply connect V^- to system ground and GND (Pin 13) to a ''clean'' reference voltage at mid-supply. This reference voltage can be developed with a pair of resistors and a capacitor as shown in *Figures 10* through *16*. Note that for single supply operation, the three-level logic inputs should be connected to system ground and $V^+/2$ instead of V^- and GND. The CLK input will operate properly with TTL-level clock signals when the LMF90 is powered from either single or dual supplies because it has two TTL thresholds, one referred to the V^- pin and one referred to the GND pin. XLS should be connected to the V^- pin when an external TTL clock is used. *Figures 6* through *16* illustrate a wide variety of power supply and clock options.

2.0 Applications Information (Continued)

DUAL-SUPPLY CLOCK OPTIONS



TL/H/10354–10

FIGURE 6. Dual supply; external CMOS-level clock. Internal frequency divider disabled.

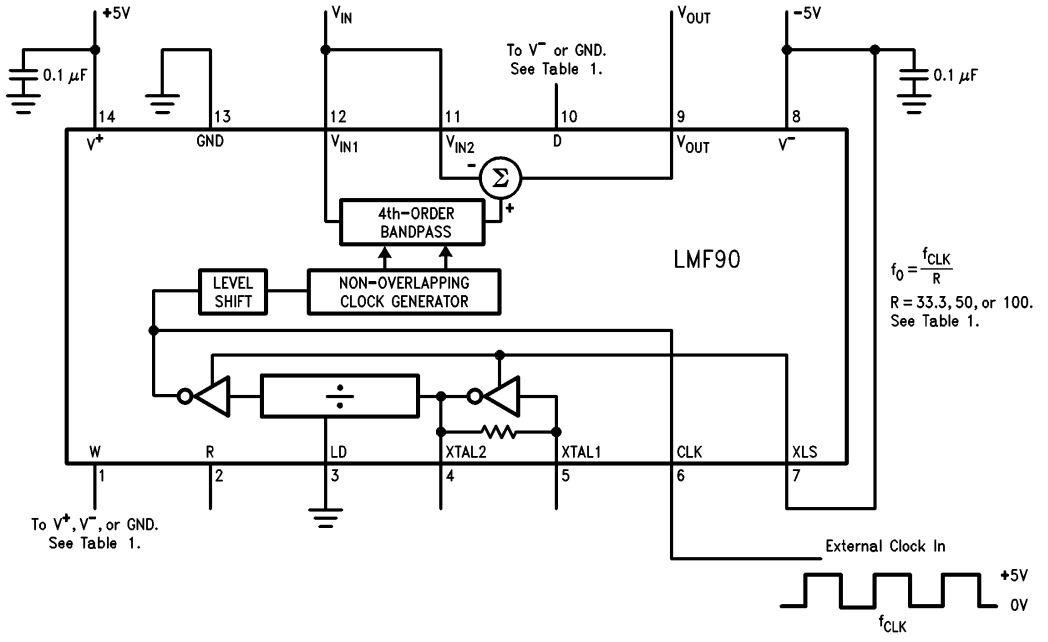


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FIGURE 7. Dual supply; TTL-level clock. Internal frequency divider disabled.

2.0 Applications Information (Continued)

DUAL-SUPPLY CLOCK OPTIONS

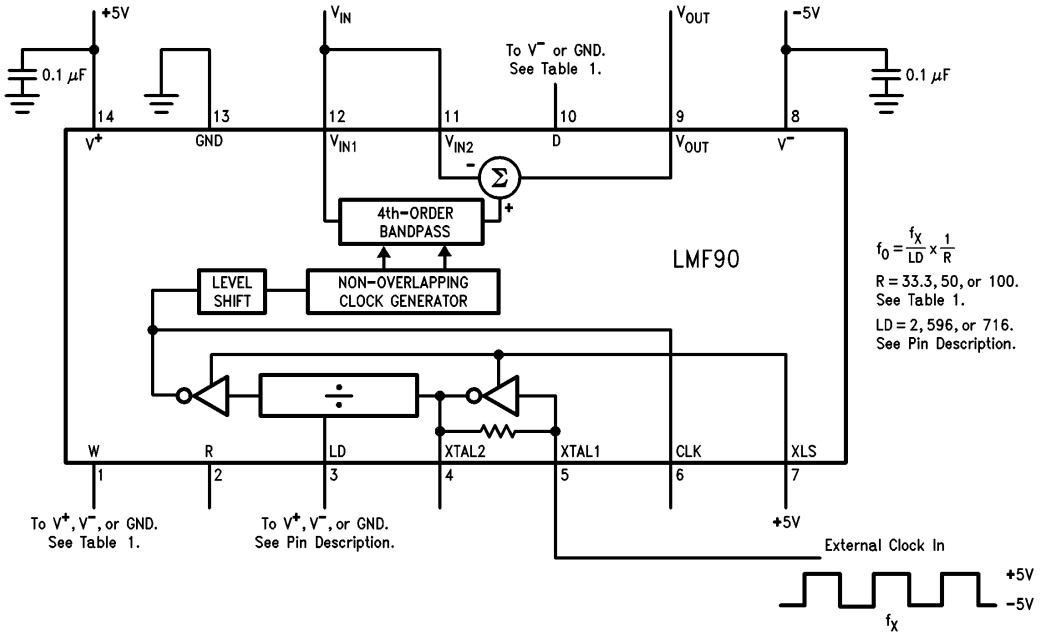

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FIGURE 8. Dual Supply; external CMOS-level clock. Internal frequency divider enabled. Output of logic divider available on pin 6.

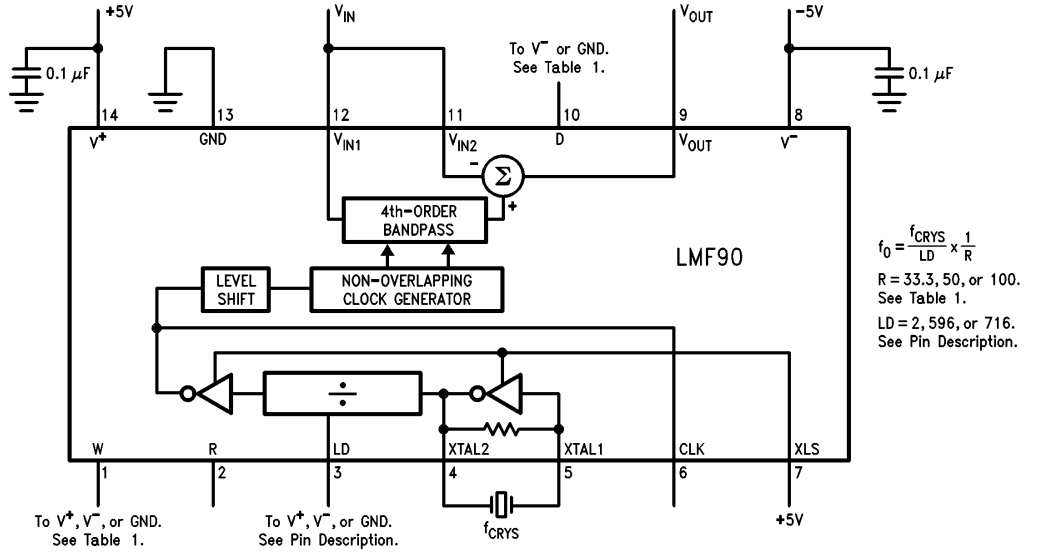

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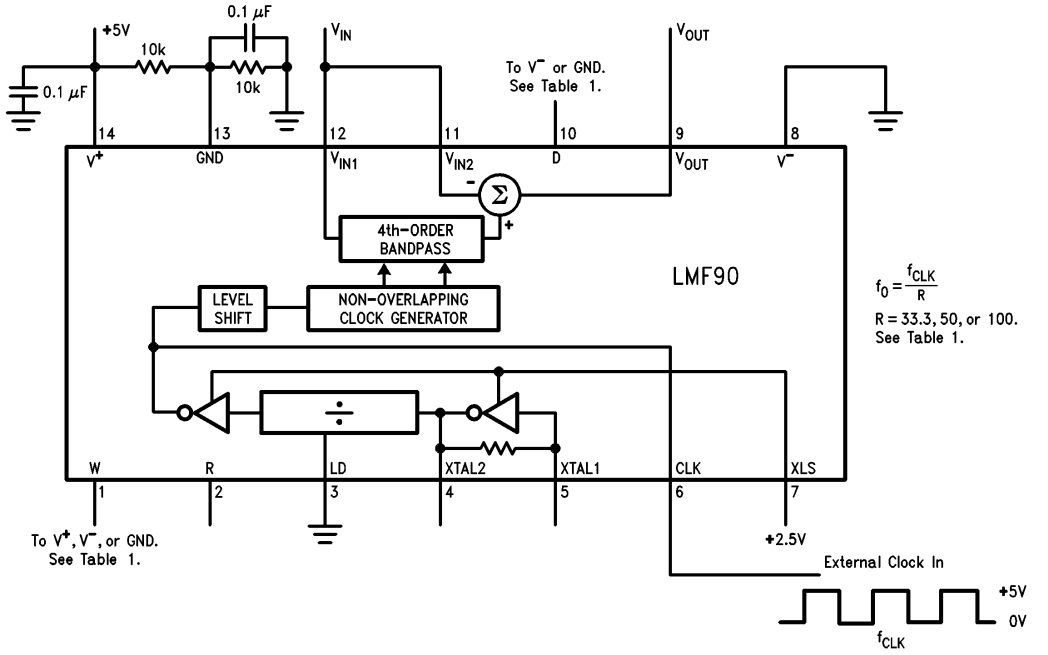
FIGURE 9. Dual supply; internal crystal clock oscillator. Internal frequency divider enabled. Output of logic divider available on pin 6.

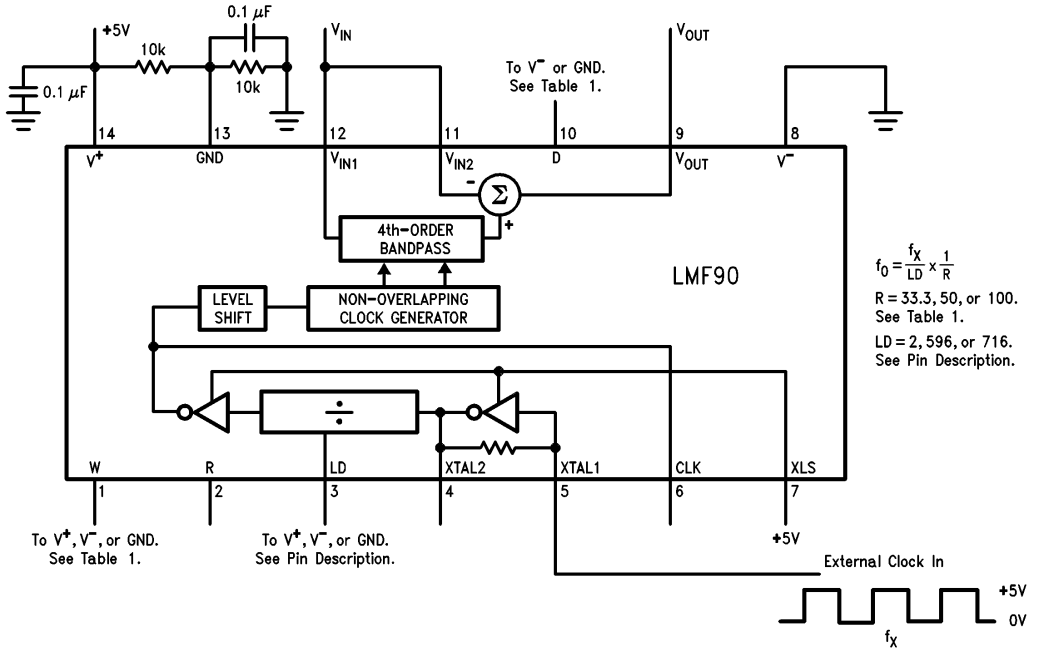
2.0 Applications Information (Continued)

SINGLE-SUPPLY CLOCK OPTIONS



TL/H/10354–14

FIGURE 10. Single + 5V supply; external TTL-level clock. Internal frequency divider disabled.

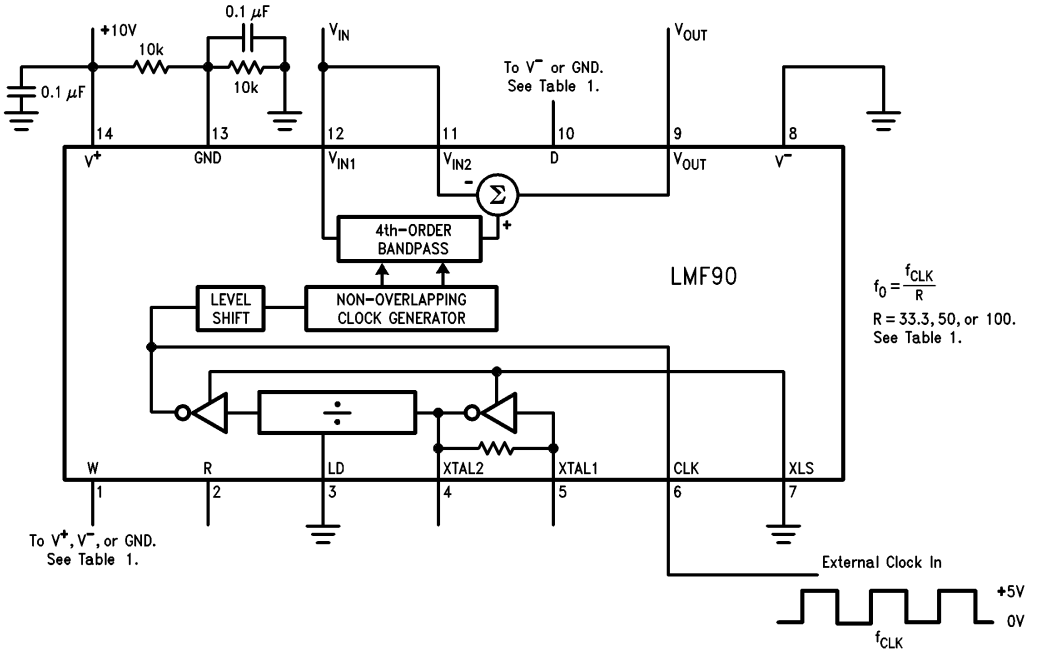


TL/H/10354–15

FIGURE 11. Single + 5V supply; external CMOS-level clock. Internal frequency divider enabled. Output of logic divider available on pin 6.

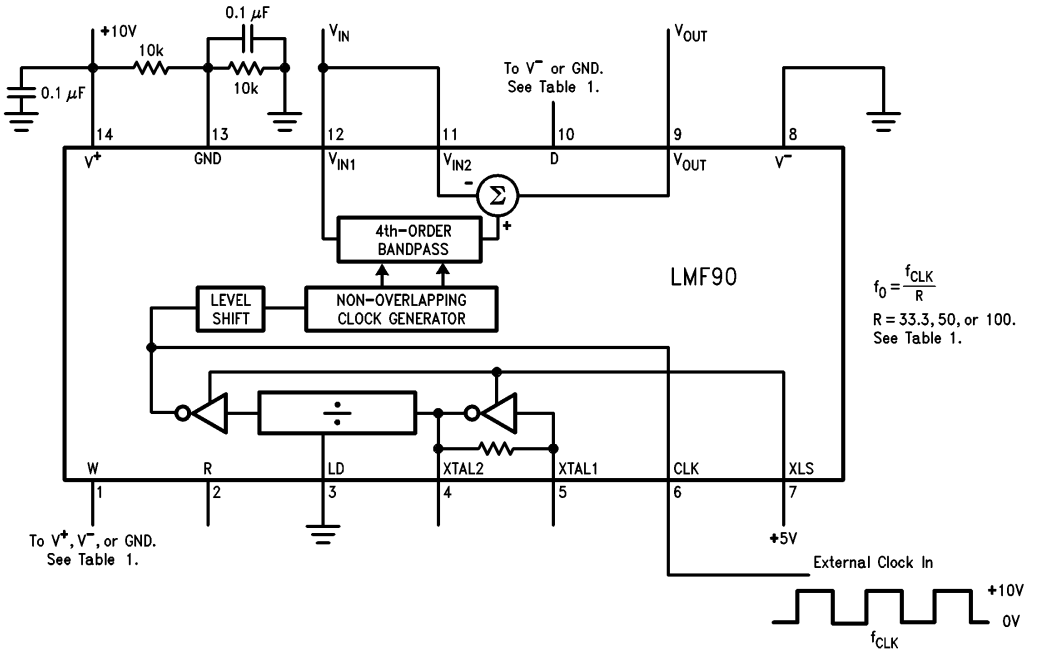
2.0 Applications Information (Continued)

SINGLE-SUPPLY CLOCK OPTIONS



TL/H/10354–16

FIGURE 12. Single + 10V supply; external TTL-level clock. Internal frequency divider disabled.

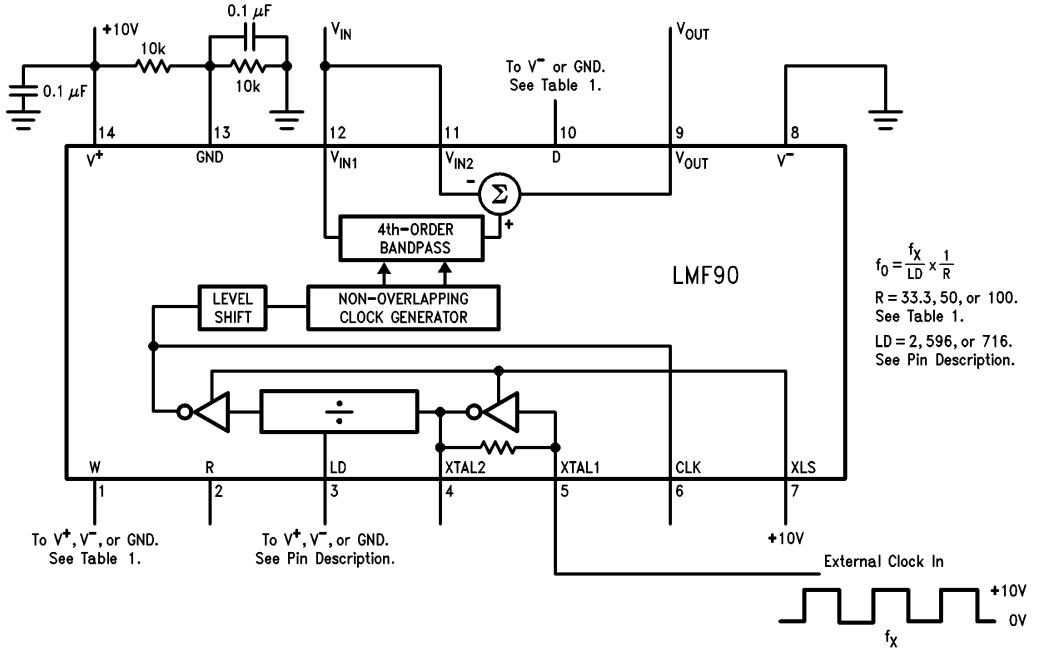


TL/H/10354–17

FIGURE 13. Single + 10V supply; external CMOS-level clock. Internal frequency divider disabled.

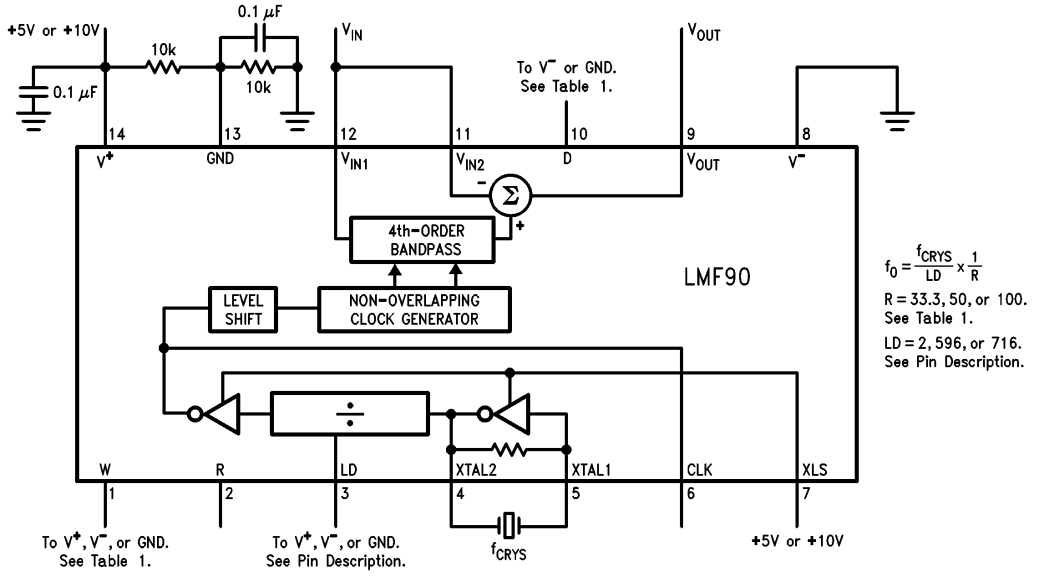
2.0 Applications Information (Continued)

SINGLE-SUPPLY CLOCK OPTIONS



TL/H/10354–18

FIGURE 14. Single + 10V supply; external CMOS-level clock. Internal frequency divider enabled. Output of logic divider available on pin 6.



TL/H/10354–19

FIGURE 15. Single + 5V or + 10V supply; internal crystal clock oscillator. Internal frequency divider enabled. Output of logic divider available on pin 6.

Typical Application

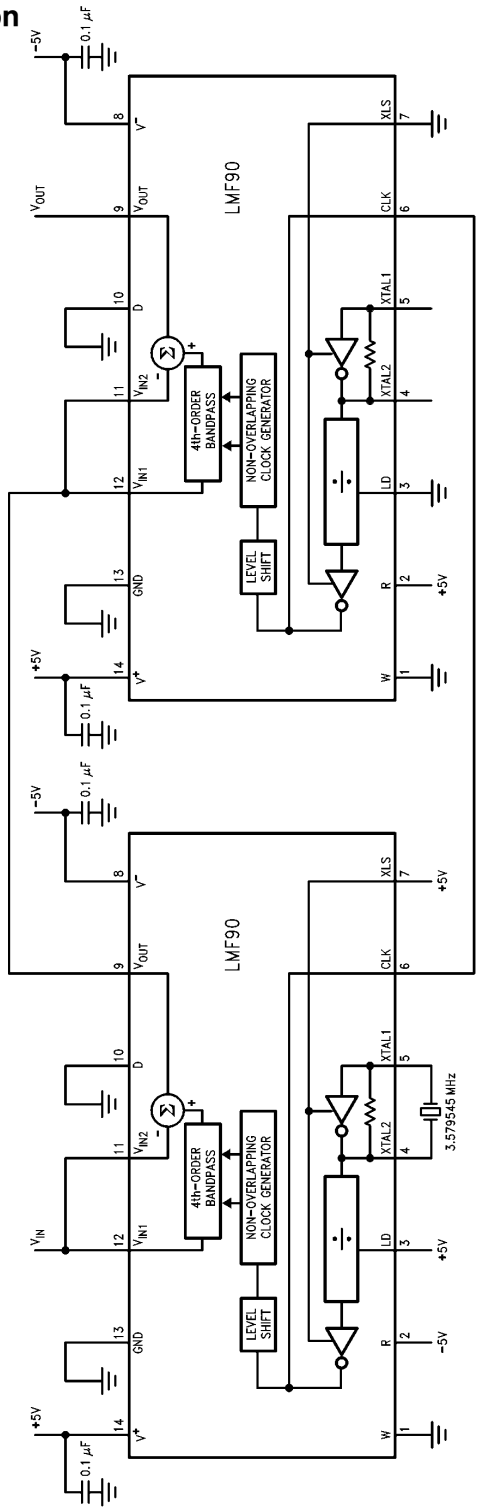
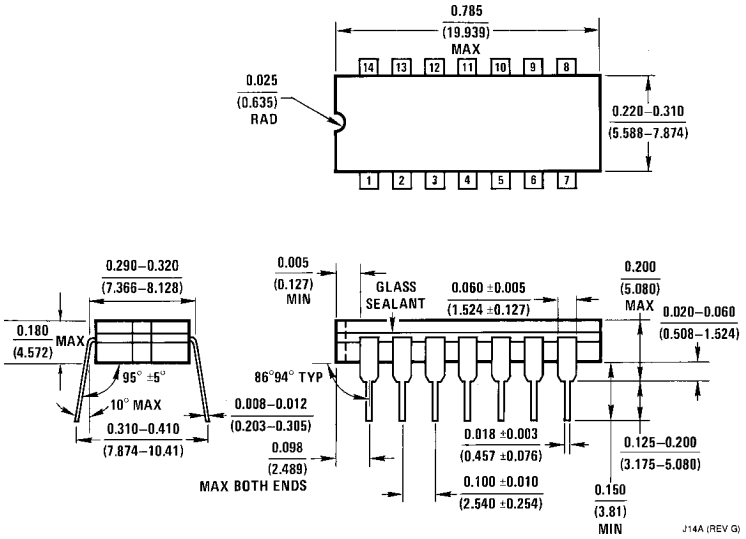
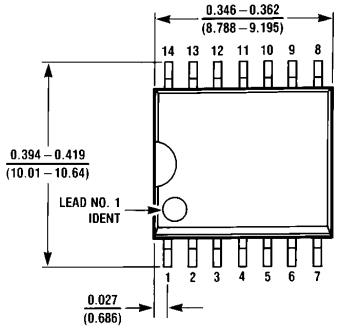


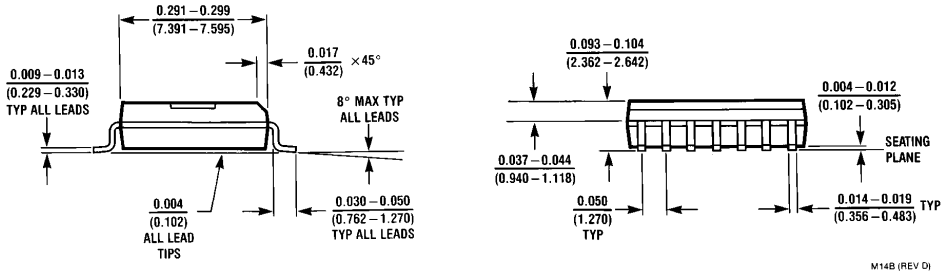
FIGURE 16. 50 Hz and 150 Hz Notch Filter

Physical Dimensions inches (millimeters)



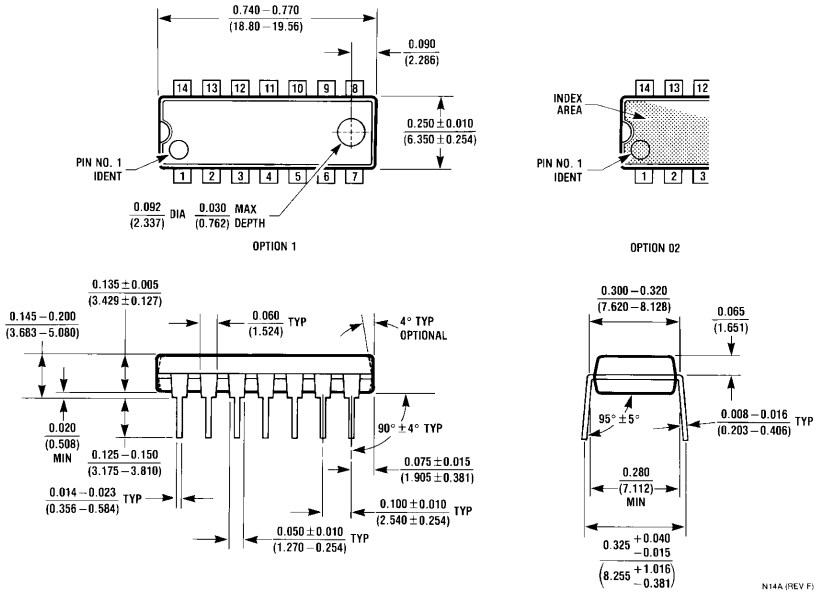
14 Lead Ceramic Dual-In-Line Package (J)
Order Number LMF90CIJ, LMF90CMJ, LMF90CMJ/883 or LMF90CCJ
NS Package Number J14A





14 Lead Molded Package, Small Outline, 0.300″ Wide
Order Number LMF90CCWM or LMF90CIWM
NS Package Number M14B

Physical Dimensions inches (millimeters) (Continued)



14 Lead Molded Dual-In-Line Package (N)
Order Number LMF90CCN or LMF90CIN
NS Package Number N14A

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