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National
Semiconductor

MICROCIRCUIT DATA SHEET

MNLMH6628-X-RH REV 0A0

Original Creation Date: 04/29/03
Last Update Date: 05/13/03
Last Major Revision Date:

DUAL WIDEBAND, LOW-NOISE, VOLTAGE FEEDBACK OP AMP, GUARANTEED TO 300k rd(Si) TESTED TO MIL-STD-883, METHOD 1019

General Description

The National LMH6628 is a high speed dual op amp that offers a traditional voltage feedback topology featuring unity-gain stability and slew-enhanced circuitry. The LMH6628's low noise and very low harmonic distortion combine to form a very wide dynamic range op amp that operates from a single (5 to 12V) or dual (±5V) power supply.

Each of the LMH6628's closely matched channels provides a 300MHz unity gain bandwidth and low input voltage noise density (2nV/SqRtHz). Low 2nd/3rd harmonic distortion (-65/-74dBc at 10MHz) makes the LMH6628 a perfect wide dynamic-range amplifier for matched I/Q channels.

With its fast and accurate settling (12ns to 0.1%), the LMH6628 is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of hi resolution analog-to-digital converters. Combining the LMH6628's two tightly matched amplifiers in a single package reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

The LMH6628 is fabricated using National's VIP 10 (TM) comlimentary bipolar process.

Industry Part Number

LMH6628

Prime Die

LMH6628A

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

LMH6628J-QML
LMH6628J-QMLV
LMH6628JFQML
LMH6628JFQMLV
LMH6628WG-QML
LMH6628WG-QMLV
LMH6628WGFQML
LMH6628WGFQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

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Features

- Wide unity-gain bandwidth: 300 MHz
- Low noise: 2.0nV/SqRtHz
- Low distortion: -65/-74dBc (10MHz)
- Settling time: 12ns to 0.1%
- Wide supply voltage range: ±2.5V to ±6V
- High output current ±85mA
- Improved replacement for CLC428

CONTROLLING DOCUMENTS:

LMH6628J-QML	5962-0254501MPA
LMH6628J-QMLV	5962-0254501VPA
LMH6628JFQML	5962F0254501MPA
LMH6628JFQMLV	5962F0254501VPA
LMH6628WG-QML	5962-0254501MZA
LMH6628WG-QMLV	5962-0254501VZA
LMH6628WGFQML	5962F0254501MZA
LMH6628WGFQMLV	5962F0254501VZA

Applications

- High speed dual op amp
- Low noise integrators
- Low noise active filters
- Driver/receiver for transmission systems
- High-speed detectors
- I/Q channel amplifiers

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage		±7V dc
Maximum Junction temperature (Note 2)		+175 C
Lead temperature Soldering, 10 seconds		+300 C
Differential input voltage		V+ - V-
Common mode input voltage		V+ - V-
Storage temperature range		-65 C ≤ Ta ≤ +150 C
Power Dissipation (Note 2)		1.0W
Short circuit current (Note 3)		
Thermal Resistance		
ThetaJA		
Ceramic DIP	(Still Air)	135 C/W
	(500LF/Min Air Flow)	75 C/W
Ceramic SOIC	(Still Air)	200 C/W
	(500LF/Min Air Flow)	145 C/W
ThetaJC		
Ceramic DIP		30 C/W
Ceramic SOIC		19 C/W
Package Weight (typical)		
Ceramic DIP		TBD
Ceramic SOIC		TBD
ESD Tolerance (Note 4)		4000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperatuer). The maximum allowable power dissipation at any temperatuer is Pdmax = (Tjmax -TA) / ThetaJA or the number given in the Absoulute Maximum Ratings, whichever is lower.

Note 3: Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

Note 4: Human body model, 1.5k Ohms in series with 100pF.

Recommended Operating Conditions

Supply Voltage	±2.5V to ±6.0V
Ambient Operating Temperture Range	-55 C ≤ Ta ≤ +125 C

Electrical Characteristics

DC PARAMETERS: Static and DC Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±5V dc, Av = +2, Rl = 100 Ohms, Rf = 100 Ohms, -55 C ≤ Ta ≤ +125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ib	Input Bias Current		3		-10	+10	uA	1
					-20	+20	uA	2
					-20	+20	uA	3
Vio	Input Offset Voltage		3		-2	+2	mV	1
					-2.6	+2.6	mV	2, 3
Icc	Supply Current	Rl = infinity	3			24	mA	1
						24	mA	2
						25	mA	3
PSRR	Power Supply Rejection Ration	+Vs = +4.0V to +5.0v, -Vs = -4.0V to -5.0V			60		dB	1
					55		dB	2, 3
Vout	Output Voltage Range	Rl = Infinity			-5.0	+5.0	V	1, 2, 3

AC PARAMETERS: Frequeuncy Domain Response

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = ±5V dc, Av = +2, Rl = 100 Ohms, Rf = 100 Ohms, -55 C ≤ Ta ≤ +125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small Signal Bandwith	-3 dB bandwidth, Vout < 0.5 Vpp	2		50		MHz	4
GFP	Gain Flatness Peaking	0.1 MHz to 200 MHz, Vout ≤0.5 Vpp	2			0.6	dB	4
GFR	Gain Flatness Rolloff	0.1 MHz to 20 MHz, Vout ≤0.5 Vpp	2			0.6	dB	4
Aol	Open Loop Gain		2		55		dB	4

AC PARAMETERS: Distortion and Noise Tests.

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = ±5V dc, Av = +2, Rl = 100 Ohms, Rf = 100 Ohms, -55 C ≤ Ta ≤ +125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	Second Harmonic Distortion	1 Vpp at 10 MHz	2			50	dBc	4
HD3	Third Harmonic Distortion	1 Vpp at 10 MHz	2			60	dBc	4

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: " Deltas not required on B-Level product. Deltas required for S-Level product at Group B5 ONLY, or as specified on the Internal Processing Instructions (IPI).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ib	Input Bias Current		1		-1.0	+1.0	uA	1
Vio	Input Offset Voltage		1		-0.2	+0.2	mV	1
Icc	Supply Current	Rl = Infinity	1		-1	+1	mA	1

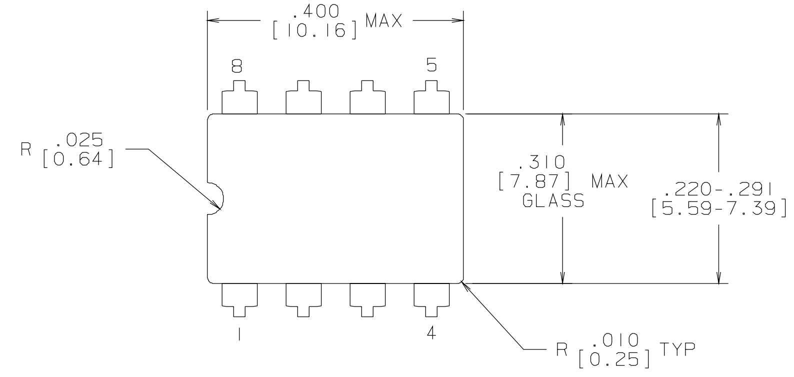
Note 1: If not tested, shall be guaranteed to the limits specified in table 1.
Note 2: Group A testing only.
Note 3: Pre and post irradiation limits are identical to those listed under electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.

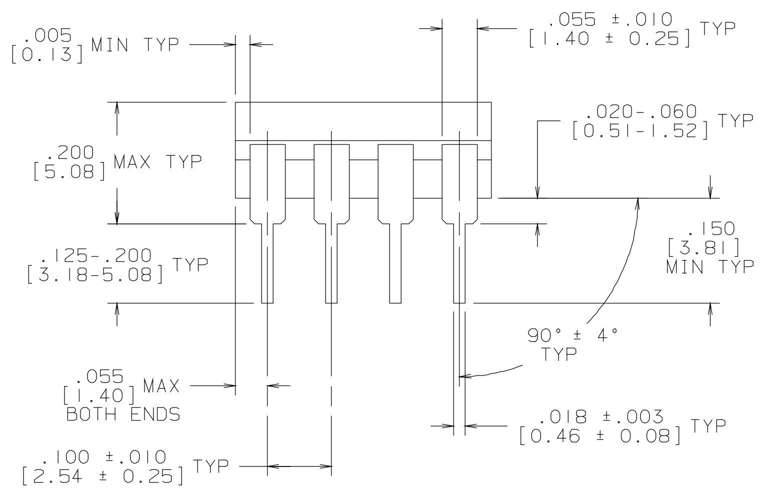
Graphics and Diagrams

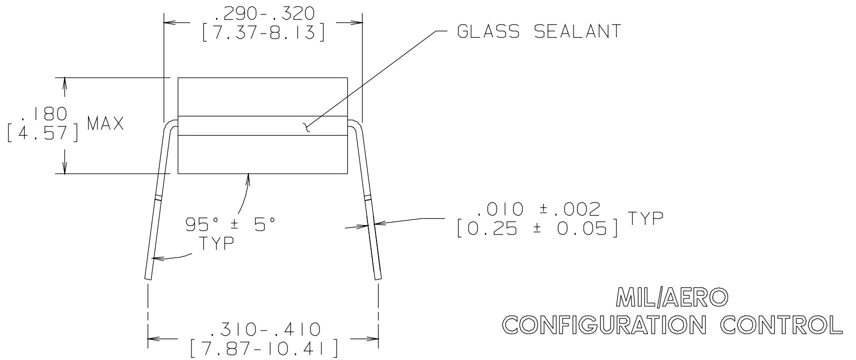
GRAPHICS#	DESCRIPTION
06403HRA1	CERAMIC SOIC (WG), 10 LEAD (B/I CKT)
07082HRA4	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000480A	CERDIP (J), 8 LEAD (PIN OUT)
P000484A	CERAMIC SOIC (WG), 10 LEAD (PIN OUT)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

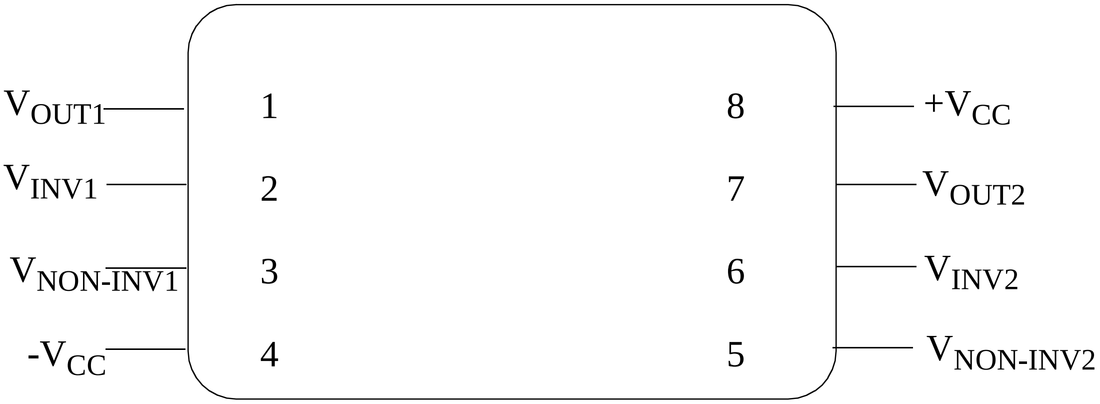
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING SHEET 1 OF 1



LMH6628J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000480A

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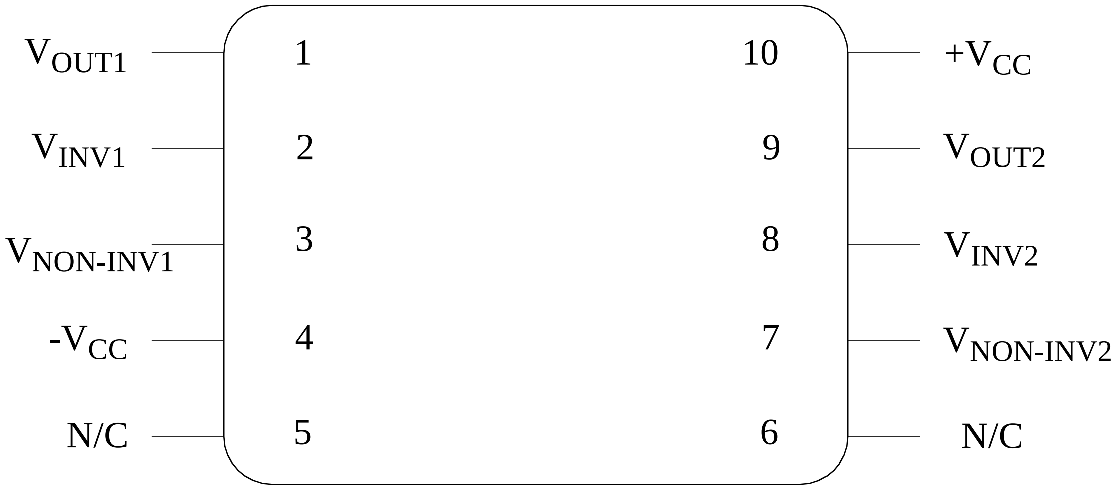

LMH6628WG

10 - LEAD CERAMIC SOIC

CONNECTION DIAGRAM

TOP VIEW

P000484A

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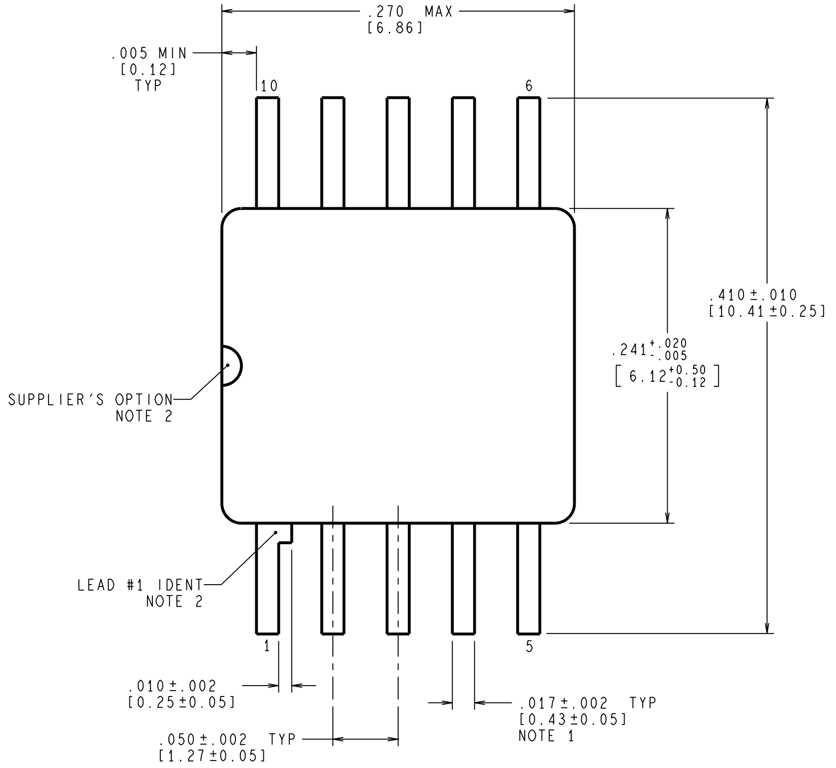
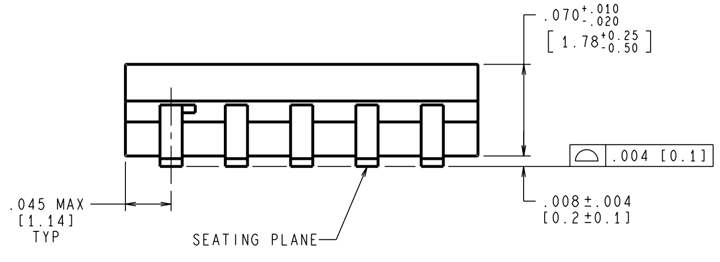
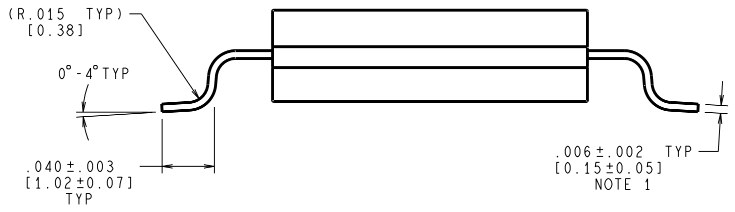
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

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CERPACK,
10 LEAD,
GULL WING

PROJECTION
INCH
[MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	**C**	**(SC)MKT-WG10A**	**C**

DO NOT SCALE DRAWING
SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0004149	05/13/03	Rose Malone	Initial MDS Release: MNLMH6628-X-RH, Rev. 0A0