National Semiconductor

March 2004

LMV7291
Single 1.8V Low Power Comparator with Rail-to-Rail Input

General Description

The LMV7291 is a rail-to-rail input low power comparator, characterized at supply voltage 1.8V, 2.7V and 5.0V. It consumes only 9uA supply current per channel while achieving a 800ns propagation delay.

The LMV7291 is available in SC70 package. With this tiny package, the PC board area can be significantly reduced. It is ideal for low voltage, low power and space critical designs.

The LMV7291 features a push-pull output stage which allows operation with minimum power consumption when driving a load.

The LMV7291 is built with National Semiconductor's advance submicron silicon-gate BiCMOS process. It has bipolar inputs for improved noise performance and CMOS outputs for rail-to-rail output swing.

Features

(V_S = 1.8V, T_A = 25˚C, Typical values unless specified).

- Single Supply
- Ultra low supply current — 9µA per channel
- Low input bias current — 10nA
- Low input offset current — 200pA
- Low guaranteed V_{OS} — 4mV
- Propagation delay — 880ns (20mV overdrive)
- Input common mode voltage range — 0.1V beyond rails

Applications

- Mobile communications
- Laptops and PDA's
- Battery powered electronics
- General purpose low voltage applications

Typical Circuit

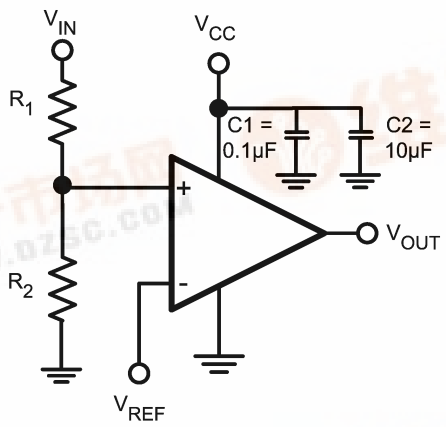


FIGURE 1. Threshold Detector

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2)
	200V (Note 6)
V_{IN} Differential	±Supply Voltage
Supply Voltage (V^+ - V^-)	5.5V
Voltage at Input/Output pins	V^+ +0.1V, V^- –0.1V
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C
Storage Temperature Range	–65˚C to +150˚C
Junction Temperature (Note 4)	+150˚C

Operating Ratings (Note 1)

Operating Temperature Range (Note 3)	–40˚C to +85˚C
Package Thermal Resistance (Note 3)	
SC-70	265˚C/W

1.8V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 1.8V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 0.9V (Note 7)		10		uV/C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current	LMV7291		9	12 **14**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0.9V	3.5	6		mA
		Sinking, V_O = 0.9V	4	6		
V_{OH}	Output Voltage High	I_O = 0.5mA	1.7	1.74		V
		I_O = 1.5mA	1.58	1.63		
V_{OL}	Output Voltage Low	I_O = –0.5mA		52	70	mV
		I_O = –1.5mA		166	220	
V_{CM}	Input Common Mode Voltage Range	CMRR > 45 dB			1.9	V
			–0.1			V
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 1.8V	47	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 1.8V		2		pA

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 1.8V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		880		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		570		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1100		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		800		ns

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 1.35V (Note 7)		10		µV/C
I_B	Input Bias Current			10		nA
I_{OS}	Input offset Current			200		pA
I_S	Supply Current	LMV7291		9	13 **15**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 1.35V	12	15		mA
		Sinking, V_O = 1.35V	12	15		
V_{OH}	Output Voltage High	I_O = 0.5mA	2.63	2.66		V
		I_O = 2.0mA	2.48	2.55		
V_{OL}	Output Voltage Low	I_O = –0.5mA		50	70	mV
		I_O = –2mA		155	220	
V_{CM}	Input Common Voltage Range	CMRR > 45dB			2.8	V
			–0.1			V
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 2.7V	47	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 2.7V		2		pA

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		1200		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		810		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1300		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		860		ns

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage			0.3	4 **6**	mV
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 2.5V (Note 7)		10		µV/C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current	LMV7291		10	14 **16**	µA
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 2.5V	28	34		mA
		Sinking, V_O = 2.5V	28	34		

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OH}	Output Voltage High	I_O = 0.5mA	4.93	4.96		V
		I_O = 4.0mA	4.70	4.77		
V_{OL}	Output Voltage Low	I_O = –0.5mA		27	70	mV
		I_O = –4.0mA		225	300	
V_{CM}	Input Common Voltage Range	CMRR > 45dB			5.1	V
			–0.1			
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 5.0V	47	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 5V		2		pA

5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5.0V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2 and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ		2100		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		1380		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ		1800		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ		1100		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: Typical values represent the most likely parametric norm.

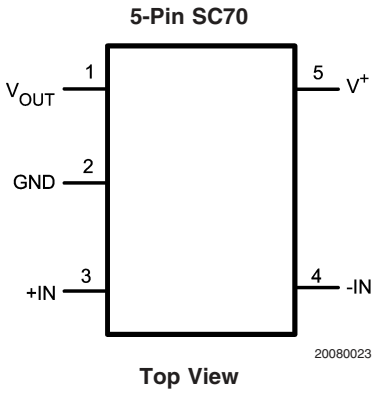
Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: Machine Model, 0Ω in series with 200pF.

Note 7: Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Note 8: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

Connection Diagram



Top View

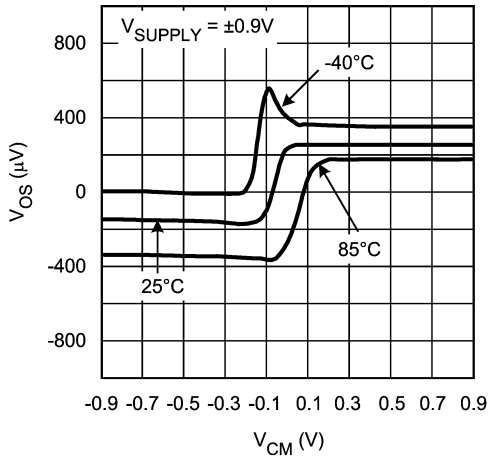
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SC70	LMV7291MG	C36	1k Units Tape and Reel	MAA05A
	LMV7291MGX		3k Units Tape and Reel	

Typical Performance Characteristics

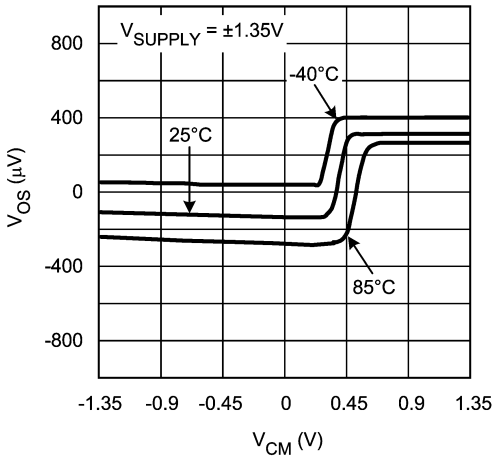
(T_A = 25˚C, Unless otherwise specified).

V_{OS} vs. V_{CM}



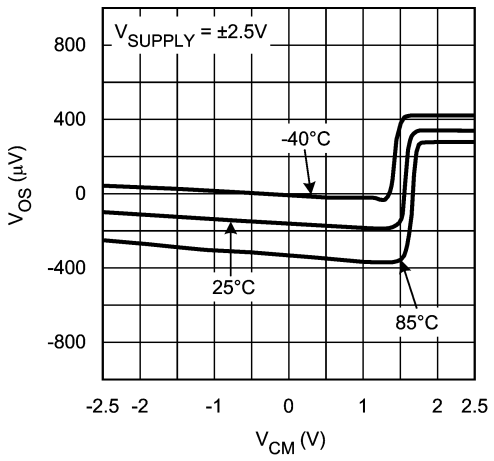
20080028

V_{OS} vs. V_{CM}



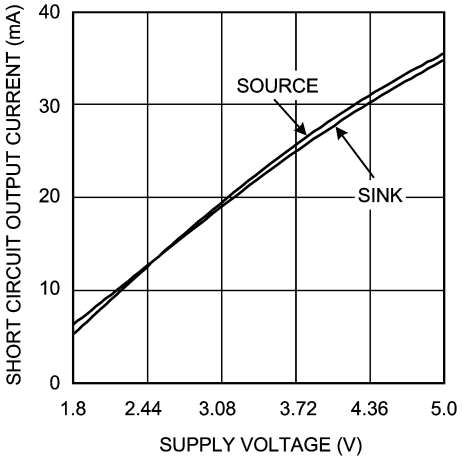
20080029

V_{OS} vs. V_{CM}



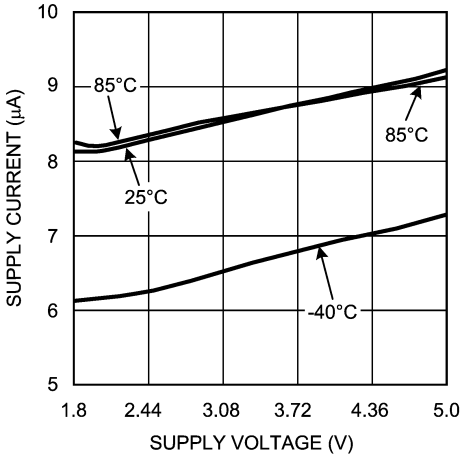
20080030

Short Circuit vs. Supply Voltage



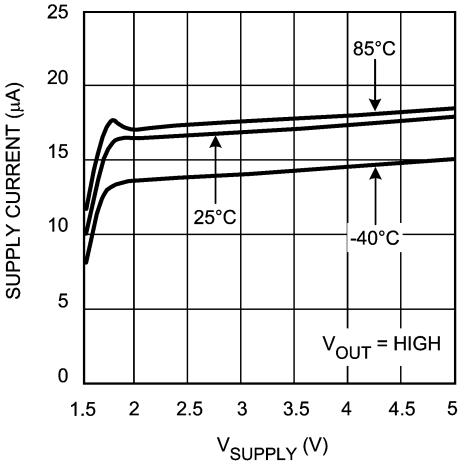
20080001

Supply Current vs. Supply Voltage



20080002

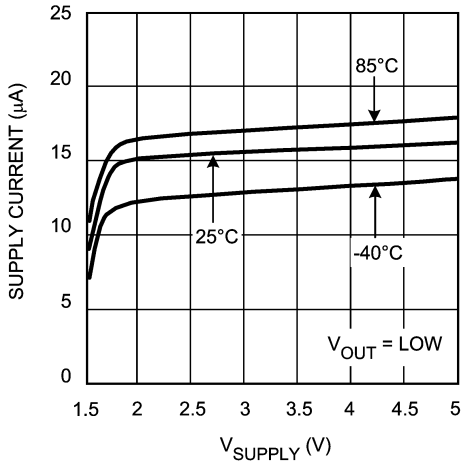
Supply Current vs. Supply Voltage



20080031

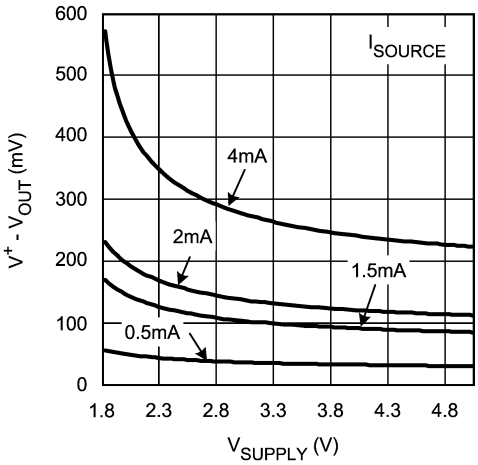
Typical Performance Characteristics (T_A = 25˚C, Unless otherwise specified). (Continued)

Supply Current vs. Supply Voltage



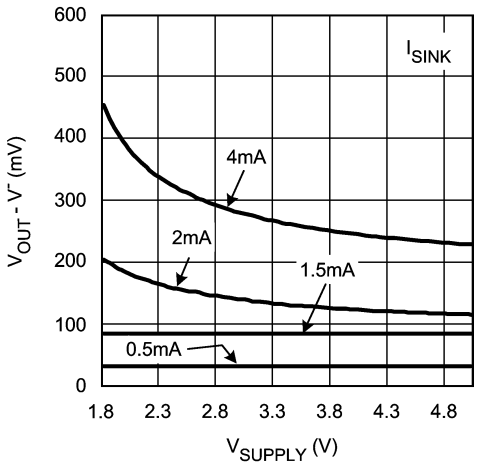
20080032

Output Positive Swing vs. V_{SUPPLY}



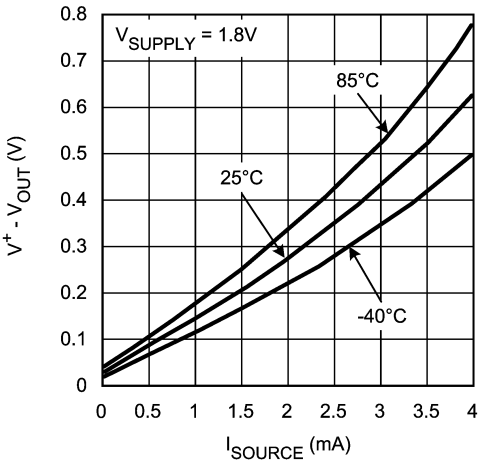
20080033

Output Negative Swing vs. V_{SUPPLY}



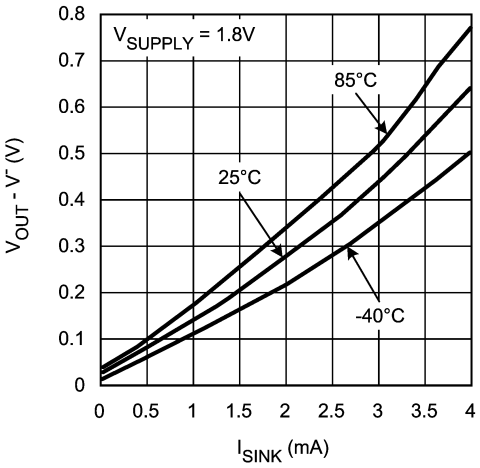
20080034

Output Positive Swing vs. I_{SOURCE}



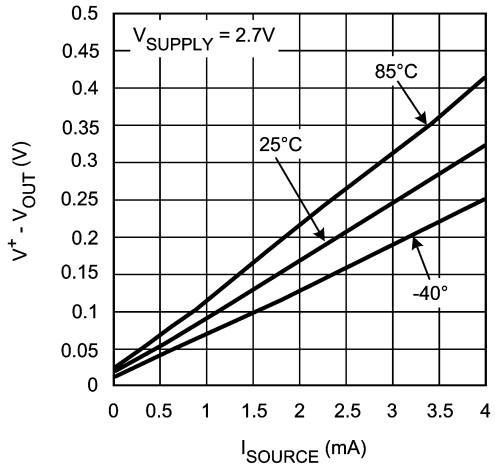
20080035

Output Negative Swing vs. I_{SINK}



20080036

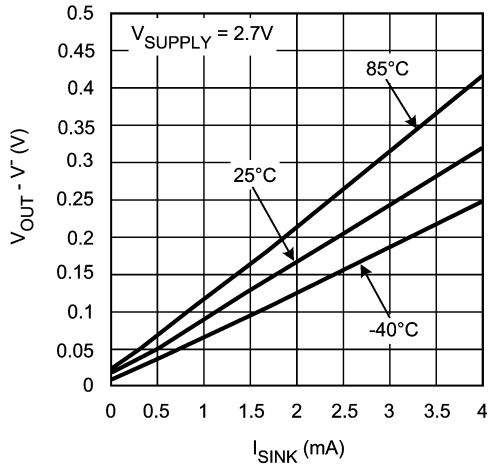
Output Positive Swing vs. I_{SOURCE}



20080037

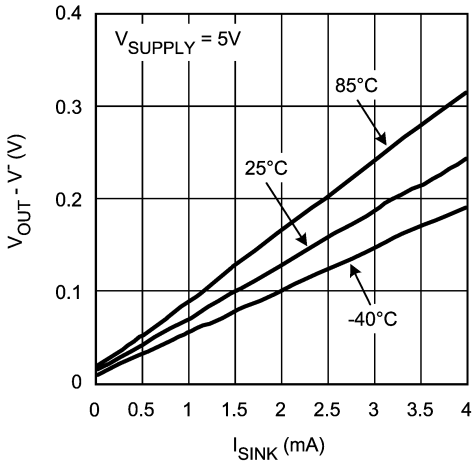
Typical Performance Characteristics (T_A = 25˚C, Unless otherwise specified). (Continued)

Output Negative Swing vs. I_{SINK}



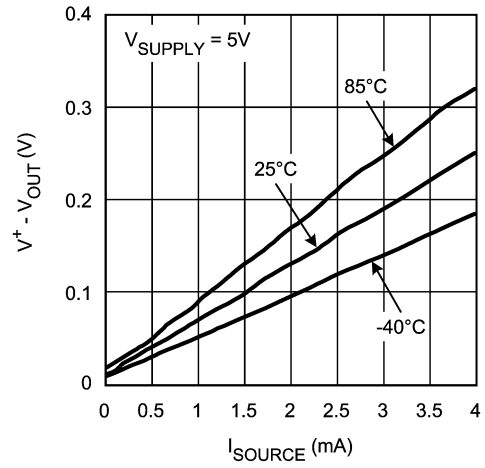
20080038

Output Negative Swing vs. I_{SINK}



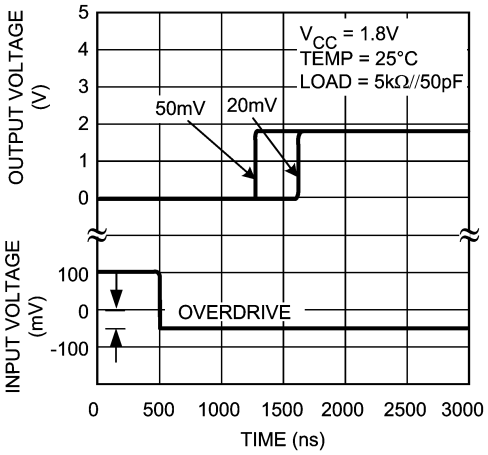
20080039

Output Positive Swing vs. I_{SOURCE}



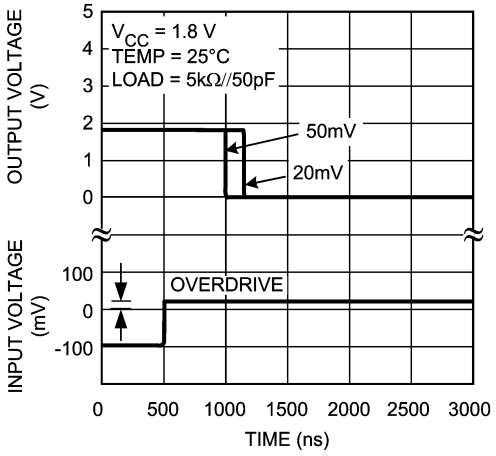
20080040

Propagation Delay (t_{PLH})



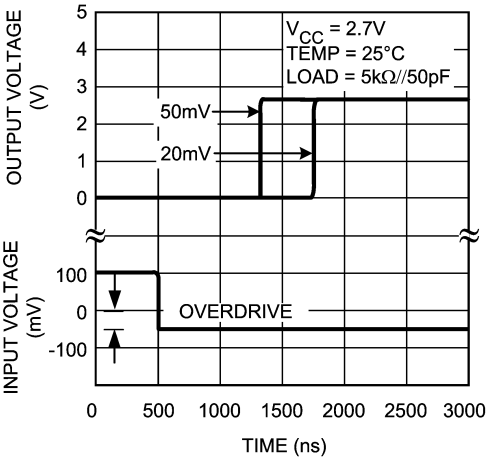
20080014

Propagation Delay (t_{PHL})



20080018

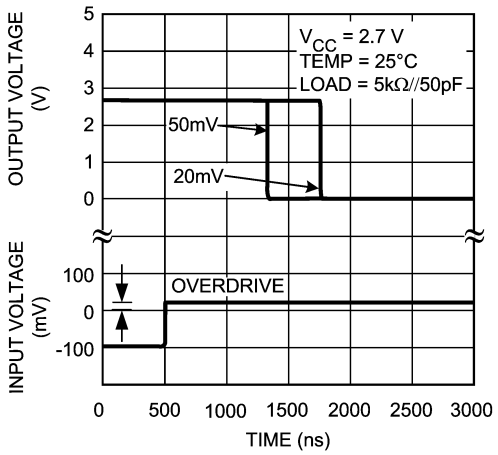
Propagation Delay (t_{PLH})



20080015

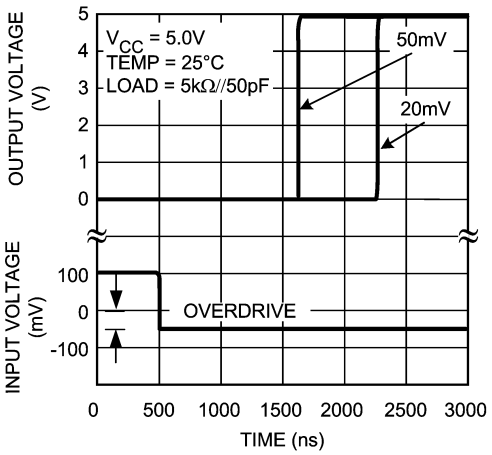
Typical Performance Characteristics (T_A = 25˚C, Unless otherwise specified). (Continued)

Propagation Delay (t_{PHL})



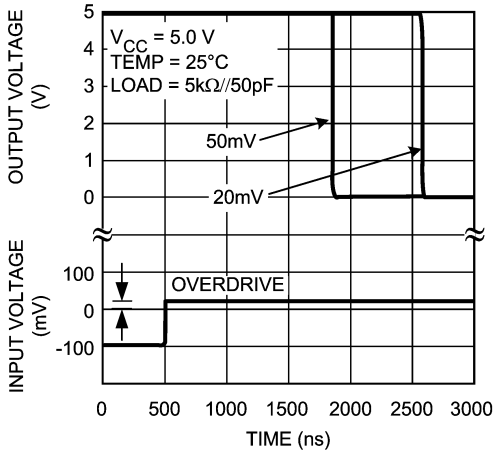
20080020

Propagation Delay (t_{PLH})



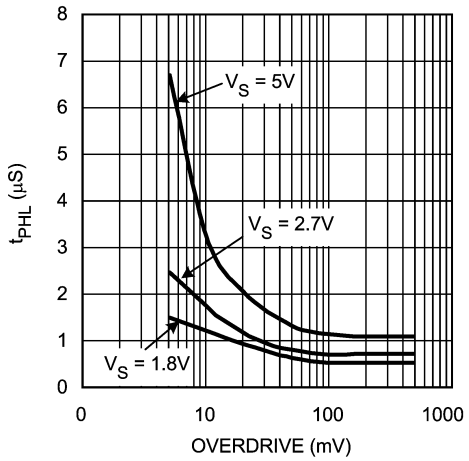
20080016

Propagation Delay (t_{PHL})



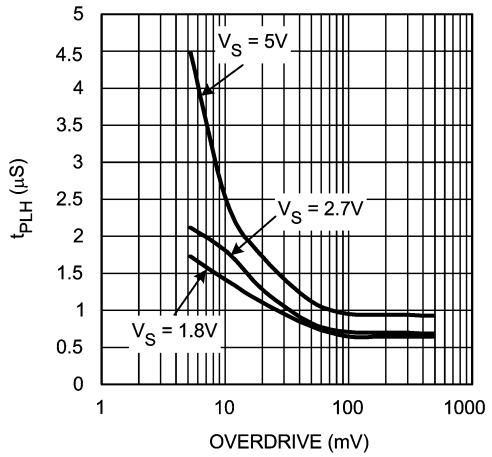
20080022

t_{PHL} vs. Overdrive



20080050

t_{PLH} vs. Overdrive



20080049

Application Notes

BASIC COMPARATOR

A comparator is often used to convert an analog signal to a digital signal. As shown in *Figure 2*, the comparator compares an input voltage (V_{IN}) to a reference voltage (V_{REF}). If V_{IN} is less than V_{REF}, the output (V_O) is low. However, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is high.

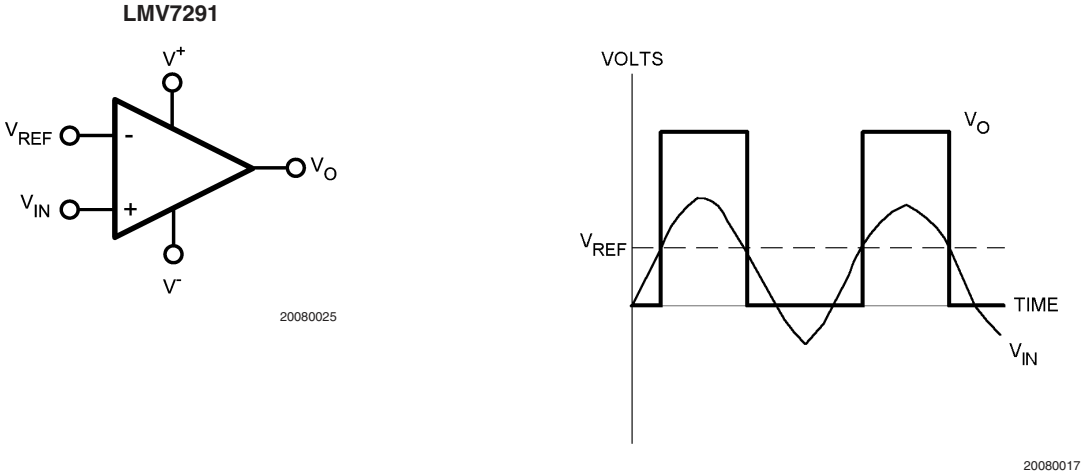


FIGURE 2. LMV7291 Basic Comparator

RAIL-TO-RAIL INPUT STAGE

The LMV7291 has an input common mode voltage range (V_{CM}) of −0.1V below the V^- to 0.1V above V^+. This is achieved by using paralleled PNP and NPN differential input pairs. When the V_{CM} is near V^+, the NPN pair is on and the PNP pair is off. When the V_{CM} is near V^-, the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around 950mV from V^+. Since each input stage has its own offset voltage (V_{OS}), the V_{OS} of the comparator becomes a function of the V_{CM}. See curves for V_{OS} vs. V_{CM} in Typical Performance Characteristics section. In application design, it is recommended to keep the V_{CM} away from the crossover point to avoid problems. The wide input voltage range makes LMV7291 ideal in power supply monitoring circuits, where the comparators are used to sense signals close to gnd and power supplies.

OUTPUT STAGE

The LMV7291 has a push-pull output stage. This output stage keeps the total system power consumption to the absolute minimum. The only current consumed is the low supply current and the current going directly into the load. When output switches, both PMOS and NMOS at the output stage are on at the same time for a very short time. This allows current to flow directly between V^+ and V^- through output transistors. The result is a short spike of current (shoot-through current) drawn from the supply and glitches in the supply voltages. The glitches can spread to other parts of the board as noise. To prevent the glitches in supply lines, power supply bypass capacitors must be installed. See section for supply bypassing in the Application Notes for details.

HYSTERESIS

It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier of its own noise.

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage V_{CC} of the comparator (*Figure 3*). When V_{IN} at the inverting input is less than V_A, the voltage at the non-inverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1||R_3$ in series with R_2. The lower input trip voltage V_{A1} is defined as

$$V_{A1} = \frac{V_{CC}\, R_2}{(R_1||R_3) + R_2}$$

When V_{IN} is greater than V_A ($V_{IN} > V_A$), the output voltage is low and very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{A2} is defined as

$$V_{A2} = \frac{V_{CC}\, (R_2||R_3)}{R_1 + (R_2||R_3)}$$

The total hysteresis provided by the network is defined as

$$\Delta V_A = V_{A1} - V_{A2}$$

A good typical value of ΔV_A would be in the range of 5 to 50 mV. This is easily obtained by choosing R_3 as 1000 to 100 times ($R_1||R_2$) for 5V operation, or as 300 to 30 times ($R_1||R_2$) for 1.8V operation.

Application Notes (Continued)

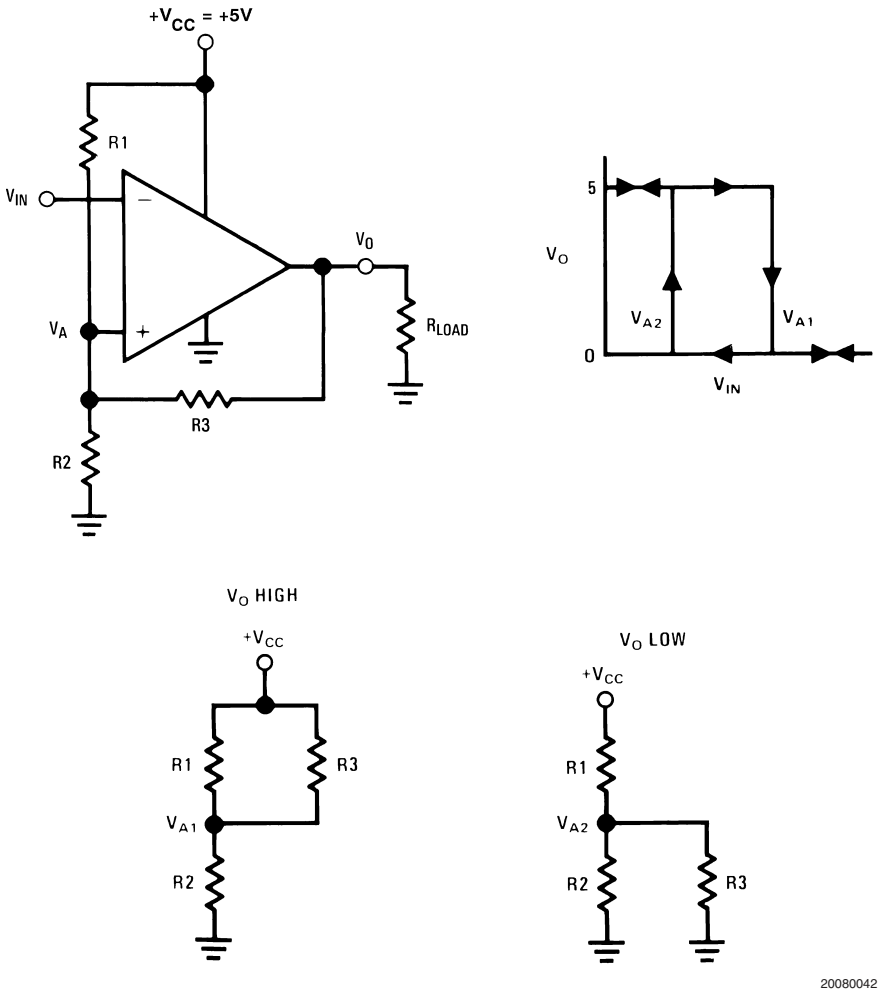


FIGURE 3. Inverting Comparator with Hysteresis

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input (*Figure 4*). When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}, where V_{IN1} is calculated by

$$V_{in1} = \frac{V_{ref}(R_1 + R_2)}{R_2}$$

When V_{IN} is high, the output is also high. To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN} can be calculated by:

$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC} R_1}{R_2}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{CC} R_1 / R_2$$

Application Notes (Continued)

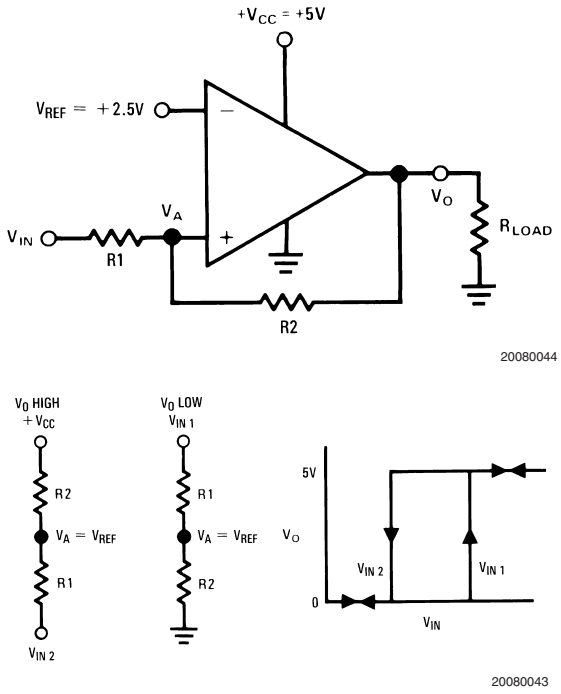


FIGURE 4. Non-Inverting Comparator with Hysteresis

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and transient response. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to mis-operate. To avoid problems, a small bypass capacitor, such as 0.1uF ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8µF or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In dual supply application, a 0.1µF capacitor is recommended to be placed across V^+ and V^- pins.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).
3. It is a good practice to use an unbroken ground plane on a printed circuit board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.
4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard.
5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.
6. All pins of any unused comparators should be tied to the negative supply.

Typical Applications

POSITIVE PEAK DETECTOR

A positive peak detect circuit is basically a comparator operated in a unity gain follower configuration, with a capacitor as a load to maintain the highest voltage. A diode is added at the output to prevent the capacitor from discharging through the output, and a 1MΩ resistor added in parallel to the capacitor to provide a high impedance discharge path. When the input V_{IN} increases, the inverting input of the comparator follows it, thus charging the capacitor. When it decreases, the cap discharges through the 1MΩ resistor. The decay time can be modified by changing the resistor. The output should be accessed through a follower circuit to prevent loading.

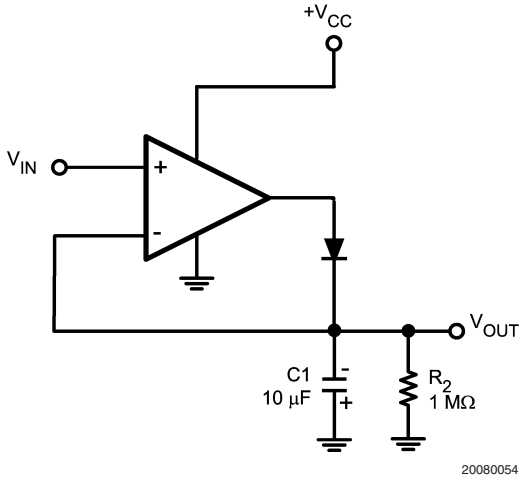


FIGURE 5. Positive Peak Detector

NEGATIVE PEAK DETECTOR

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. Since there is no pull-up resistor, the only discharge path will be the 1MΩ resistor and any load impedance used. Decay time is changed by varying the 1MΩ resistor.

Typical Applications (Continued)

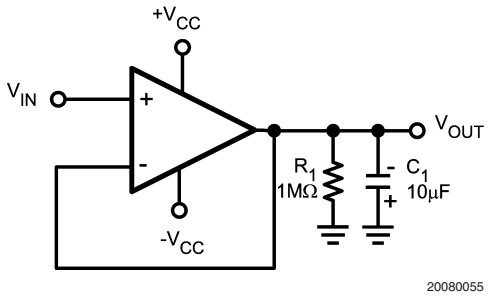


FIGURE 6. Negative Peak Detector

SQUARE WAVE GENERATOR

A typical application for a comparator is as a square wave oscillator. The circuit below generates a square wave whose period is set by the RC time constant of the capacitor $C_1$and resistor R_4. The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.

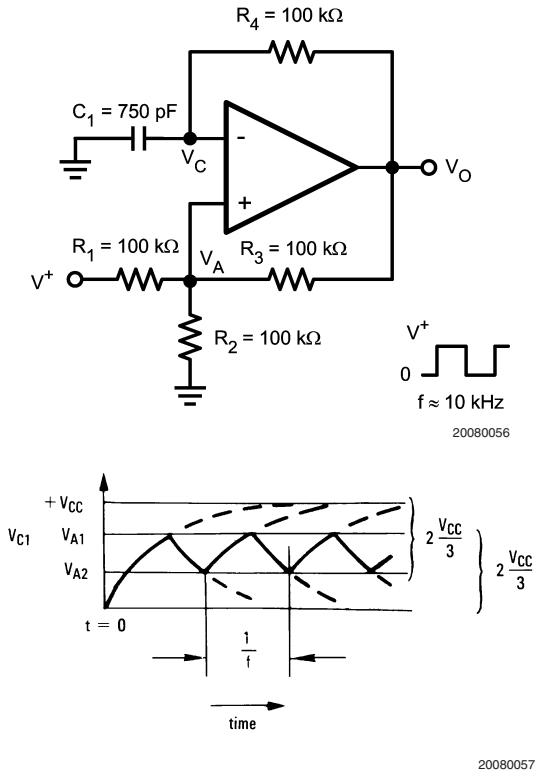


FIGURE 7. Squarewave Oscillator

To analyze the circuit, consider it when the output is high. That implies that the inverted input (V_C) is lower than the non-inverting input (V_A). This causes the C_1 to get charged through R_4, and the voltage V_C increases till it is equal to the non-inverting input. The value of V_A at this point is

$$V_{A1} = \frac{V_{CC}.R_2}{R_2 + R_1||R_3}$$

If $R_1 = R_2 = R_3$ then $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

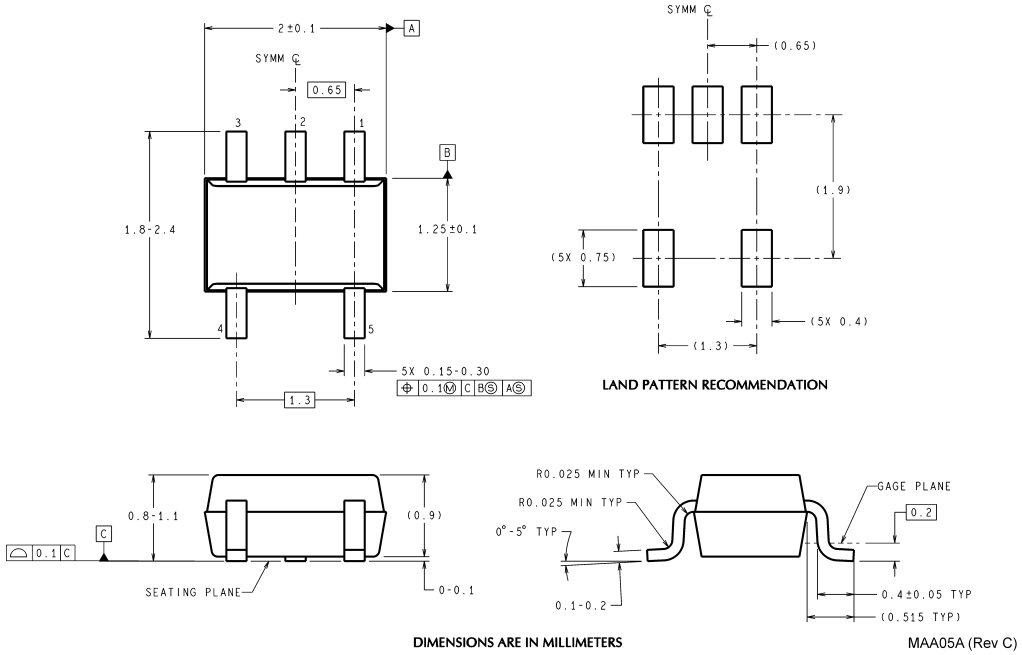
$$V_{A2} = \frac{V_{CC}\,(R_2||R_3)}{R_1 + (R_2||R_3)}$$

If $R_1 = R_2 = R_3$ then $V_{A2} = V_{CC}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1.\ln 2$. Hence the formula for the frequency is:

$F = 1/(2.R_4.C_1.\ln 2)$

Physical Dimensions inches (millimeters)
unless otherwise noted



5-Pin SC70
NS Package Number MAA05A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560

www.national.com