National Semiconductor

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LMX2531
PLLatinum™ High Performance Frequency Synthesizer System with Integrated VCO

General Description

The LMX2531 is a low power, high performance frequency synthesizer system which includes a fully integrated delta-sigma PLL and VCO with fully integrated tank circuit. The third and fourth poles are also integrated and also adjustable. Also included are integrated ultra-low noise and high precision LDOs for the PLL and VCO which give higher supply noise immunity and also more consistent performance. When combined with a high quality reference oscillator, the LMX2531 generates very stable, low noise local oscillator signals for up and down conversion in wireless communication devices. The LMX2531 is a monolithic integrated circuit, fabricated in an advanced BiCMOS process. There are actually several different versions of this product, for which the primary difference is frequency range.

Device programming is facilitated using a three-wire MICROWIRE Interface that can operate down to 1.8 volts.

Supply voltage range is 2.8 to 3.2 Volts. The LMX2531 is available in a 36 pin 6x6x0.8 mm Lead-Free Leadless Leadframe Package (LLP).

Target Applications

- 3G Cellular Base Stations (WCDMA, TD-SCDMA,CDMA2000)
- 2G Cellular Base Stations (GSM/GPRS, EDGE, CDMA1xRTT)
- Wireless LAN
- Broadband Wireless Access
- Satellite Communications
- Wireless Radio
- Automotive
- CATV Equipment
- Instrumentation and Test Equipment
- RFID Readers

Features

Multiple Frequency Options Available
- — See Selection Guide Below
- — Frequencies from: 765 MHz - 2790 MHz

PLL Features
- — Fractional-N Delta Sigma Modulator Order programmable up to 4th order
- — FastLock/Cycle Slip Reduction with Timeout Counter
- — Partially integrated, adjustable Loop Filter
- — Very low phase noise and spurs

VCO Features
- — Integrated tank inductor
- — Low phase noise

Other Features
- — 2.8 V to 3.2 V Operation
- — Low Power-Down Current
- — 1.8V MICROWIRE Support
- — Package: 36 Lead LLP

Part	Low Band	High Band
LMX2531LQ1570E	765 - 818 MHz	1530 - 1636 MHz
LMX2531LQ1650E	795 - 850 MHz	1590 - 1700 MHz
LMX2531LQ1700E	831 - 885 MHz	1662 - 1770 MHz
LMX2531LQ1778E	863 - 920 MHz	1726 - 1840 MHz
LMX2531LQ1910E	917 - 1014 MHz	1834 - 2028 MHz
LMX2531LQ2080E	952 - 1137 MHz	1904 - 2274 MHz
LMX2531LQ2265E	1089 - 1200 MHz	2178 - 2400 MHz
LMX2531LQ2570E	1168 - 1395 MHz	2336 - 2790 MHz

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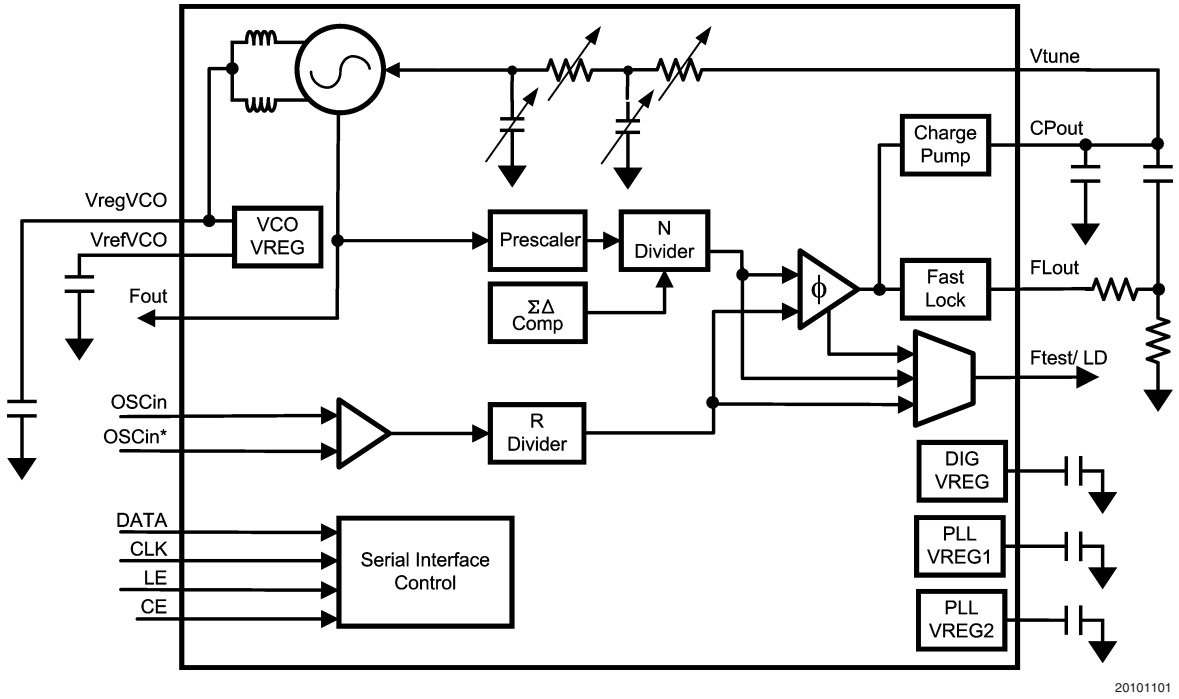
Functional Block Diagram



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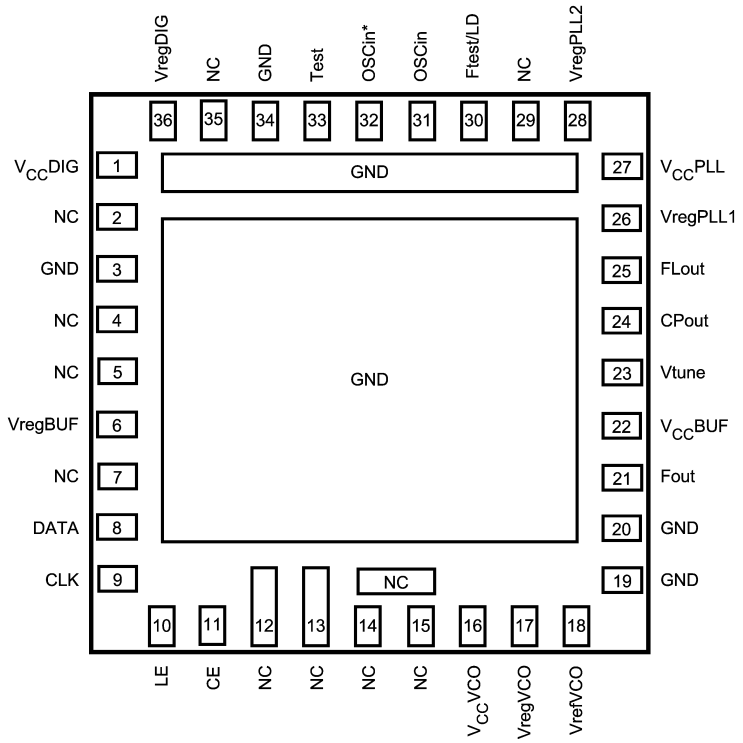
Connection Diagram

36-Pin LLP (LQ) Package



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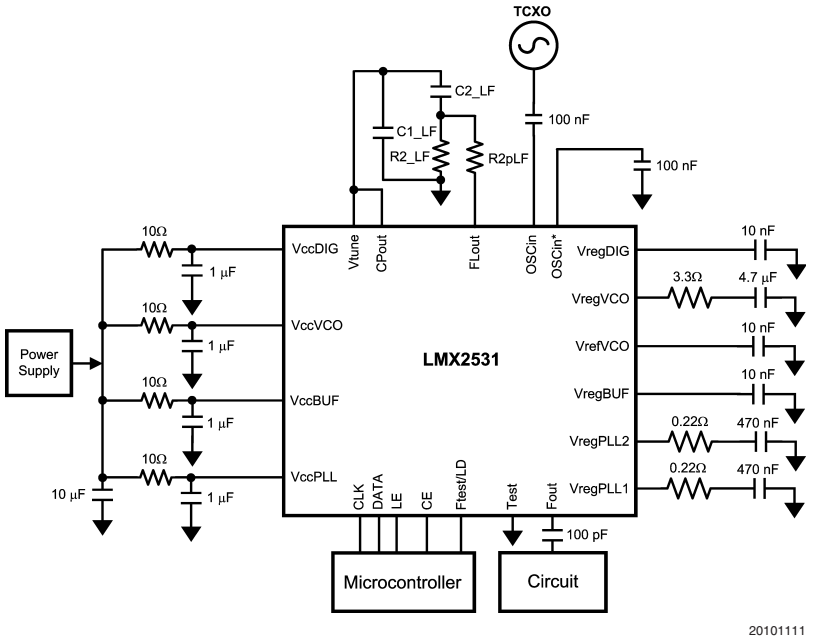
Pin Descriptions

Pin Number	Pin Name	I/O	Description
1	VccDIG	-	Power Supply for digital LDO circuitry. Input may range from 2.8 - 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
3	GND	-	Ground
2,4,5,7, 12, 13, 29, 35	NC	-	No Connect.
6	VregBUF	-	Internally regulated voltage for the VCO buffer circuitry. Connect to ground with a capacitor.
8	DATA	I	MICROWIRE serial data input. High impedance CMOS input. This pin must not exceed 2.75V. Data is clocked in MSB first. The last bits clocked in form the control or register select bits.
9	CLK	I	MICROWIRE clock input. High impedance CMOS input. This pin must not exceed 2.75V. Data is clocked into the shift register on the rising edge.
10	LE	I	MICROWIRE Latch Enable input. High impedance CMOS input. This pin must not exceed 2.75V. Data stored in the shift register is loaded into the selected latch register when LE goes HIGH.
11	CE	I	Chip Enable Input. High impedance CMOS input. This pin must not exceed 2.75V. When CE is brought high the LMX2531 is powered up corresponding to the internal power control bits. It is necessary to reprogram the R0 register to get the part to re-lock.
14, 15	NC	-	No Connect. Do NOT ground.
16	VccVCO	-	Power Supply for VCO regulator circuitry. Input may range from 2.8 - 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
17	VregVCO	-	Internally regulated voltage for VCO circuitry. Not intended to drive an external load. Connect to ground with a capacitor and some series resistance.
18	VrefVCO	-	Internal reference voltage for VCO LDO. Not intended to drive an external load. Connect to ground with a capacitor.
19	GND	-	Ground for the VCO circuitry.
20	GND	-	Ground for the RF Output Buffer circuitry.
21	Fout	O	Buffered RF Output for the VCO.
22	VccBUF	-	Power Supply for the VCO Buffer circuitry. Input may range from 2.8 - 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
23	Vtune	I	Tuning voltage input for the VCO. For connection to the CPout Pin through an external passive loop filter.
24	CPout	O	Charge pump output for PLL. For connection to Vtune through an external passive loop filter.
25	FLout	O	An open drain NMOS output which is used for FastLock or a general purpose output.
26	VregPLL1	-	Internally regulated voltage for PLL charge pump. Not intended to drive an external load. Connect to ground with a capacitor.
27	VccPLL	-	Power Supply for the PLL. Input may range from 2.8 - 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
28	VregPLL2	-	Internally regulated voltage for RF digital circuitry. Not intended to drive an external load. Connect to ground with a capacitor.
30	Ftest/LD	O	Multiplexed CMOS output. Typically used to monitor PLL lock condition.
31	OSCin	I	Oscillator input. The oscillator can be placed in either single-ended or differential mode of operation.
32	OSCin*	I	Oscillator complimentary input. When a single ended source is used, then a bypass capacitor should be placed as close as possible to this pin and be connected to ground.
33	Test	O	This pin if for test purposes and should be grounded for normal operation.
34	GND	-	Ground
36	VregDIG	-	Internally regulated voltage for LDO digital circuitry.

Connection Diagram



Pin(s)	Application Information
VccDIG VccVCO VccBUF VccPLL	Because the LMX2531 contains internal regulators, the power supply noise rejection is very good and capacitors at this pin are not critical. If desired, capacitors can be placed at these pins to improve the noise rejection. Recommended values are from open to 1 µF.
VregDIG	There is not really any reason to use any other values than the recommended values.
VrefVCO	If the VregVCO capacitor is changed, it is recommended to keep this capacitor between 1/100 and 1/1000 of the value of the VregVCO capacitor.
VregVCO	Because this pin is the output of a regulator, there are be stability concerns if there is not sufficient series resistance. For ceramic capacitors the ESR (Equivalent Series Resistance) is too low, and it recommended that a series resistance of 1 - 3.3Ω is necessary. If there is insufficient ESR, then there may be degradation in the phase noise, especially in the 100 - 300 kHz offset. Recommended values are from 1 µF to 10 µF.
VregPLL1 VregPLL2	The choice of the capacitor value at this pin involves a trade-off between integer spurs and phase noise in the 100 - 300 kHz offset range. If too much series resistance is at this pin, the spurs at far offset will be severely degraded. If there is too little, the phase noise may be degraded. A 470 nF capacitor in series with 220 mΩ provides optimal spurs with a minimal degradation in phase noise, although these optimal values may be design specific.
CLK DATA LE	Since the maximum voltage on these pins is less than the minimum Vcc voltage, level shifting may be required, if the output voltage of the microcontroller is too high. This can be accomplished with a resistive divider.
CE	As with the CLK, DATA, and LE pins, level shifting may be required if the output voltage of the microcontroller is too high. A resistive divider is or a series diode are two ways to accomplish this. The diode has the advantage that no current flows through it when the chip is powered down.
Ftest/LD	It is an option to use the lock detect information from this pin.
Fout	This is the high frequency output. This needs to be AC coupled, and matching may also be required. The value of the DC blocking capacitor may be changed, depending on the output frequency.
CPout Vtune	In most cases, it is sufficient to short these together. C1_LF, C2_LF, and R2_LF are used in conjunction with the internal loop filter to make a fourth order loop filter. However, the user always has the option of adding additional poles.
R2pLF	This is the fastlock resistor, which can be useful in many cases, since the spurs are often better with low charge pump currents, and the internal loop filter can be adjusted during fastlock.
OSCin	This is the crystal oscillator input pin. It needs to be AC coupled.
OSCin*	If the device is being driven single-ended, this pin needs to be shunted to ground with a capacitor.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Power Supply Voltage	V_{CC} (VccDIG, VccVCO, VccBUF, VccPLL)	-0.3 to 3.5	V
	All other pins (Except Ground)	-0.3 to 3.0	
Storage Temperature Range	T_{STG}	-65 to 150	˚C
Lead Temperature (solder 4 sec.)	T_L	+ 260	˚C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage (VccDig, VccVCO, VccBUF)	Vcc	2.8	3.0	3.2	V
Serial Interface and Power Control Voltage	V_i	0		2.75	V
Ambient Temperature (Note 3)	T_A	-40		+85	˚C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only to the test conditions listed.

Electrical Characteristics (V_{CC} = 3.0 V, -40˚C ≤ T_A ≤ 85 ˚C; except as specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		Current Consumption				
I_{CC}	Power Supply Current (All Parts Except LMX2531LQ2265E, LMX2531LQ2570E)	Divider Disabled		34	41	mA
		Divider Enabled		37	46	
	Power Supply Current (LMX2351LQ2265E, LMX2531LQ2570E)	Divider Disabled		38	44	
		Divider Enabled		41	49	
$I_{CC}PD$	Power Down Current	CE = 0 V, Part Initialized		7		µA
		Oscillator				
$I_{IH}OSC$	Oscillator Input High Current	V_{IH} = 2.75 V			100	µA
$I_{IL}OSC$	Oscillator Input Low Current	V_{IL} = 0	-100			µA
f_{OSCin}	Frequency Range		5		80	MHz
v_{OSCin}	Oscillator Sensitivity		0.5		2.0	Vpp
		PLL				
f_{COMP}	Phase Detector Frequency				20	MHz
I_{CPout}	Charge Pump Output Current Magnitude	ICP = 0		90		µA
		ICP = 1		180		µA
		ICP = 3		360		µA
		ICP = 15		1510		µA
$I_{CPout}TRI$	CP TRI-STATE Current	0.4 V < V_{CPout} < 2.0 V		2	10	nA
$I_{CPout}MM$	Charge Pump Sink vs. Source Mismatch	V_{CPout} = 1.2 V, T_A = 25˚C		2	8	%
$I_{CPout}V$	Charge Pump Current vs. CP Voltage Variation	0.4 V < V_{CPout} < 2.0 V, T_A = 25˚C		4		%
$I_{CPout}T$	CP Current vs. Temperature Variation	V_{CPout} = 1.2 V		8		%
LN(f)	Normalized Phase Noise Contribution (Note 2)	ICP = 1X Charge Pump Gain, 4 kHz Offset		-202		dBc/Hz
		ICP = 16X Charge Pump Gain, 4 kHz Offset		-212		

Electrical Characteristics (V_{CC} = 3.0 V, -40˚C ≤ T_A ≤ 85 ˚C; except as specified.) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VCO Frequencies							
f_{Fout}	Operating Frequency Range (All options have a frequency divider, this applies before the divider. The frequency after the divider is half of what is shown)	LMX2531LQ1570E		1530		1636	MHz
		LMX2531LQ1650E		1590		1700	
		LMX2531LQ1700E		1662		1770	
		LMX2531LQ1778E		1726		1840	
		LMX2531LQ1910E		1834		2028	
		LMX2531LQ2080E		1904		2274	
		LMX2531LQ2265E		2178		2400	
		LMX2531LQ2570E		2336		2790	
Other VCO Specifications							
ΔT_{CL}	Continuous Lock Temperature Range (Note 3)	LMX2531LQ1570E, LMX2531LQ1650E		90			˚C
		LMX2531LQ1700E, LMX2531LQ1778E, LMX2531LQ1910E, LMX2531LQ2080E, LMX2531LQ2265E,LMX2531LQ2570E		125			
p_{Fout}	Output Power to a 50Ω/5pF Load (Applies across entire tuning range.)	LMX2531LQ1570E	Divider Disabled	2.0	4.5	8.0	dBm
		LMX2531LQ1650E		2.0	4.5	8.0	
		LMX2531LQ1700E		1.0	3.5	7.0	
		LMX2531LQ1778E		1.0	3.5	7.0	
		LMX2531LQ1910E		1.0	3.5	7.0	
		LMX2531LQ2080E		1.0	3.5	7.0	
		LMX2531LQ2265E		1.0	3.5	7.0	
		LMX2531LQ2570E		0.0	3.0	6.0	
		LMX2531LQ1570E	Divider Enabled	1.0	2.5	6.0	dBm
		LMX2531LQ1650E		1.0	2.5	6.0	
		LMX2531LQ1700E		1.0	3.0	6.0	
		LMX2531LQ1778E		1.0	3.0	6.0	
		LMX2531LQ1910E		1.0	3.0	6.0	
		LMX2531LQ2080E		0.0	2.5	5.0	
		LMX2531LQ2265E		1.0	2.5	5.0	
		LMX2531LQ2570E		-1.0	1.5	4.0	
K_{Vtune}	Fine Tuning Sensitivity (When a range is displayed in the typical column, indicates the lower sensitivity is typical at the lower end of the tuning range, and the higher tuning sensitivity is typical at the higher end of the tuning range.)	LMX2531LQ1570E			4-7		MHz/V
		LMX2531LQ1650E			4-7		
		LMX2531LQ1700E			6-10		
		LMX2531LQ1778E			6-10		
		LMX2531LQ1910E			8-14		
		LMX2531LQ2080E			9-20		
		LMX2531LQ2265E			10-17		
		LMX2531LQ2570E			10-23		
HS_{Fout}	Harmonic Suppression (Applies Across Entire Tuning Range)	2nd Harmonic, 50Ω / 5pF Load	Divider Disabled		-30	-25	dBc
			Divider Enabled		-20	-15	
		3rd Harmonic, 50Ω / 5pF Load	Divider Disabled		-40	-35	
			Divider Enabled LMX2531LQ1570E LMX2531LQ1650E		-20	-15	
			Divider Enabled All Other Options		-25	-20	
$PUSH_{Fout}$	Frequency Pushing	Creg = 0.1uF, V_{DD} ± 100mV, Open Loop			300		kHz/V
$PULL_{Fout}$	Frequency Pulling	VSWR=2:1, Open Loop				±600	kHz
Z_{Fout}	Output Impedance				50		Ω

Electrical Characteristics (V_{CC} = 3.0 V, -40˚C ≤ T_A ≤ 85 ˚C; except as specified.) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VCO Frequencies							
VCO Phase Noise (Note 4)							
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1570E)	f_{Fout} = 1583 MHz DIV2 = 0	10 kHz Offset		-93		dBc/Hz
			100 kHz Offset		-118		
			1 MHz Offset		-140		
			5 MHz Offset		-154		
		f_{Fout} = 791.5 MHz DIV2 = 1	10 kHz Offset		-99		
			100 kHz Offset		-122		
			1 MHz Offset		-144		
			5 MHz Offset		-155		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1650E)	f_{Fout} = 1645 MHz DIV2 = 0	10 kHz Offset		-93		dBc/Hz
			100 kHz Offset		-118		
			1 MHz Offset		-140		
			5 MHz Offset		-154		
		f_{Fout} = 822.5 MHz DIV2 = 1	10 kHz Offset		-99		
			100 kHz Offset		-122		
			1 MHz Offset		-144		
			5 MHz Offset		-155		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1770E)	f_{Fout} = 1716 MHz DIV2 = 0	10 kHz Offset		-92		dBc/Hz
			100 kHz Offset		-117		
			1 MHz Offset		-139		
			5 MHz Offset		-153		
		f_{Fout} = 858 MHz DIV2 = 1	10 kHz Offset		-98		
			100 kHz Offset		-122		
			1 MHz Offset		-144		
			5 MHz Offset		-154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1778E)	f_{Fout} = 1783 MHz	10 kHz Offset		-92		dBc/Hz
			100 kHz Offset		-117		
			1 MHz Offset		-139		
			5 MHz Offset		-152		
		f_{Fout} = 891.5 MHz	10 kHz Offset		-97		
			100 kHz Offset		-122		
			1 MHz Offset		-144		
			5 MHz Offset		-154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ1910E)	f_{Fout} = 1931	10 kHz Offset		-89		dBc/Hz
			100 kHz Offset		-115		
			1 MHz Offset		-138		
			5 MHz Offset		-151		
		f_{Fout} = 965.5	10 kHz Offset		-95		
			100 kHz Offset		-121		
			1 MHz Offset		-143		
			5 MHz Offset		-155		

Electrical Characteristics (V_{CC} = 3.0 V, -40˚C ≤ T_A ≤ 85 ˚C; except as specified.) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VCO Frequencies							
$L(f)_{Fout}$	Phase Noise (LMX2531LQ2080E)	f_{Fout} = 2089 MHz	10 kHz Offset		-87		dBc/Hz
			100 kHz Offset		-113		
			1 MHz Offset		-136		
			5 MHz Offset		-150		
		f_{Fout} = 1044.5 MHz	10 kHz Offset		-93		
			100 kHz Offset		-119		
			1 MHz Offset		-142		
			5 MHz Offset		-154		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ2265E)	f_{Fout} = 2264 MHz	10 kHz Offset		-90		dBc/Hz
			100 kHz Offset		-114		
			1 MHz Offset		-137		
			5 MHz Offset		-151		
		f_{Fout} = 1132 MHz	10 kHz Offset		-95		
			100 kHz Offset		-118		
			1 MHz Offset		-142		
			5 MHz Offset		-152		
$L(f)_{Fout}$	Phase Noise (LMX2531LQ2570E)	f_{Fout} = 2563 MHz	10 kHz Offset		-86		dBc/Hz
			100 kHz Offset		-112		
			1 MHz Offset		-135		
			5 MHz Offset		-149		
		f_{Fout} = 1281.5 MHz	10 kHz Offset		-91		
			100 kHz Offset		-117		
			1 MHz Offset		-139		
			5 MHz Offset		-152		

Electrical Characteristics (V_{CC} = 3.0 V, -40˚C ≤ T_A ≤ 85 ˚C; except as specified.) (Continued)

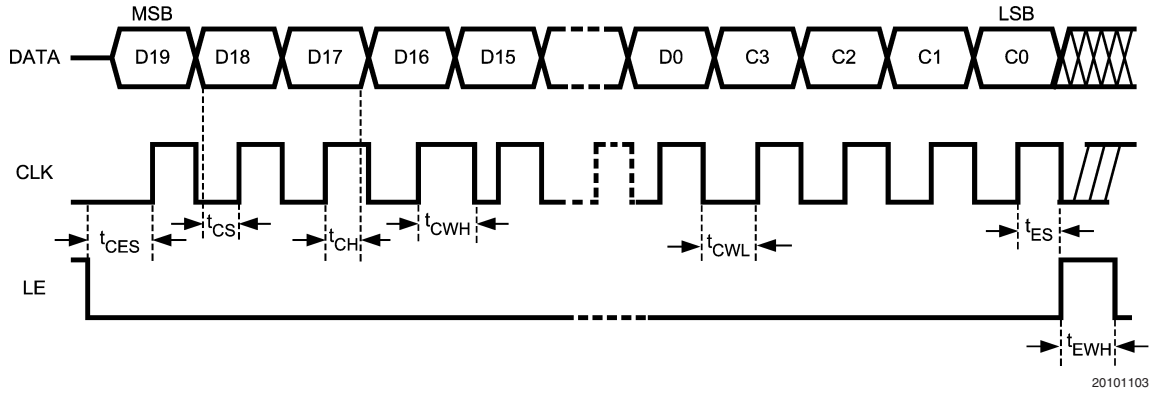
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital Interface (DATA, CLK, LE, CE, Ftest/LD, FLout)						
V_{IH}	High-Level Input Voltage		1.6		2.75	V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current	V_{IH} = 1.75	-3.0		3.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V	-3.0		3.0	µA
V_{OH}	High-Level Output Voltage	I_{OH} = 500 µA	2.0			V
V_{OL}	Low-Level Output Voltage	I_{OL} = -500 µA			0.4	V
MICROWIRE Timing						
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	25			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	20			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	25			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	25			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	25			ns
t_{CES}	Enable to Clock Set Up Time	See Data Input Timing	25			ns
t_{EWH}	Enable Pulse Width High	See Data Input Timing	25			ns

Note 2: Normalized Phase Noise Contribution is defined as: LN(f) = L(f) – 20log(N) – 10log(Fcomp) where L(f) is defined as the single side band phase noise measured at an offset frequency, f, in a 1 Hz Bandwidth and Fcomp is the comparison frequency of the synthesizer. The offset frequency, f, must be chosen sufficiently smaller then the PLL's loop band-width, and large enough to avoid a substantial noise contribution from the reference.

Note 3: Continuous Lock Temperature Range is how far the temperature can drift in either direction from it's original value at the time of the part being programmed, before the PLL has to be reprogrammed. The action of programming the R0 register activates a calibration routine. However, if this register is not reprogrammed, the temperature drift spec applies. Note that regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of -40˚C ≤T_A≤ 85˚C without violating specifications.

Note 4: The VCO phase noise is measured assuming that the loop bandwidth is sufficiently narrow that the VCO noise dominates. The maximum limits apply only at center frequecy and over temperature, assuming that the part is reloaded at each test frequency. Over frequency, the phase noise can vary 1-2 dB, with the worst case performance typically occurring at the highest frequency. Over temperature, the phase noise typically varies 1-2 dB, assuming the part is reloaded.

Serial Data Timing Diagram



1.0 Functional Description

The LMX2531 is a low power, high performance frequency synthesizer system which includes the PLL, VCO, and partially integrated loop filter. Section 2.0 on programming describes the bits mentioned in this section in more detail.

1.1 Reference Oscillator Input

Because the VCO frequency calibration algorithm is based on clocks from the OSCin pin, there are certain bits that need to be set depending on the OSCin frequency. XTLSEL (R6[22:20]) and XTLDIV (R7[9:8]) are both need to be set based on the OSCin frequency. For the LMX2531LQ2080E and the LMX2531LQ2570E, the XTLMAN[11:0] and XTLMAN2.

1.2 R Divider

The R divider divides the OSCin frequency down to the phase detector frequency. The only valid R counter values are 2, 4, 8, 16, and 32. The R divider also has an impact on the fractional modulus that can be used, if it is greater than 8.

1.3 N Divider

The N divider on the LMX2531 is fractional and can achieve any fractional denominator between 1 and 4,194,303 using a delta-sigma modulator of selectable order of 2, 3, or 4. Depending on the prescaler used, there are restrictions on how small the N counter can be.

1.4 Phase Detector

The phase detector compares the outputs of the R and N counters and puts out a correction current corresponding to the phase error. The choice of the phase detector freqeuncy does have an impact on performance.

1.5 Partially Integrated Loop Filter

The LMX2531 integrates the third pole (formed by R3 and C3) and fourth pole (formed by R4 and C4) of the loop filter. This loop filter can be enabled or bypassed using the EN_LPFLTR (R6[15]). The values for C3, C4, R3, and R4 can also be programmed independently through the MICROWIRE interface . Also, the values for R3 and R4 can be changed during FastLock, for minimum lock time. It is recommended that the integrated loop filter be set to the maximum possible attenuation (R3=R4=40kΩ, C3=C4=100pF), the internal loop filter is more effective at reducing certain spurs than the external loop filter. However, the attenuation of the internal loop filter is too high, it limits the maximum attainable loop bandwidth that can be achieved, which corresponds to the case where the shunt loop filter capacitor, C1, is zero. Increasing the charge pump current and/or the comparison frequency increases the maximum attainable loop bandwidth when desigining with the integrated filter. Furthermore, this often allows the loop filter to be better optimized and have stronger attenuation. If the charge pump current and comparison frequency are already as high as they go, and the maximum attainable loop bandwidth is still too low, the resistor and capacitor values can be decreased or the internal loop filter can even be bypassed. For design tools and more information on partially integrated loop filters, go to wireless.national.com.

1.6 Low Noise, Fully Integrated VCO

The LMX2531 includes a fully integrated VCO, including the inductors. In order for optimum phase noise performance, this VCO has frequency and phase noise calibration algorithms. The VCO internally divides up the frequency range into several bands, in order to achieve a lower tuning gain, and therefore better phase noise performance. The frequency calibration routine is activated any time that the R0 register is programmed. If the temperature shifts considerably and the R0 register is not programmed, then it can not drift more than continuous lock temperature range, ΔT_{CL}, or else the VCO is not guaranteed to stay in lock. There is also a routine for optimum phase noise performance as well, for each version of the LMX2531, the VCO_ACI_SEL bit (R6[19:16]) needs to be set to the correct value to ensure the best possible phase noise.

The gain of the VCO can change considerably over frequency. It is lowest at the minimum frequency and highest at the maximum frequency. This range is specified in the datasheet. When designing the loop filter, the following method is recommended. First, take the gemetric mean of the minimum and maximum frequencies that are to be used. Then use a linear approximation to extrapolate the VCO gain. An example is in order. Suppose the application requires the LMX2531LQ2080E PLL to tune from 2100 to 2150 MHz. The geometric mean of these freqeuncies is sqrt(2100 x 2150) MHz = 2125 MHz. The VCO gain is specified as 9 MHz/V at 1904 MHz and 20 MHz/V at 2274 MHz. Over this range of 370 MHz, the VCO gain changes 11 MHz/volt. So at 2125 MHz, the VCO gain would be approximately 9 + (2125-1904)* 11/370 = 15.6 MHz/V. Although the VCO gain can change from part to part, this variation is small to how much the VCO gain can change over frequency.

1.7 Programmable Divide by 2

All options of the LMX2531 offer a divide by 2 option. This allows the user to get exactly half of the VCO frequency. In order to use this feature, the VCO is programmed to it's non-divided frequency. Note that R0 register should be reprogrammed the first time after the DIV2 bit is enabled or disabled for optimal phase noise performance.

1.8 Choosing the Charge Pump Current and Comparison Frequency

The LMX2531 has 16 levels of charge pump currents and a highly flexible fractional modulus. This gives the user many degrees of freedom. This section discusses some of the design considerations. From the perspective of the PLL noise, choosing the charge pump current and comparison frequency as high as possible are best for optimal phase noise performance. The far out PLL noise improves 3 dB for every doubling of the comparison frequency, but at lower offsets, this effect is much less due to the PLL 1/f noise. Increasing the charge pump current inproves the phase noise about 3 dB per doubling of the charge pump current, although there are small diminishing returns as the charge pump current goes higher.

So, from a loop filter design perspective and from a PLL phase noise perspective, one might think to always design with the highest possible comparison frequency and charge pump current. However, if one considers the worst case fractional spurs that occur at an output frequency equal to 1 channel spacing away from a multiple of the OSCin frequency, then this gives reason to reconsider. If the comparison frequency or charge pump currents are too high, then these spurs could be degraded, and the loop filter may not be able to filter these spurs as well as theoretically predicted. For optimal spur performance, a comparison frequency in the ballpark of 2.5 MHz and a charge pump current of 1X are recommended.

2.0 General Programming Information

The LMX2531 is programmed using 14 24-bit registers used to control the LMX2531 operation. A 24-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field and an address field. The last 4 register bits, CTRL[3:0] form the address field, which is used to decode the internal register address. The remaining 20 bits form the data field DATA[19:0]. While LE is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When LE goes high, data is transferred from the data field into the selected register bank.

Although there are actually 14 registers in this part, only a portion of them should be programmed, since the state of the other hidden registers (R13, R11, and R10) are set during the initialization sequence. Although it is possible to program these hidden registers, as well as a lot of bits that are defined to either '1' or '0', the user should not experiment with these bits, since doing so may easily lead to degraded performance. The optimal settings for these bits have already been found, and not programming them would not be consistent with how the part is tested.

DATA[19:0]																				CONTROL[3:0]			
MSB																							**LSB**
D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	C3	C2	C1	C0

2.01 Register Location Truth Table

C3	C2	C1	C0	Data Address
1	1	0	0	R12
1	0	0	1	R9
1	0	0	0	R8
0	1	1	1	R7
0	1	1	0	R6
0	1	0	1	R5
0	1	0	0	R4
0	0	1	1	R3
0	0	1	0	R2
0	0	0	1	R1
0	0	0	0	R0

2.02 Initialization Sequence

The initial loading sequence from a cold start is described below. The registers must be program in order shown.

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R5 INIT1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R5 INIT2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R5	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	1
R12	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	0
R9	See individual section for R9 programming information.																				1	0	0	1
R8	See individual section for Register R8 programming information. Register R8 only needs to be programmed for a few options of the LMX2531 and and only in the case that the OSCin frequency is greater than 40 MHz.																				1	0	0	0
R7	See individual section for Register R7 programming information.																				0	1	1	1
R6	See individual section for Register R6 programming information.																				0	1	1	0
R4	See individual section for Register R4 programming information. Register R4 only needs to be program if FastLock is used.																				0	1	0	0
R3	See individual section for Register R3 programming information.																				0	0	1	1
R2	See individual section for Register R2 programming information.																				0	0	1	0
R1	See individual section for Register R1 programming information.																				0	0	0	1
R0	See individual section for Register R0 programming information.																				0	0	0	0

Note: There must be a minimum of 10 mS between the time when R5 is last loaded and when R1 is loaded to ensure time for the LDOs to power up properly.

2.03 Complete Register Content Map

2.0 General Programming Information (Continued)

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R0	N [7:0]								NUM [11:0]												0	0	0	0
R1	0	0	PRESC16	ICP [3:0]			N [10:8]				NUM [21:12]										0	0	0	1
R2	0	1	DEN [11:0]												R [5:0]						0	0	1	0
R3	DIV2	FDM	DITHER [1:0]		ORDER [1:0]		FoLD [3:0]				DEN [21:12]										0	0	1	1
R4	0	0	ICPFL [3:0]				TOC [13:0]														0	1	0	0
R5	1	0	0	0	0	REG_RST	0	0	0	0	0	0	0	EN_DIGLDO	EN_PLLLDO2	EN_PLLLDO1	EN_VCOLD	EN_OSC	EN_VCO	EN_PLL	0	1	0	1
R6	0	XTLSEL [2:0]			VCO_ACI_SEL [3:0]				EN_LPFLTR	R4_ADJ [1:0]		R4_ADJ_FL [1:0]		R3_ADJ [1:0]		R3_ADJ_FL [1:0]		C3_4_ADJ [2:0]			0	1	1	0
R7	0	0	XTLMAN [11:0]												XTLDIV [1:0]		0	0	0	0	0	1	1	1
R8	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	XTL MAN2	1	0	0	0
R9	0	0	0	0	0	0	LDDIV4	0	0	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1
R12	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	0

2.0 General Programming Information (Continued)

2.1 REGISTER R0

Note that the action of programming the R0 register activates a calibration routine for the VCO. This calibration is necessary to get the VCO to center the tuning voltage for optimal performance. If the temperature drifts considerably, then the PLL should stay in lock, provided that the temperature drift specification is not violated.

2.1.1 NUM[10:0] and NUM[21:12] -- Fractional Numerator

The NUM word is split between the R0 register and R1 register. The Numerator bits determine the fractional numerator for the delta sigma PLL. This value can go from 0 to 4095 when the FDM bit (R3[22]) is 0 (the other bits in this register are ignored), or 0 to 4194303 when the FDM bit is 1.

	NUM[21:12]										**NUM[11:0]**											
Fractional Numerator																						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...																						
409503	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
...																						
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note that there are restrictions on the fractional numerator value depending on the R counter value. These restrictions are related to the coarse tuning algorithm of the VCO. A numerator value of zero is the exception and is always allowed. If the R counter is ≤ 8, then there is no restriction on the fractional numerator. If R>8, the LSB of the fractional numerator must be 0. If R>16, the two LSB bits of the fractional numerator must be 0. If R>32, the three LSB bits of the fractional numerator must be 0. If this becomes an issue, recall that smaller fractions can be expressed as larger ones. For instance, 1/65 can be expressed as 8/520.

2.1.2 N[7:0] and N[10:8]

The N counter is 11 bits. 8 of these bits are located in the R0 register, and the remaining 3 (MSB bits) are located in the R1 register. The LMX2531 consists of an A, B, and C counter, which work in conjunction with the prescaler in order to form the final N counter value.

Operation with the 8/9/12/13 Prescaler											
	N[10:8]			**N[7:0]**							
N Value	C							B		A	
<31	Values less than 31 are prohibited.										
31	0	0	0	0	0	1	1	0	1	1	1
...											
1023	1	1	1	1	1	1	1	0	1	1	1

Operation with the 16/17/20/21 Prescaler											
	N[10:8]			**N[7:0]**							
N Value	C							B		A	
<55	Values less than 55 are prohibited.										
55	0	0	0	0	0	1	1	0	1	1	1
...											
2039	1	1	1	1	1	1	1	0	1	1	1

2.0 General Programming Information (Continued)

2.2 REGISTER R1

2.2.1 NUM[21:12]

These are the MSB bits in for the fractional numerator that already have been described.

2.2.2 N[10:8] -- 3 MSB Bits for the N Counter

These are the 2 MSB bits for the N counter, which were discussed in the R0 register section.

2.2.3 ICP[3:0] -- Charge Pump Gain

This bit programs the charge pump current when the charge pump gain. The current is programmable between 100uA and 1.6mA in 100uA steps. In general, higher charge pump currents yield better phase noise for the PLL, but also can cause higher spurs.

ICP	Charge Pump State	Typical Charge Pump Current at 3 Volts (µA)
0	1X	95
1	2X	180
2	3X	285
3	4X	380
4	5X	475
5	6X	970
6	7X	665
7	8X	760
8	9X	855
9	10X	950
10	11X	1045
11	12X	1140
12	13X	1235
13	14X	1330
14	15X	1425
15	16X	1520

2.2.4 PRESC16 -- PLL Prescaler

PRESC16	Prescaler	Minimum Continuous Divide Ratio	Maximum VCO Frequency (Before the Divider by 2)
0	8/9/12/13	31	1.2 GHz
1	16/17/20/21	55	3.0 GHz

2.0 General Programming Information (Continued)

2.3 REGISTER R2

2.3.1 R[5:0] -- R Counter Value

These bits determine the phase detector frequency. The OSCin frequency is divided by this R counter value. In single-ended mode, values of 1-63 are allowed. In differential mode, only 1,2,4,8,16, and 32 are allowed.

R Value	R[5:0]					
0-1,3,5-7,9-15 ,17-31,33-63	Illegal State					
2	0	0	0	0	1	0
4	0	0	0	1	0	0
8	0	0	1	0	0	0
16	0	1	0	0	0	0
32	1	0	0	0	0	0

2.3.2 DEN[21:12] and DEN[11:0]-- Fractional Denominator

These bits determine the fractional denominator. Note that the MSB bits for this word are in register R3. If the FDM bit is set to 0, DEN[21:12] are ignored.

	DEN[21:12]										DEN[11:0]											
Fractional Denominator																						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...																						
4095	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...																						
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.0 General Programming Information (Continued)

2.4 REGISTER R3

2.4.1 DEN[21:12] -- Extension for the Fractional Denominator

These are the MSB bits of the fractional denominator (DEN word), which have already been discussed.

2.4.2 FoLD[3:0] -- Multiplexed Output for Ftest/LD Pin

The FoLD[3:0] word is used to program the output of the FoLD Pin in accordance with the table below:

FoLD	Output Type	Function
0	High Impedance	Disabled
1	Push-Pull	Logical "High" State
2	Push-Pull	Logical "Low" State
3	Push-Pull	Digital Lock Detect
4	N/A	Reserved
5	Push-Pull	RF N Counter divided by 2
6	Open-Drain	Analog Lock Detect
7	Push-Pull	Analog Lock Detect
8	N/A	Reserved
9	N/A	Reserved
10	N/A	Reserved
11	N/A	Reserved
12	N/A	Reserved
13	N/A	Reserved
14	N/A	Reserved
15	N/A	Reserved

2.4.3 ORDER -- Order of Delta Sigma Modulator

This bit determines the order of the delta sigma modulator in the PLL. In general, higher order fractional modulators tend to reduce the primary fractional spurs that occur at increments of the channel spacing, but can also create spurs that are at a fraction of the channel spacing, if there is not sufficient filtering. The optimal choice of modulator order is very application specific, however, a third order modulator is a good starting point if not sure what to try first.

ORDER	Delta Sigma Modulator Order
0	Fourth
1	Reset Modulator (Integer Mode -- all fractions are ignored)
2	Second
3	Third

2.4.4 DITHER -- Dithering

Dithering is useful in reducing fractional spurs, especially those that occur a a fraction of the channel spacing. The only exception is when the fractional numerator is zero. In this case, dithering usually is not a benefit. Dithering also can sometimes increase the PLL phase noise by a fraction of a dB. In general, if dithering is disabled, phase noise may be slightly better inside the loop bandwidth of the system, but spurs are likely to be worse too.

DITHER	Dithering Mode
0	Weak Dithering
1	Reserved
2	Strong Dithering
3	Dithering Disabled

2.4.5 FDM -- Fractional Denominator Mode

When this bit is set to 1, the 10 MSB bits for the fractional numerator and denominator are considered. Otherwise they are ignored. When this bit is disabled, the current consumption is about 0.5 mA lower.

2.0 General Programming Information (Continued)

2.4.6 -- DIV2

When this bit is enabled on the appropriate option, the output of the VCO is divided by 2 on options that offer this feature. This has a small impact on harmonic content and output power.

DIV2	VCO Output Frequency
0	Not Divided by 2
1	Divided by 2

2.0 General Programming Information (Continued)

2.5 REGISTER R4

2.5.1 TOC[13:0] -- Time Out Counter for FastLock

When the value of this word is 3 or less, then FastLock is disabled, and this pin can only be used for general purpose I/O. When this value is 4 or greater, the time out counter is engaged for the amount of phase detector cycles shown in the table below.

TOC Value	FLout Pin State	Timeout Count
0	High Impedance	0
1	Low	Always Enabled
2	Low	0
3	High	0
4	Low	4 X 2 Phase Detector
.	.	.
16383	Low	16383 X 2 Phase Detector

When this count is active, the FLout Pin is grounded, the FastLock current is engaged, and the resistors R3 and R4 are also potentially changed. The table below summarizes the bits that control various values in and out of FastLock differences.

FastLock State	FLoutRF	Charge Pump Current	R3	R4
Steady State	High Impedance	ICP	R3_ADJ	R4_ADJ
Fastlock	Grounded	ICPFL	R3_ADJ_FL	R4_ADJ_FL

2.5.2 ICPFL[3:0] -- Charge Pump Current for Fastlock

When FastLock is enabled, this is the charge pump current that is used for faster lock time.

ICPFL	Fastlock Charge Pump State	Typical Fastlock Charge Pump Current at 3 Volts (µA)
0	1X	95
1	2X	190
2	3X	285
3	4X	380
4	5X	475
5	6X	570
6	7X	665
7	8X	760
8	9X	855
9	10X	950
10	11X	1045
11	12X	1140
12	13X	1235
13	14X	1330
14	15X	1425
15	16X	1520

2.0 General Programming Information (Continued)

2.6 REGISTER R5

2.6.1 EN_PLL -- Enable Bit for PLL

When this bit is set to 1, the PLL is powered up, otherwise, it is powered down.

2.6.2 EN_VCO -- Enable Bit for the VCO

When this bit is set to 1, the VCO is powered up, otherwise, it is powered down.

2.6.3 EN_OSC -- Enable Bit for the Oscillator Inverter

When this bit is set to 1 (default), the reference oscillator is powered up, otherwise it is powered down.

2.6.4 EN_VCOLDO -- Enable Bit for the VCO LDO

When this bit is set to 1 (default), the VCO LDO is powered up, otherwise it is powered down.

2.6.5 EN_PLLLDO1 -- Enable Bit for the PLLLDO 1

When this bit is set to 1 (default), the PLLLDO 1 is powered up, otherwise it is powered down.

2.6.6 EN_PLLLDO2 -- Enable Bit for the PLLLDO 2

When this bit is set to 1 (default), the PLLLDO 2 is powered up, otherwise it is powered down.

2.6.6 EN_PLLLDO2 -- Enable Bit for the PLLLDO 2

When this bit is set to 1 (default), the PLLLDO 2 is powered up, otherwise it is powered down.

2.6.7 EN_DIGLDO -- Enable Bit for the Digital LDO

When this bit is set to 1 (default), the Digital LDO is powered up, otherwise it is powered down.

2.6.8 REG_RST -- Resets all registers to default settings

This bit needs to be programmed three times to initialize the part. When this bit is set to one, all registers are set to default mode, and the part is powered down. The second time the R5 register is programmed with REG_RST=0, the register reset is released and the default states are still in the registers. However, since the default states for the blocks and LDOs is powered off, it is therefore necessary to program R5 a third time so that all the LDOs and blocks can be programmed to a power up state.When this bit is set to 1, all registers are set to the default modes, but part is powered down. For normal operation, this bit is set to 0. Note that once this initialization is done, it is not necessary to initialize the part any more.

2.0 General Programming Information (Continued)

2.7 REGISTER R6

2.7.1 C3_C4_ADJ[2:0] -- Value for C3 and C4 in the internal Loop Filter

C3_C4_ADJ	C3 (pF)	C4 (pF)
0	50	50
1	50	100
2	50	150
3	100	50
4	150	50
5	100	100
6	50	150
7	50	150

2.7.2 R3_ADJ_FL[1:0] -- Value for Internal Loop Filter Resistor R3 During Fastlock

R3_ADJ_FL Value	R3 Resistor During Fastlock (kΩ)
0	10
1	20
2	30
3	40

2.7.3 R3_ADJ[1:0] -- Value for Internal Loop Filter Resistor R3

R3_ADJ	R3 Value (kΩ)
0	10
1	20
2	30
3	40

2.7.4 R4_ADJ_FL[1:0] -- Value for Internal Loop Filter Resistor R4 During Fastlock

R4_ADJ_FL	R4 Value during Fast Lock (kΩ)
0	10
1	20
2	30
3	40

2.7.5 R4_ADJ[1:0] -- Value for Internal Loop Filter Resistor R4

R4_ADJ	R4 Value (kΩ)
0	10
1	20
2	30
3	40

2.7.6 EN_LPFLTR-- Enable for Partially Integrated Internal Loop Filter

The Enable Loop Filter bit is used to enable/disable the 3rd and 4th pole on-chip loop filters.

EN_LPFLTR	3rd and 4th Poles of Loop Filter
0	disabled (R3 = R4 = 0 ohms and C3 = C4 = 100 pF)
1	enabled

2.0 General Programming Information (Continued)

2.7.7 VCO_ACI_SEL

This bit is used to optimize the VCO phase noise. The recommended values are what are used for all testing purposes, and this bit should be set as the table below instructs.

Part	VCO_ACI_SEL
LMX2531LQ1570E LMX2531LQ1650E LMX2531LQ1700E LMX2531LQ1778E LMX2531LQ1910E LMX2531LQ2080E	8
LMX2531LQ2265E LMX2531LQ2570E	6

2.7.8 XTLSEL[2:0] -- Crystal Select

XTLSEL	Crystal Frequency
0	<20 MHz
1	30 - 50 MHz
2	50 - 70 MHz
3	>70 MHz
4	Manual Mode
5	Reserved
6	Reserved
7	Reserved

The value of this word needs to be changed based on the frequency presented to the OSCin pin in accordance to the table above.

2.8 Register R7

2.8.1 XTLDIV[1:0] -- Division Ratio for Higher Crystal Frequencies

The VCO frequency calibration algorithm is clocked from the OSCin pin frequency. However, this frequency needs to be divided down in accordance to the table below:

XTLDIV	Crystal Division Ratio	Crystal Range
0	Reserved	Reserved
1	Divide by 2	< 20 MHz
2	Divide by 4	20-40 MHz
3	Divide by 8	> 40 MHz

2.8.2 XTLMAN[11:0] -- Sets the calibration timing for lock time

With the exception of the parts listed in the table below, this bit should be set to zero for normal operation. For those parts in the table. For f_{OSCin} frequencies (expressed in MHz) not shown in the table, this bit value can be calculated as 16 X f_{OSCIN} / Kbit.

Part	Kbit	f_{OSCin}				
		10 MHz	20 MHz	30.72 Mhz	61.44 MHz	76.8 MHz
LMX2531LQ2080E	4.5	36	71	109	218	273
LMX2531LQ2570E	4.5	36	71	109	218	273

2.9 REGISTER R8

2.9.1 XTLMAN2 -- Calibration Select

In the case that manual mode for XTLSEL is selected and the OSCin frequency is greater than 40 MHz, this bit should be enabled, otherwise it should be 0.

2.0 General Programming Information (Continued)

2.10 REGISTERS R9 and R12

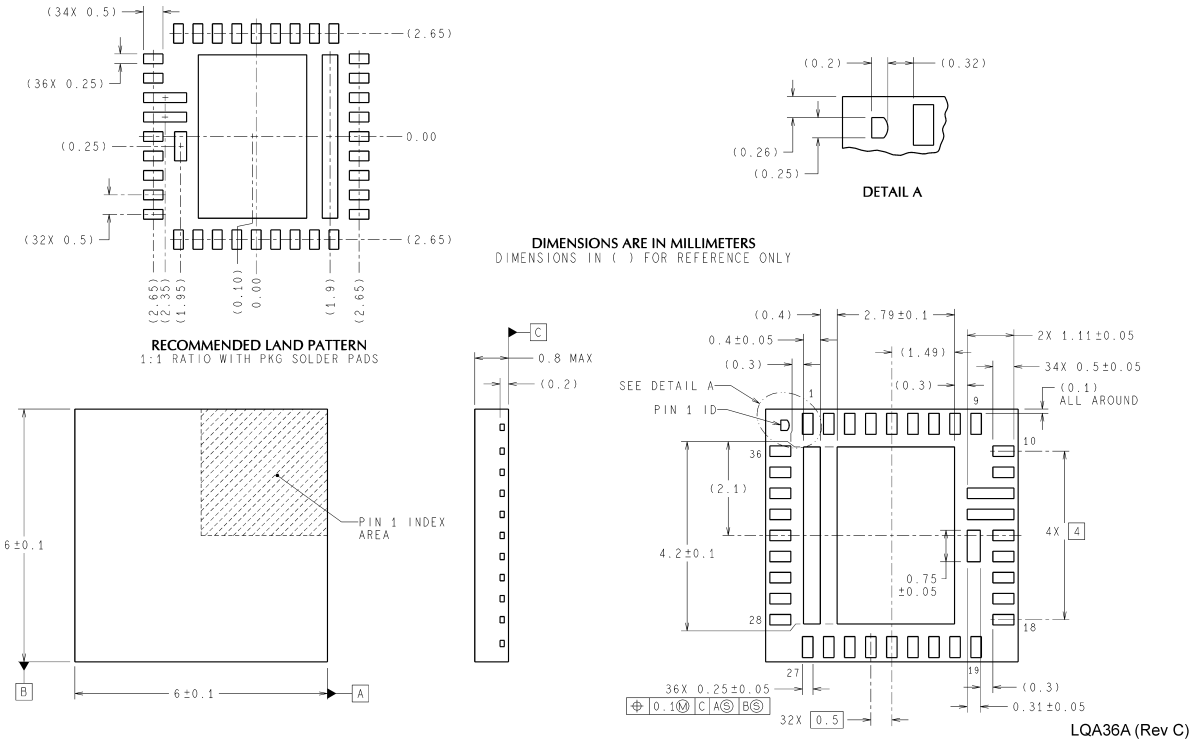
2.10.1 LDDIV4- RF Digital Lock Detect Divide By 4

Because the digital lock detect function is based on a phase error, it becomes more difficult to detect a locked condition for larger comparison frequencies. When this bit is enabled, it subdivides the RF PLL comparison frequency presented to the digital lock detect circuitry by 4. This enables this circuitry to work at higher comparison frequencies. It is recommended that this bit be enabled whenever the comparison frequency exceeds 20 MHz and RF digital lock detect is used. This does not apply to the IF comparison frequency.

2.11 REGISTER R12

This register does not have user selectable bits. This register should be loaded as shown in section 2.02 Complete Register Content Map.

Physical Dimensions inches (millimeters) unless otherwise noted



LQA36A (Rev C)

Leadless Leadframe Package (Bottom View)
Order Number LMX2531LQX for 2500 Unit Reel
Order Number LMX2531LQ for 250 Unit Reel
NS Package Number LQA036AA

Part	Marking
LMX2531LQ1570E	311570EB
LMX2531LQ1650E	311650EA
LMX2531LQ1700E	311778EB
LMX2531LQ1778E	311778EA

Part	Marking
LMX2531LQ1910E	311910EB
LMX2531LQ2080E	312080EB
LMX2531LQ2265E	312265ED
LMX2531LQ2570E	312570EC

Notes

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