



100mA Low Dropout Voltage Regulators

LP2950 / LP2951

FEATURES

- 5V, 3.3V, and 3.0V Versions at 100mA Output
- Very Low Quiescent Current
- Low Dropout Voltage
- Extremely Tight Load and Line Regulation
- Very Low Temperature Coefficient
- Current and Thermal Limiting
- Needs Only 1 μ F for Stability

LP2951 Versions Only

- Error Flag Warns of Output Dropout
- Logic-Controlled Electronic Shutdown
- Output Programmable from 1.24 to 29V

APPLICATIONS

- Battery Powered Systems
- Cordless Telephones
- Radio Control Systems
- Portable / Palm Top / Notebook Computers
- Portable Consumer Equipment
- Portable Instrumentation
- Avionics
- SMPS Post-Regulator
- Voltage Reference
- Automotive Electronics

PRODUCT DESCRIPTION

The Calogic LP2950 and LP2951 are low power voltage regulators. These devices are an excellent choice for use in battery-powered applications such as cordless telephones, radio control systems, and portable computers. The LP2950 and LP2951 features very low quiescent current and very low dropout voltage (Typ. 50mV at light load and 380mV at 100mA). This includes a tight initial tolerance of 0.5% typ., extremely good load and line regulation 0.05% typ. and very low output temperature coefficient, making the LP2950/LP2951 useful as a low-power voltage reference.

The error flag output feature is used as power-on reset for warning of a low output voltage, due to falling voltage input of batteries. Another feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. The LP2950 is offered in a 3-pin TO-92 package compatible with other 5V, 3.0V, 3.3V regulators. The LP2951 is also available in 8-pin plastic and SO-8.

The regulator output voltage may be pin-strapped for 5V, 3V or 3.3 volts or programmed from 1.24 volt to 29 volts with an external pair of resistors. Use of AS's design, processing and testing techniques make our LP2950 and LP2951 superior over similar products.

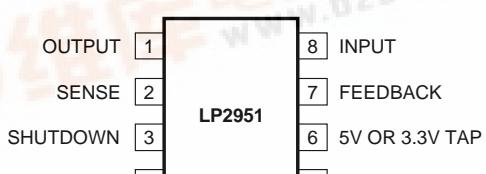
ORDERING INFORMATION

| PART | PACKAGE | TEMPERATURE RANGE |
|-------------|----------------------|-------------------|
| LP2950ACN-X | TO-92 (3-Pin) | IND. |
| LP2950CN-X | TO-92 (3-Pin) | IND. |
| LP2951ACP-X | Plastic DIP (8-Pin) | IND. |
| LP2951CP-X | Plastic DIP (8-Pin) | IND. |
| LP2951ACS-X | Plastic SOIC (8-Pin) | IND. |
| LP2951CS-X | Plastic SOIC (8-Pin) | IND. |

X = 3.0V, 3.3V or 5.0V

PIN CONNECTIONS

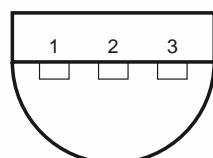
8-PIN SURFACE MOUNT



TOP VIEW

1D-19

TO-92



BOTTOM VIEW

1. OUTPUT
2. GROUND
3. INPUT

1D-20

LP2950/LP2951



ABSOLUTE MAXIMUM RATINGS

| | |
|--------------------------------------|--------------------|
| Power Dissipation | Internally Limited |
| Lead Temp. (Soldering, 5 Seconds) | 260°C |
| Storage Temperature Range | -65 to +150°C |
| Operating Junction Temperature Range | |
| LP2951 | -55 to +150°C |
| LP2950AC/LP2950C | |
| LP2951AC/LP2951C | -40 to +125°C |

| | |
|-------------------------|--------------|
| Input Supply Voltage | -0.3 to +30V |
| Feedback Input Voltage | -1.5 to +30V |
| Shutdown Input Voltage | -0.3 to +30V |
| Error Comparator Output | -0.3 to +30V |
| ESD Rating | 2KV Min |

ELECTRICAL CHARACTERISTICS: $V_S = 15V$, $T_A = 25^\circ C$, unless otherwise specified.

| PARAMETER | LP2951 | | | LP2950AC / LP2951AC | | | LP2950C / LP2951C | | | CONDITIONS (Note 2) | |
|--|----------------|-------------------|----------------|---------------------|-------------------|----------------|-------------------|-------------------|----------------|-------------------------|--|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| 3V VERSIONS | | | | | | | | | | | |
| Output Voltage | 2.985 2.964 | 3.0 3.036 | 3.015 2.970 | 2.985 2.964 | 3.0 3.036 | 3.015 2.955 | 2.970 2.940 | 3.0 3.045 | 3.030 3.060 | V V | $T_J = 25^\circ C$ $-25^\circ C \leq T_J \leq 85^\circ C$ Full Operating Temperature |
| Output Voltage | 2.955 | 3.0 | 3.045 | 2.958 | 3.0 | 3.042 | 2.928 | 3.0 | 3.072 | V | $100\mu A \leq I_L \leq 100mA$ $T_J \leq T_{JMAX}$ |
| 3.3V VERSIONS | | | | | | | | | | | |
| Output Voltage | 3.284 3.260 | 3.3 3.340 | 3.317 3.267 | 3.284 3.260 | 3.3 3.340 | 3.317 3.251 | 3.267 3.234 | 3.3 3.350 | 3.333 3.366 | V V | $T_J = 25^\circ C$ $-25^\circ C \leq T_J \leq 85^\circ C$ Full Operating Temperature |
| Output Voltage | 3.251 | 3.3 | 3.350 | 3.254 | 3.3 | 3.346 | 3.221 | 3.3 | 3.379 | V | $100\mu A \leq I_L \leq 100mA$ $T_J \leq T_{JMAX}$ |
| 5V VERSIONS | | | | | | | | | | | |
| Output Voltage | 4.975 4.94 | 5.0 5.06 | 5.025 4.95 | 4.975 4.94 | 5.0 5.0 | 5.025 5.050 | 4.95 4.925 | 5.0 5.0 | 5.05 5.075 | V V | $T_J = 25^\circ C$ $-25^\circ C \leq T_J \leq 85^\circ C$ Full Operating Temperature |
| Output Voltage | 4.925 | 5.0 | 5.075 | 4.93 | 5.0 | 5.07 | 4.88 | 5.0 | 5.12 | V | $100\mu A \leq I_L \leq 100mA$ $T_J \leq T_{JMAX}$ |
| ALL VOLTAGE OPTIONS | | | | | | | | | | | |
| Output Voltage Temperature Coefficient | | 20 | 120 | | 20 | | | 50 | | ppm/°C | (Note 1) |
| Line Regulation (Note 3) | | 0.03 | 0.1 | | 0.03 | 0.1 | | 0.04 | 0.2 | % | $6V \leq V_{IN} \leq 30V$ (Note 4) |
| Load Regulation (Note 3) | | 0.04 | 0.1 | | 0.04 | 0.1 | | 0.1 | 0.2 | % | $100\mu A \leq I_L \leq 100mA$ |
| Dropout Voltage (Note 5) | | 50 380 | 80 450 | | 50 380 | 80 450 | | 50 380 | 80 450 | mV mV | $I_L = 100\mu A$ $I_L = 100mA$ |
| Ground Current | | 150 8 | 170 12 | | 150 8 | 170 12 | | 150 8 | 170 12 | µA mA | $I_L = 100\mu A$ $I_L = 100mA$ |
| Current Limit | | 130 | 200 | | 130 | 200 | | 130 | 200 | mA | $V_{OUT} = 0$ |
| Thermal Regulation | | 0.05 | 0.2 | | 0.05 | 0.2 | | 0.05 | 0.2 | %/W | |
| Output Noise, 10Hz to 100KHz | | 430 160 100 | | | 430 160 100 | | | 430 160 100 | | µVrms µVrms µVrms | $C_L = 1\mu F$ $C_L = 200\mu F$ $C_L = 13.3\mu F$ (Bypass = $0.01\mu F$ pins 7 to 1 (LP2951)) |
| 8-PIN VERSIONS ONLY | | | | | | | | | | | |
| Reference Voltage | 1.22 | 1.235 | 1.25 | 1.22 | 1.235 | 1.25 | 1.21 | 1.235 | 1.26 | V | |
| Reference Voltage | 1.19 | | 1.27 | 1.19 | | 1.27 | 1.185 | | 1.285 | V | Over Temperature (Note 6) |
| Feedback Pin Bias Current | | 40 | 60 | | 40 | 60 | | 40 | 60 | nA | |
| Reference Voltage Temperature Coefficient | | 20 | | | 20 | | | 50 | | ppm/°C | (Note 7) |
| Feedback Pin Bias Current Temperature Coefficient | | 0.1 | | | 0.1 | | | 0.1 | | nA/°C | |

ELECTRICAL CHARACTERISTICS (continued)

| PARAMETER | LP2951 | | | LP2950AC / LP2951AC | | | LP2950C / LP2951C | | | UNITS | CONDITIONS (Note 2) |
|---|--------|-----------|-----------|---------------------|-----------|-----------|-------------------|-----------|-----------|-------|--|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| ERROR COMPARATOR | | | | | | | | | | | |
| Output Leakage Current | | 0.01 | 1 | | 0.01 | 1 | | 0.01 | 1 | µA | $V_{OH} = 30V$ |
| Output Low Voltage | | 150 | 250 | | 150 | 250 | | 150 | 250 | mV | $V_{IN} = 4.5V$, $I_{OL} = 400\mu A$ |
| Upper Threshold Voltage | 40 | 60 | | 40 | 60 | | 40 | 60 | | mV | (Note 7) |
| Lower Threshold Voltage | | 75 | 95 | | 75 | 95 | | 75 | 95 | mV | (Note 7) |
| Hysteresis | | 15 | | | 15 | | | 15 | | mV | (Note 7) |
| SHUTDOWN INPUT | | | | | | | | | | | |
| Input Logic Voltage | 2 | 1.3 | 0.6 | 2 | 1.3 | 0.7 | 2 | 1.3 | 0.7 | V | Low (Regulator ON) High (Regulator OFF) |
| Shutdown Pin Input Current | | 30 675 | 50 800 | | 30 675 | 50 800 | | 30 675 | 50 800 | µA | $V_S = 2.4V$ $V_S = 30V$ |
| Regulator Output Current in Shutdown | | 3 | 10 | | 3 | 10 | | 3 | 10 | µA | (Note 9) |

Note 1: Output or reference voltage temperature coefficients defined as the worst case voltage change divided by the total temperature range.

Note 2: Unless otherwise specified all limits guaranteed for $T_J = 25^\circ\text{C}$, $V_{IN} = 6\text{V}$, $I_{L}=100\mu\text{A}$ and $C_L = 1\mu\text{F}$. Additional conditions for the 8-pin versions are feedback tied to 5V tap and output tied to output Sense ($V_{OUT} = 5\text{V}$) and $V_{SHUTDOWN} \leq 0.8\text{V}$.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

Note 4: Line regulation for the LP2951 is tested at 150°C for $I_L = 1\text{ mA}$. For $I_L = 100\mu\text{A}$ and $T_J = 125^\circ\text{C}$, line regulation is guaranteed by design to 0.2%. See typical performance characteristics for line regulation versus temperature and load current.

Note 5: Dropout voltage is defined as the input to output differential at which the output voltage drops 100mV below its nominal value measured at 1V differential at very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken input account.

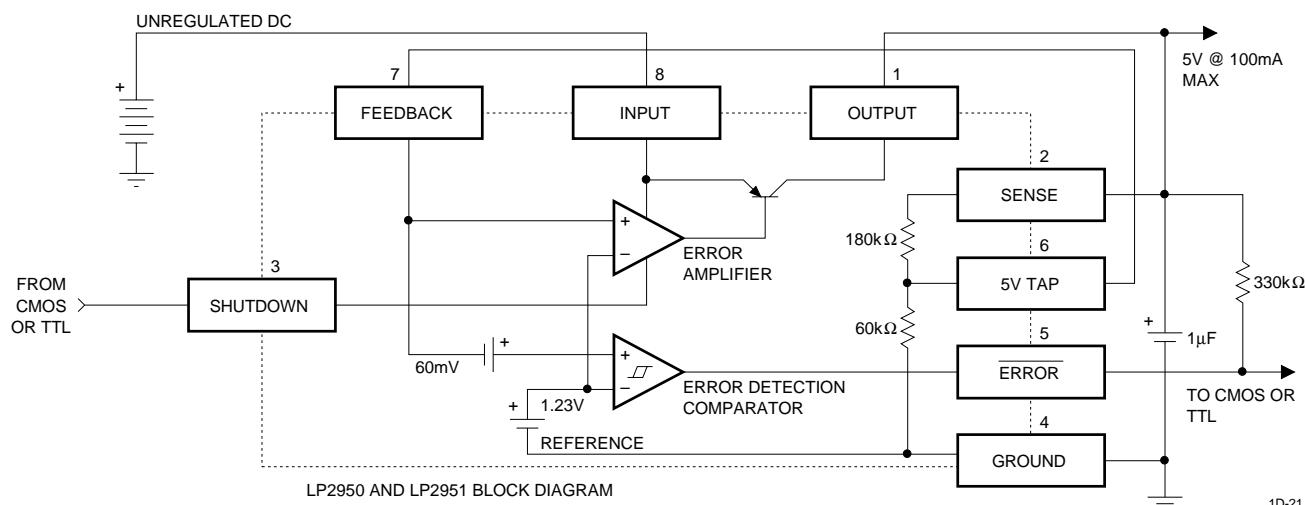
Note 6: $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1V)$, $2.3 \leq V_{IN} \leq 30V$, $100\mu A \leq I_L \leq 100mA$, $T_J \leq T_{JMAX}$.

Note 7: Comparator thresholds are expressed in terms of a voltage differential at the feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = $V_{OUT}/V_{REF} = (R1+R2)/R2$. For example, at a programmed output voltage of 5V, the error output is guaranteed to go low when the output drops by $95mV \times 5V/1.235 = 384mV$. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.

Note 8: $V_{SHUTDOWN} \geq 2V$, $V_{IN} \leq 30V$, $V_{OUT} = 0$, Feedback pin tied to 5V Tap.

Note 9: All typical values are not guaranteed.

BLOCK DIAGRAM



LP2950/LP2951



APPLICATION HINTS

EXTERNAL CAPACITORS

- The stability of the LP2950/LP2951 requires a $1.0\mu\text{F}$ or greater capacitor between output and ground. Oscillation could occur without this capacitor. Most types of tantalum or aluminum electrolytic are acceptable. For operations below -25°C a solid tantalum is recommended since the many aluminum types have electrolytes that freeze at about -30°C . The ESR of about 5Ω or less and resonant frequency about 500kHz are the most important parameters in the value of the capacitor. The capacitors value may be increased without limit.
- At lower values of output current, less output capacitance is required for stability. For currents below 10mA the value of the capacitor can be reduced to $0.33\mu\text{F}$ and $0.1\mu\text{F}$ for 1mA . More output capacitance is needed for the 8-pin version at voltages below 5V since it runs the error amplifier at lower gain.
- At worst case $3.3\mu\text{F}$ or greater must be used for the condition of 100mA load at 1.23V output.
- The LP2950, unlike other low dropout regulators will remain stable and in regulation with no load in addition to the internal voltage divider. This feature is especially important in applications like CMOS RAM keep-alive circuits. When setting the output voltage of the LP2951 version with external resistors, a minimum load of $1\mu\text{A}$ is recommended.
- If there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input then a $1\mu\text{A}$ tantalum or aluminum electrolytic capacitor should be placed from the input to the ground.
- Instability can occur if there is a stray capacitance to the LP2951 feedback terminal (pin 7). This could cause more problems when using a higher value of external resistors to set the output voltage. This problem can be eliminated by adding a 100pF capacitor between output and feedback and increasing the output capacitor to at least $3.3\mu\text{F}$.

ERROR DETECTION COMPARATOR OUTPUT

The Comparator produces a logic low output whenever the LP2951 output falls out of regulation by more than around 5%. This occurs at approximately 60mV offset divided by the 1.235 reference voltage. This trip level remains 5% below normal regardless of the programmed output voltage of the regulator. Figure 1 shows the timing diagram depicting the ERROR signal and the regulator output voltage as the LP2951 input is ramped up and down. The ERROR signal becomes low at around 1.3V input, and goes high around 5V input (input voltage at which $\text{V}_{\text{OUT}} = 4.75\text{V}$). Since the LP2951's dropout voltage is load dependent, the input voltage trip point (around 5V) will vary with the load current. The output voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. Depending on the system requirements the resistor may be returned to 5V output or other supply voltage. In determining the value of this resistor, note that the output is rated to sink $400\mu\text{A}$, this value adds to battery drain in a low battery condition. Suggested values range from $100\text{k}\Omega$ to $1\text{M}\Omega$. If the output is unused this resistor is not required.

PROGRAMMING THE OUTPUT VOLTAGE OF LP2951

The LP2951 may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5V Tap). Also, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in Figure 2, an external pair of resistors is required.

Refer to the equation below for the programming of the output voltage:

$$\text{V}_{\text{OUT}} = \text{V}_{\text{REF}} \times (1 + R_1/R_2) + I_{\text{FB}}R_1$$

The V_{REF} is 1.235 and I_{FB} is the feedback bias current, nominally -20nA . The minimum recommended load current of $1\mu\text{A}$ forces an upper limit of $1.2\text{M}\Omega$ on value of R_2 . If no load is presented the I_{FB} produces an error of typically 2% in V_{OUT} which may be eliminated at room temperature by trimming R_1 . To improve the accuracy choose the value of $R_2 = 100\text{k}\Omega$ this reduces the error by 0.17% and increases the resistor program current by $12\mu\text{A}$. Since the LP2951 typically draws $60\mu\text{A}$ at no load with Pin 2 open-circuited this is a small price to pay.

REDUCING OUTPUT NOISE

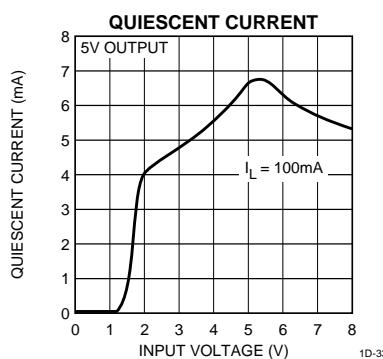
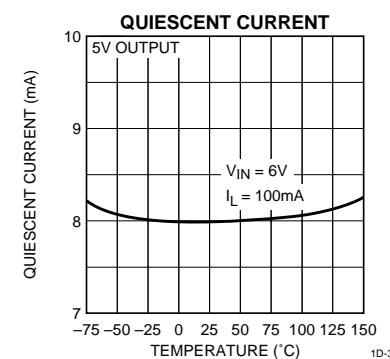
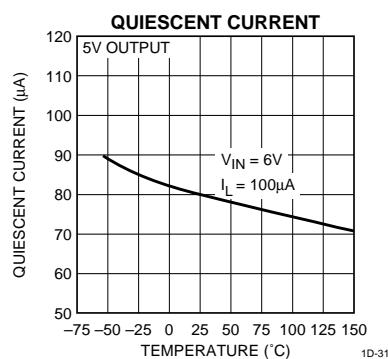
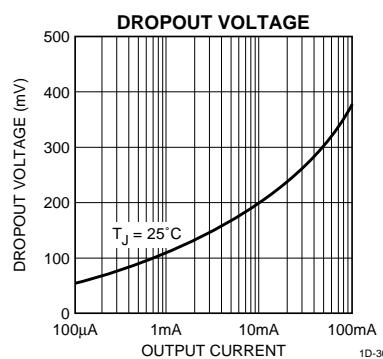
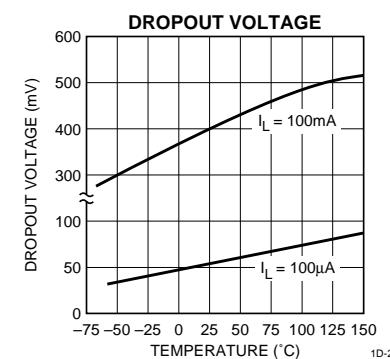
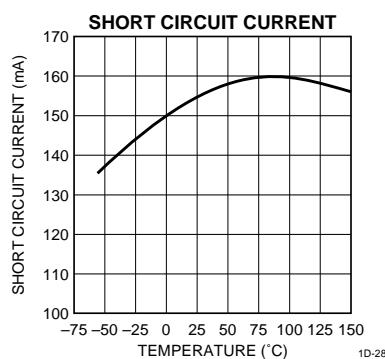
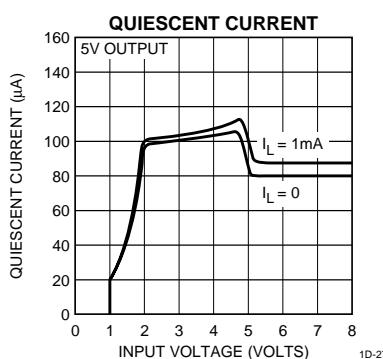
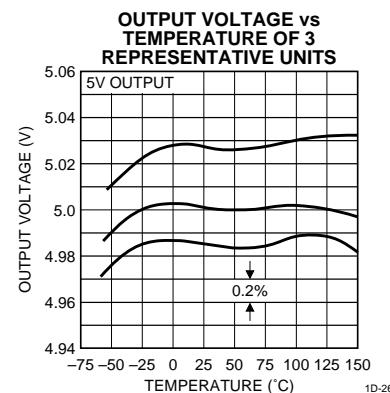
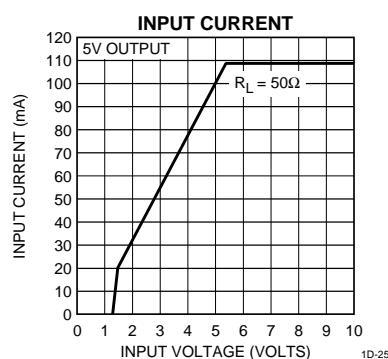
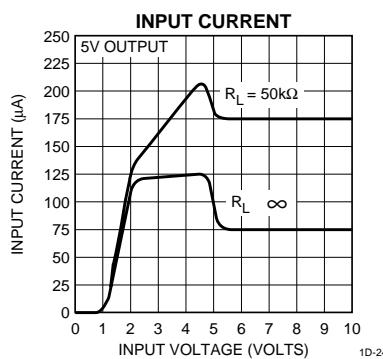
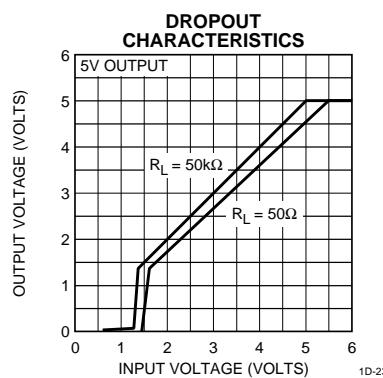
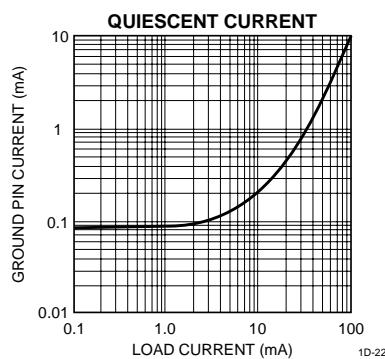
It may be an advantage to reduce the AC noise present at the output. One way is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way that noise can be reduced on the lead 3 of LP2950, but is relatively inefficient, as increasing the capacitor from $1\mu\text{F}$ to $220\mu\text{F}$ only decreases the noise from $430\mu\text{V}$ to $160\mu\text{Vrms}$ for a 100kHz bandwidth at 5V output.

Noise could also be reduced fourfold by a bypass capacitor across R_1 , since it reduces the high frequency gain from 4 to unity.

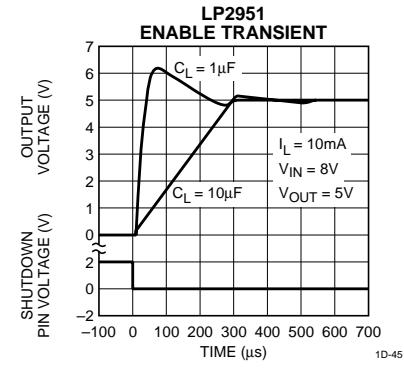
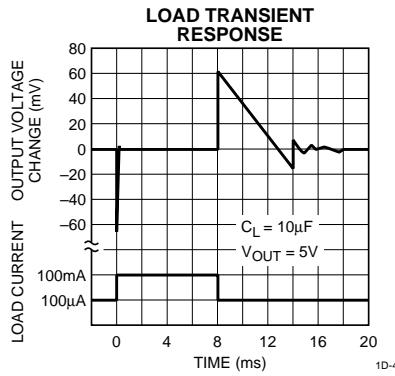
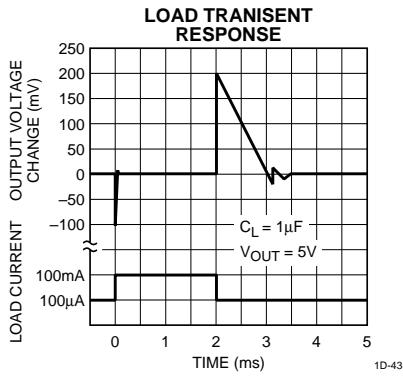
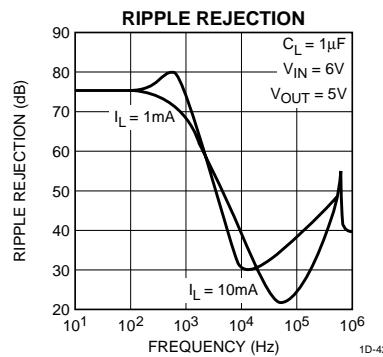
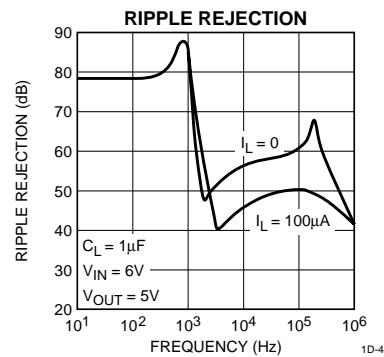
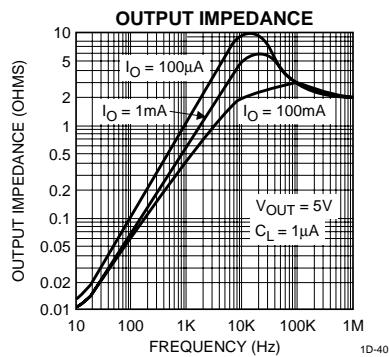
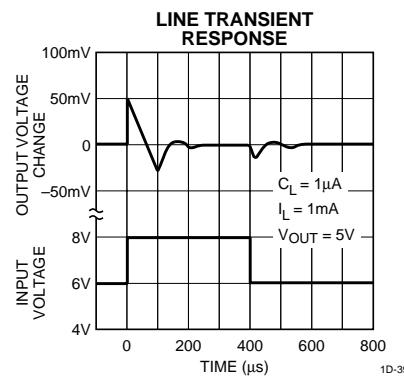
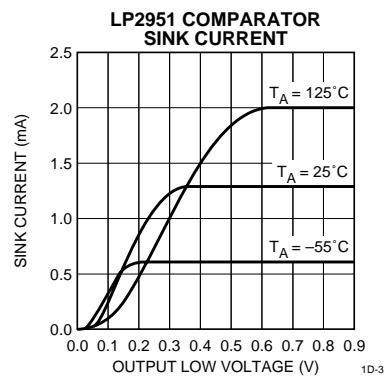
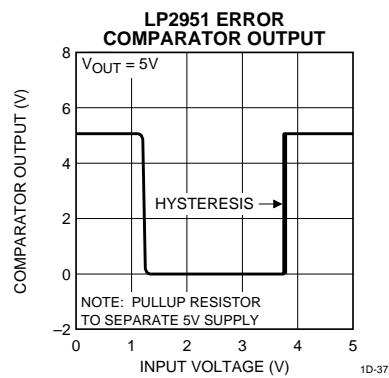
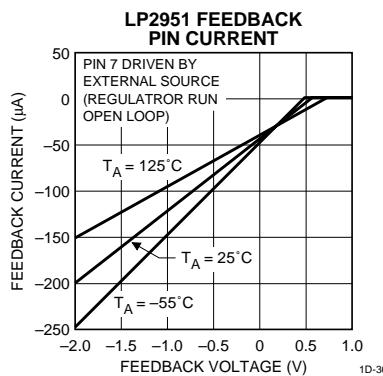
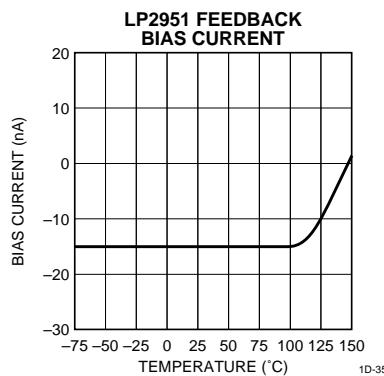
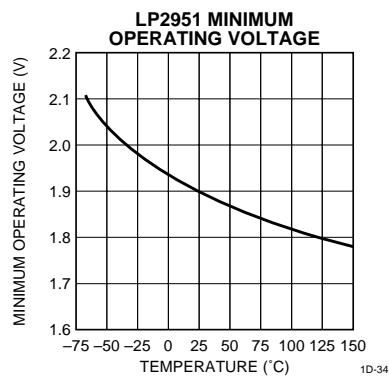
$$C_{\text{BYPASS}} \equiv 1/2\pi R_1 \times 200\text{Hz}$$

or choose $0.01\mu\text{F}$. When doing this, the output capacitor must be increased to $3.3\mu\text{F}$ to maintain stability. These changes reduce the output noise from $430\mu\text{V}$ to $100\mu\text{Vrms}$ for a 100kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher voltages.

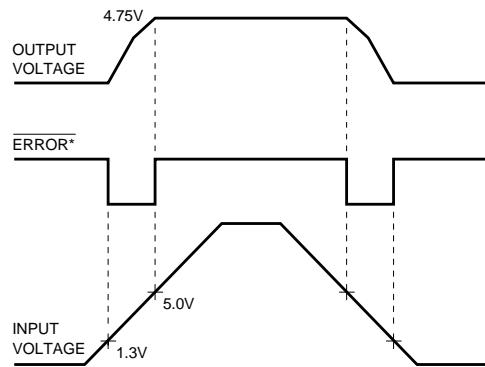
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

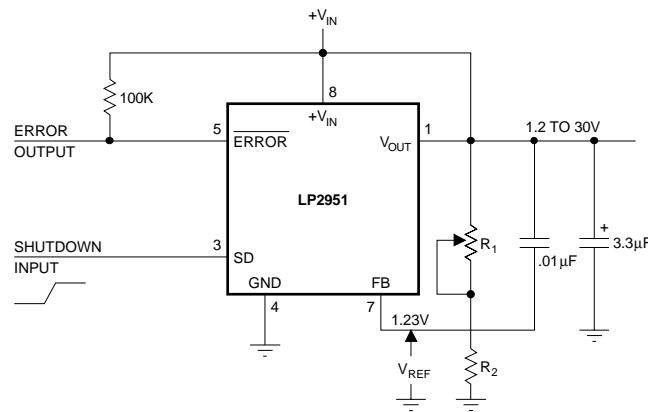


TYPICAL APPLICATIONS



*SEE APPLICATION INFO.

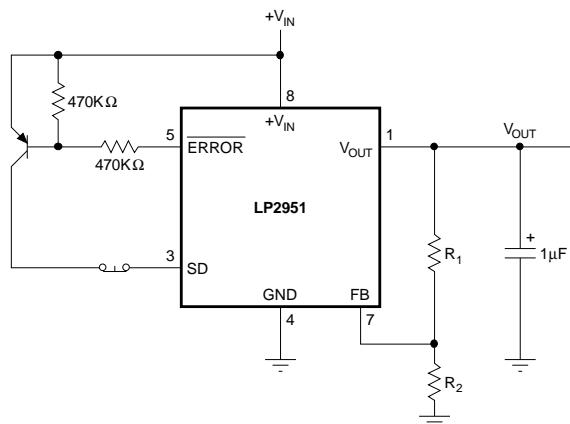
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1F-45

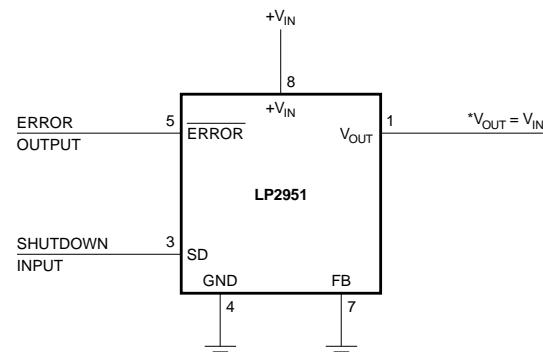
FIGURE 1. ERROR OUTPUT TIMING

FIGURE 2. ADJUSTABLE REGULATOR



LATCH OFF WHEN ERROR FLAG OCCURS

1F-46

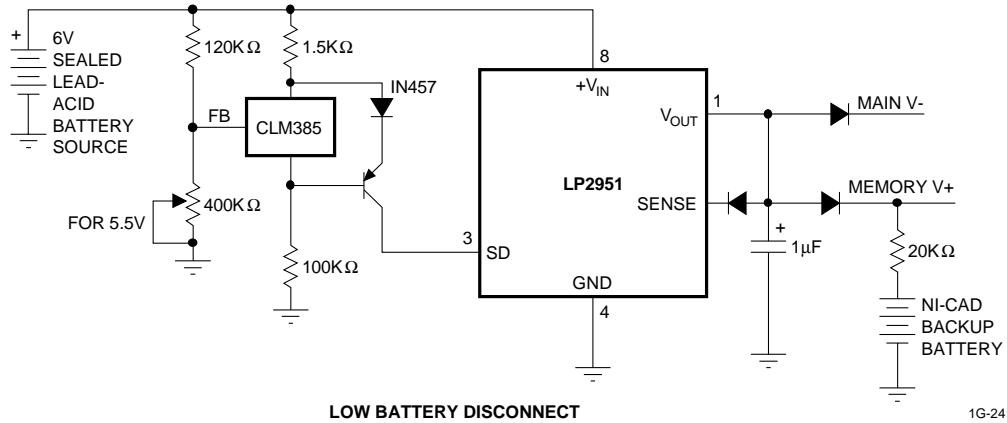


*MINIMUM INPUT - OUTPUT VOLTAGE RANGES FROM 4mV TO 400mV.
DEPENDING ON LOAD CURRENT. CURRENT LIMIT IS TYPICALLY 160mA.

WIDE INPUT VOLTAGE RANGE CURRENT LIMITER

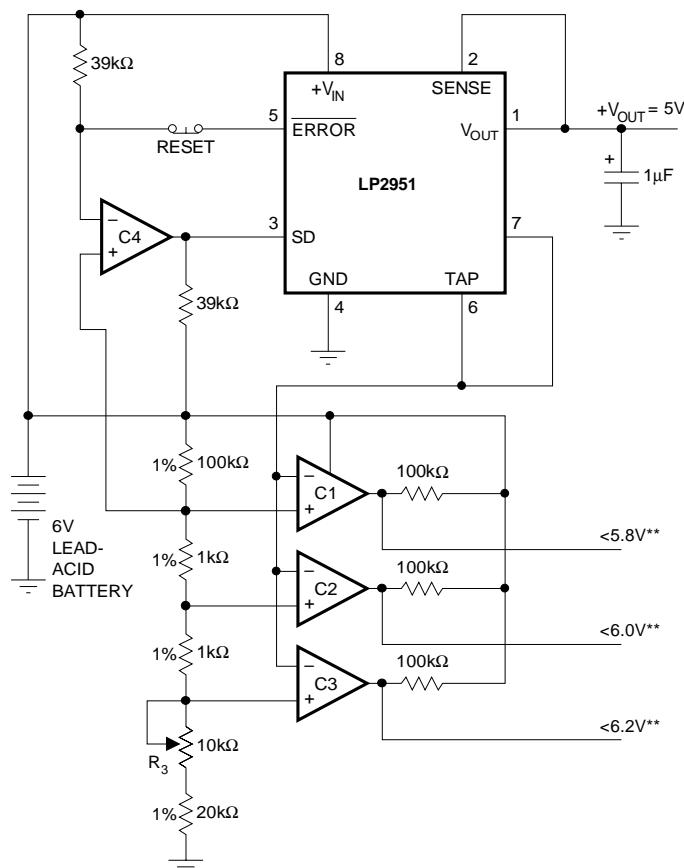
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TYPICAL APPLICATIONS (continued)



LOW BATTERY DISCONNECT

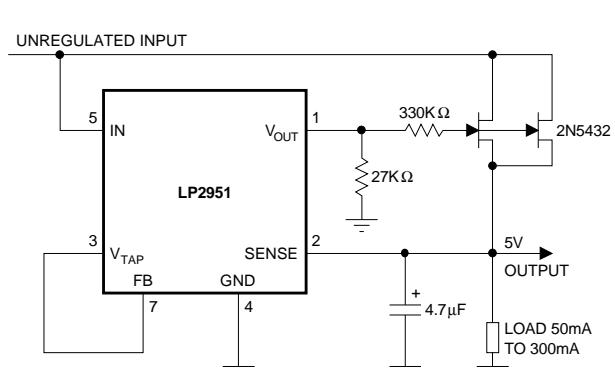
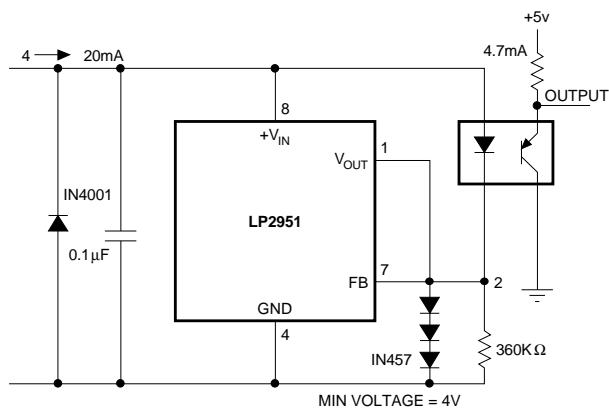
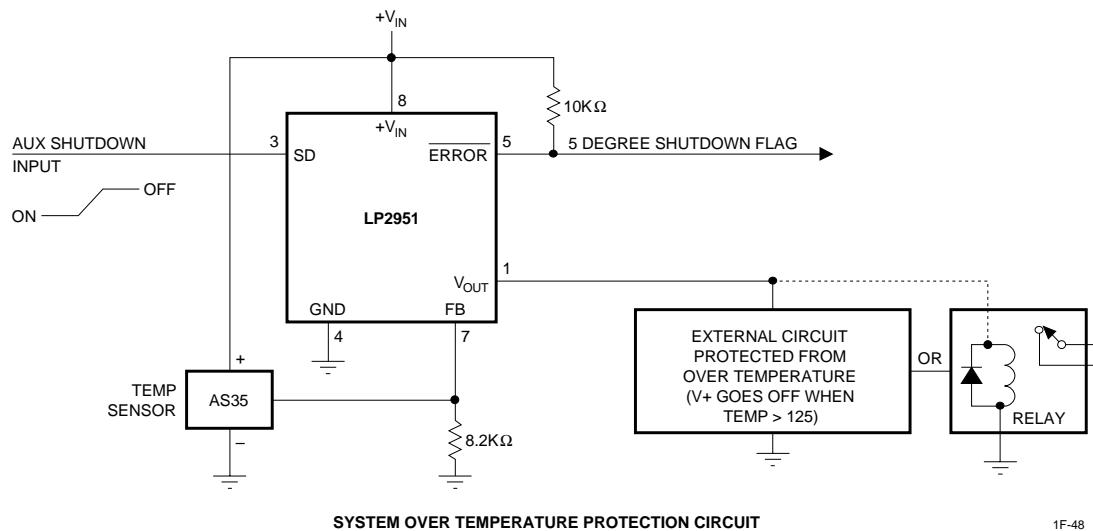
1G-24



*OPTIONAL LATCH OFF WHEN DROPOUT OCCURS. ADJUST R3 FOR C2 SWITCHING WHEN V_{IN} IS 6.0V.

**OUTPUTS GO LOW WHEN V_{IN} DROPS BELOW DESIGNATED THRESHOLDS.

TYPICAL APPLICATIONS (continued)



SCHEMATIC DIAGRAM

