

AMIC

LP62E16512-I Series

Preliminary

512K X 16 BIT LOW VOLTAGE CMOS SRAM

Document Title

512K X 16 BIT LOW VOLTAGE CMOS SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	April 26, 2002	Preliminary





LP62E16512-I Series

Preliminary

512K X 16 BIT LOW VOLTAGE CMOS SRAM

Features

- Operating voltage: 1.65V to 2.2V
- Access times: 70 ns (max.)
- Current:
Very low power version: Operating: 40mA (max.)
Standby: 10µA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 1.2V (min.)
- Available in 48-ball CSP (8×10mm) packages

General Description

The LP62E16512-I is a low operating current 8,388,608-bit static random access memory organized as 524,288 words by 16 bits and operates on low power voltage from 1.65V to 2.2V. It is built using AMIC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.

Data retention is guaranteed at a power supply voltage as low as 1.2V.

Product Family

Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I _{CCDR} , Typ.)	Standby (I _{SB1} , Typ.)	Operating (I _{CC2} , Typ.)	
LP62E16512	-40°C ~ +85°C	1.65V~2.2V	70ns	0.1µA	0.5µA	3mA	48 CSP

1. Typical values are measured at VCC = 1.8V, T_A = 25°C and not 100% tested.
2. Data retention current VCC = 1.2V.

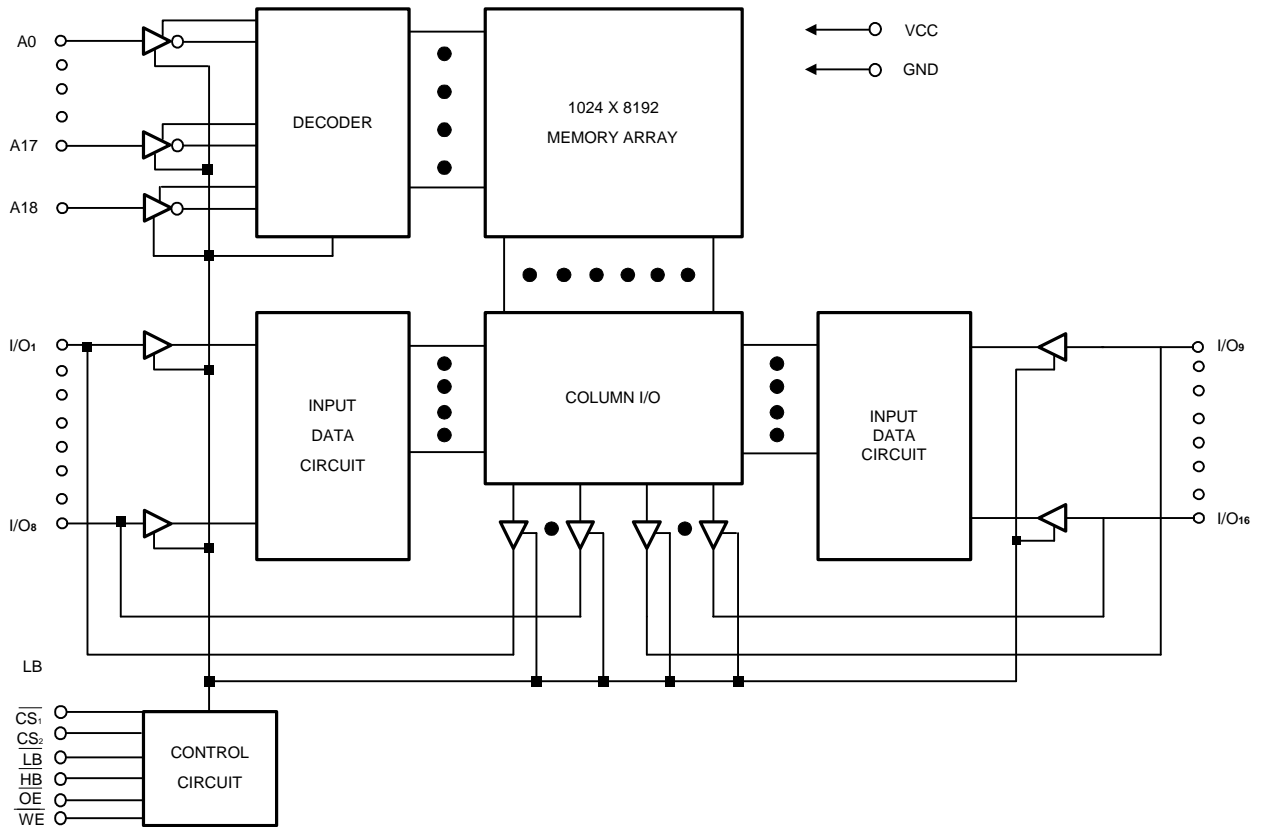
Pin Configurations

■ CSP (Chip Size Package) 48-pin Top View

	1	2	3	4	5	6
A	$\overline{\text{LB}}$	$\overline{\text{OE}}$	A0	A1	A2	CS ₂
B	I/O ₉	$\overline{\text{HB}}$	A3	A4	$\overline{\text{CS}}$ ₁	I/O ₁
C	I/O ₁₀	I/O ₁₁	A5	A6	I/O ₂	I/O ₃
D	GND	I/O ₁₂	A17	A7	I/O ₄	VCC
E	VCC	I/O ₁₃	NC	A16	I/O ₅	GND
F	I/O ₁₅	I/O ₁₄	A14	A15	I/O ₆	I/O ₇
G	I/O ₁₆	NC	A12	A13	$\overline{\text{WE}}$	I/O ₈
H	A18	A8	A9	A10	A11	NC



Block Diagram



**Pin Description - CSP**

Symbol	Description	Symbol	Description
A0 - A18	Address Inputs	$\overline{\text{HB}}$	Higher Byte Enable Input (I/O ₉ - I/O ₁₆)
$\overline{\text{CS}}_1$, CS ₂	Chip Enable	$\overline{\text{OE}}$	Output Enable
I/O ₁ - I/O ₁₆	Data Input/Output	VCC	Power Supply
$\overline{\text{WE}}$	Write Enable Input	GND	Ground
$\overline{\text{LB}}$	Byte Enable Input (I/O ₁ - I/O ₈)	NC	No Connection

Recommended DC Operating Conditions(T_A = -40°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	1.65	1.8	2.2	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	1.4	-	VCC + 0.3	V
V _{IL}	Input Low Voltage	-0.3	-	+0.4	V
C _L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-



Absolute Maximum Ratings*

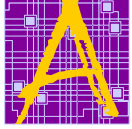
VCC to GND-0.5V to +3.0V
 IN, IN/OUT Volt to GND -0.5V to VCC + 0.5V
 Operating Temperature, Topr-40°C to +85°C
 Storage Temperature, Tstg.....-55°C to +125°C
 Power Dissipation, P_T.....0.7W

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = -40°C to + 85°C, VCC = 1.65V to 2.2V, GND = 0V)

Symbol	Parameter	LP62E16512-70LLI		Unit	Conditions
		Min.	Max.		
I _{LI}	Input Leakage Current	-	1	μA	V _{IN} = GND to VCC
I _{LO}	Output Leakage Current	-	1	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{LB} = \overline{HB} = V_{IH}$ V _{IO} = GND to VCC
I _{CC}	Active Power Supply Current	-	5	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $\overline{LB} = V_{IL}$ or $\overline{HB} = V_{IL}$, I _{IO} = 0mA
I _{CC1}	Dynamic Operating Current	-	40	mA	Min. Cycle, Duty = 100%, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $\overline{LB} = V_{IL}$ or $\overline{HB} = V_{IL}$ I _{IO} = 0mA
I _{CC2}		-	5	mA	$\overline{CS1} \leq 0.2V$, $CS2 \geq VCC-0.2V$, $\overline{LB} \leq 0.2V$ or $\overline{HB} \leq 0.2V$ f = 1MHz, I _{IO} = 0mA
I _{SB}	Standby Current	-	1	mA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{LB} = \overline{HB} = V_{IH}$
I _{SB1}		-	10	μA	$\overline{CS1} \geq VCC - 0.2V$ or $CS2 \leq 0.2V$ or $\overline{LB} = \overline{HB} \geq VCC-0.2V$ V _{IN} ≥ VCC-0.2V or V _{IN} ≤ 0.2V
V _{OL}	Output Low Voltage	-	0.2	V	I _{OL} = 0.1 mA
V _{OH}	Output High Voltage	1.4	-	V	I _{OH} = -1.0 mA



Truth Table

\overline{CS}_1	CS_2	\overline{OE}	\overline{WE}	\overline{LB}	\overline{HB}	I/O ₁ to I/O ₈ Mode	I/O ₉ to I/O ₁₆ Mode	VCC Current
H	X	X	X	X	X	High - Z	High - Z	I _{SB1} , I _{SB}
X	L	X	X	X	X	High - Z	High - Z	I _{SB1} , I _{SB}
X	X	X	X	H	H	High - Z	High - Z	I _{SB1} , I _{SB}
L	H	L	H	L	L	Read	Read	I _{CC1} , I _{CC2} , I _{CC}
				L	H	Read	High - Z	I _{CC1} , I _{CC2} , I _{CC}
				H	L	High - Z	Read	I _{CC1} , I _{CC2} , I _{CC}
L	H	X	L	L	L	Write	Write	I _{CC1} , I _{CC2} , I _{CC}
				L	H	Write	High - Z	I _{CC1} , I _{CC2} , I _{CC}
				H	L	High - Z	Write	I _{CC1} , I _{CC2} , I _{CC}
L	H	H	H	L	X	High - Z	High - Z	I _{CC1} , I _{CC2} , I _{CC}
L	H	H	H	X	L	High - Z	High - Z	I _{CC1} , I _{CC2} , I _{CC}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C _{IN} *	Input Capacitance		6	pF	V _{IN} = 0V
C _{I/O} *	Input/Output Capacitance		8	pF	V _{I/O} = 0V

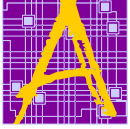
* These parameters are sampled and not 100% tested.



AC Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 1.65\text{V}$ to 2.2V)

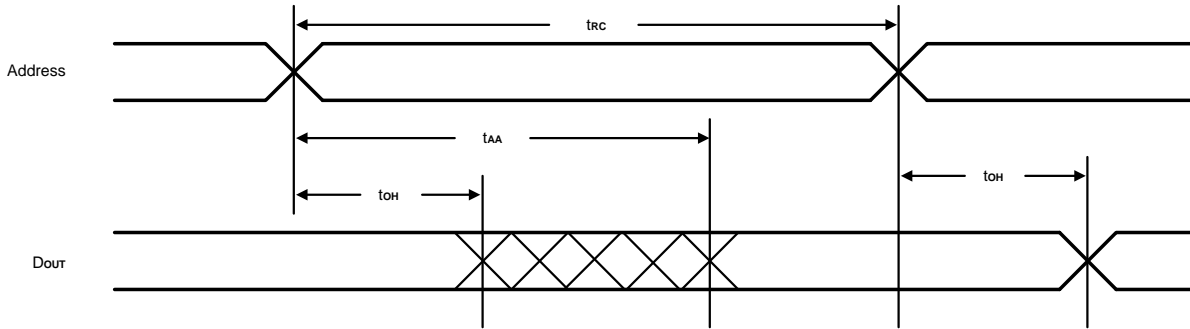
Symbol	Parameter	LP62E16512-70LLI		Unit
		Min.	Max.	
Read Cycle				
t _{RC}	Read Cycle Time	70	-	ns
t _{AA}	Address Access Time	-	70	ns
t _{Acs1} , t _{Acs2}	Chip Enable Access Time	-	70	ns
t _{BE}	Byte Enable Access Time	-	70	ns
t _{OE}	Output Enable to Output Valid	-	35	ns
t _{CLZ1} , t _{CLZ2}	Chip Enable to Output in Low Z	10	-	ns
t _{BLZ}	Byte Enable to Output in Low Z	10	-	ns
t _{OLZ}	Output Enable to Output in Low Z	5	-	ns
t _{CHZ1} , t _{CHZ2}	Chip Disable to Output in High Z	-	25	ns
t _{BHZ}	Byte Disable to Output in High Z	-	25	ns
t _{OHZ}	Output Disable to Output in High Z	-	25	ns
t _{OH}	Output Hold from Address Change	5	-	ns
Write Cycle				
t _{WC}	Write Cycle Time	70	-	ns
t _{cw1} , t _{cw2}	Chip Enable to End of Write	60	-	ns
t _{BW}	Byte Enable to End of Write	60	-	ns
t _{AS}	Address Setup Time	0	-	ns
t _{AW}	Address Valid to End of Write	60	-	ns
t _{WP}	Write Pulse Width	50	-	ns
t _{WR}	Write Recovery Time	0	-	ns
t _{WHZ}	Write to Output in High Z	-	25	ns
t _{DW}	Data to Write Time Overlap	30	-	ns
t _{DH}	Data Hold from Write Time	0	-	ns
t _{OW}	Output Active from End of Write	5	-	ns

Note: t_{CLZ1}, t_{CLZ2}, t_{BLZ}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

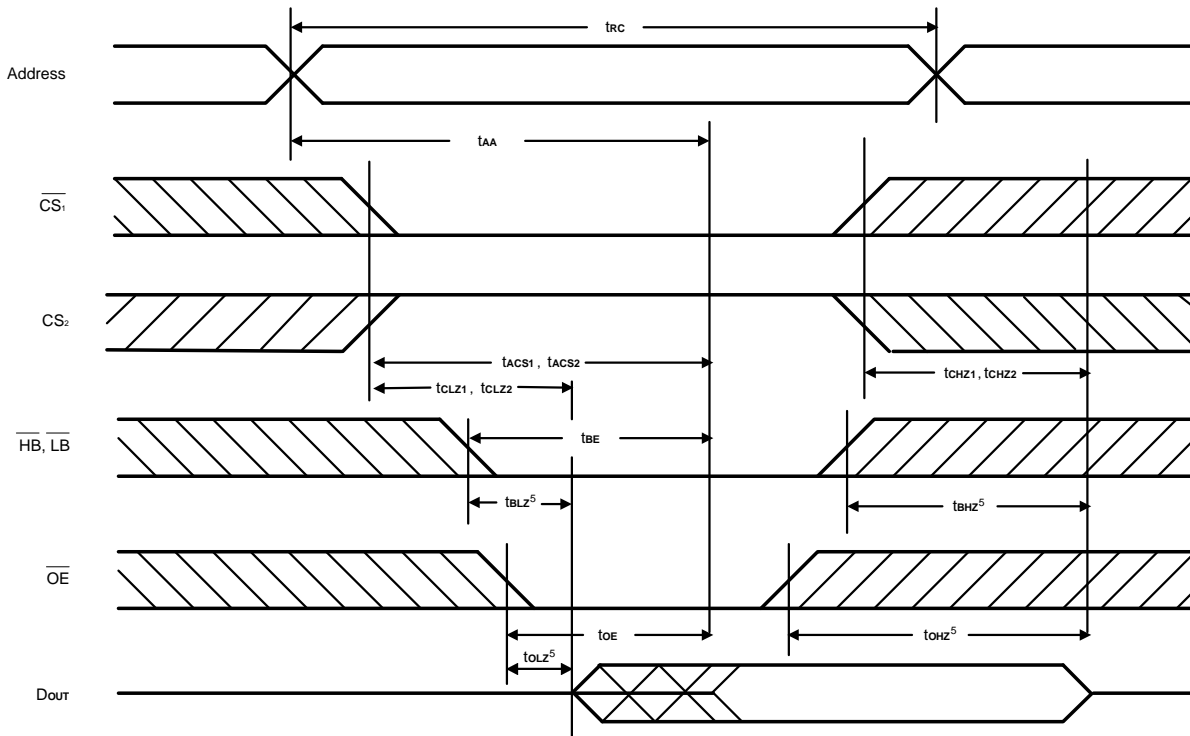


Timing Waveforms

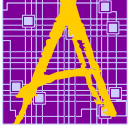
Read Cycle 1^(1, 2, 4)



Read Cycle 2^(1, 2, 3)

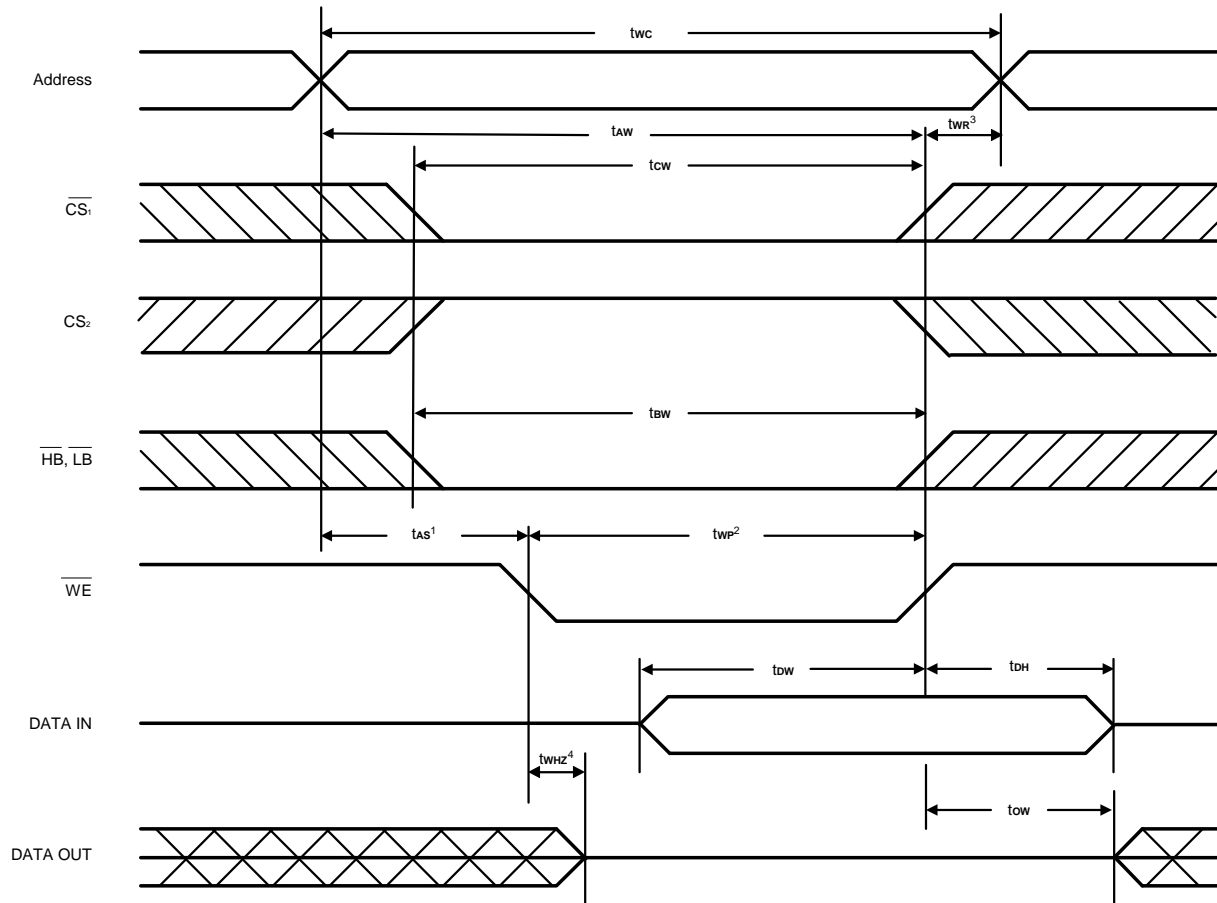


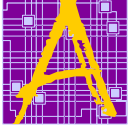
- Notes:
- \overline{WE} is high for Read Cycle.
 - Device is continuously enabled $\overline{CS1} = V_{IL}$, or $CS2 = V_{IH}$, $\overline{HB} = V_{IL}$ and, or $\overline{LB} = V_{IL}$.
 - Address valid prior to or coincident with $\overline{CS1}$ and (\overline{HB} and, or \overline{LB}) transition low or $CS2$ transition High.
 - $\overline{OE} = V_{IL}$.
 - Transition is measured $\pm 200mV$ from steady state. This parameter is sampled and not 100% tested.



Timing Waveforms (continued)

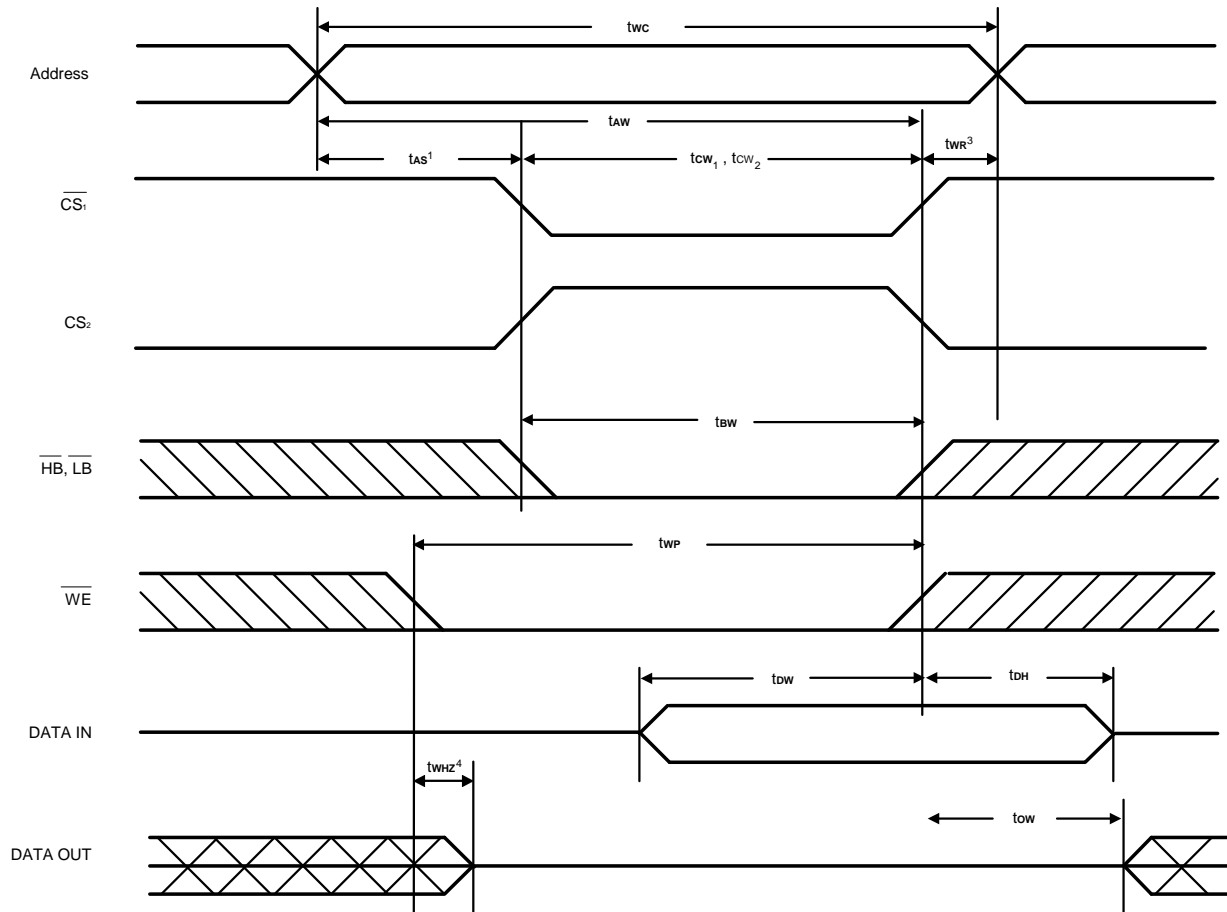
Write Cycle 1
(Write Enable Controlled)

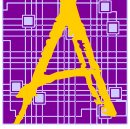




Timing Waveforms (continued)

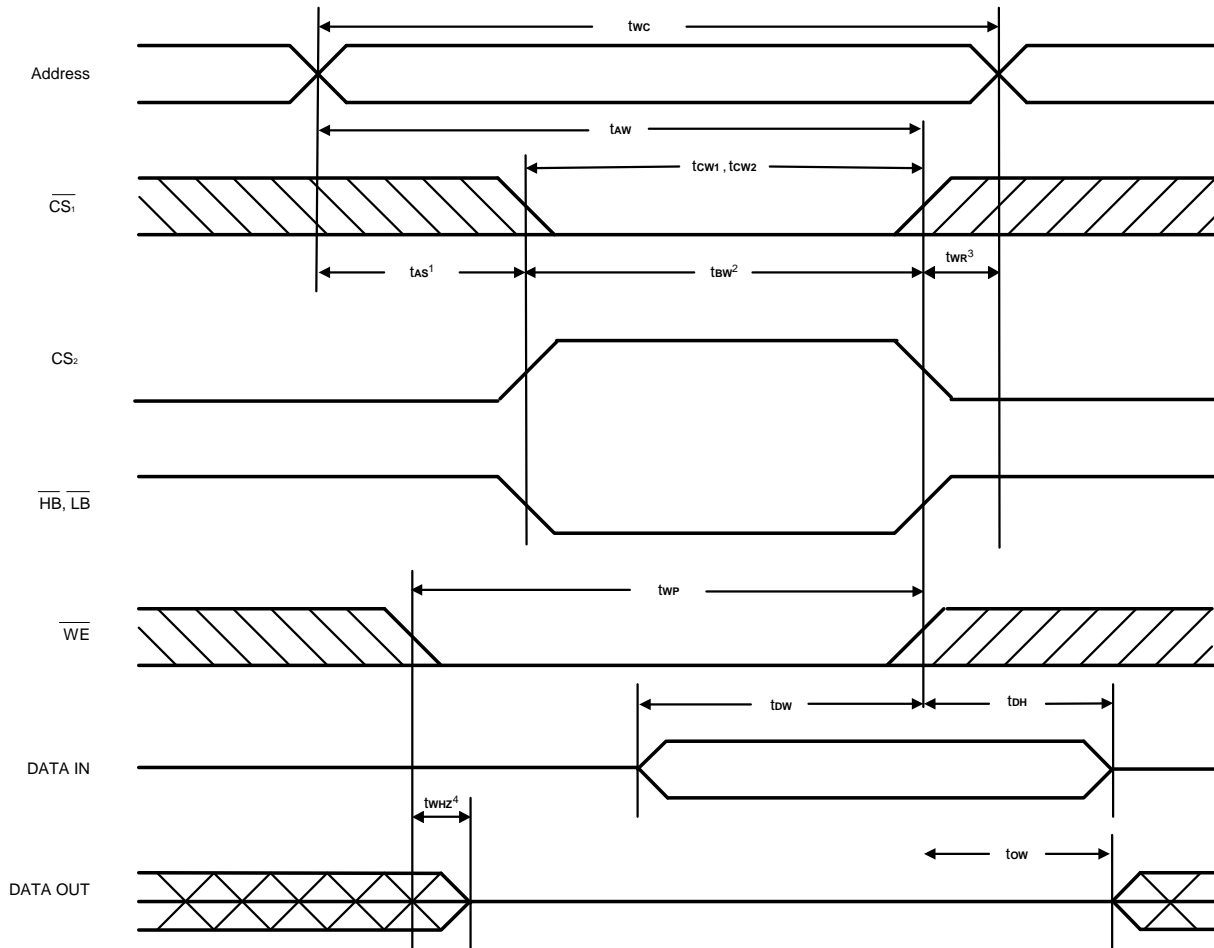
Write Cycle 2
(Chip Enable Controlled)





Timing Waveforms (continued)

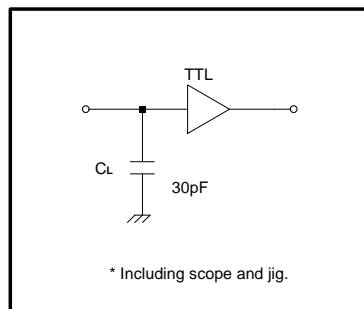
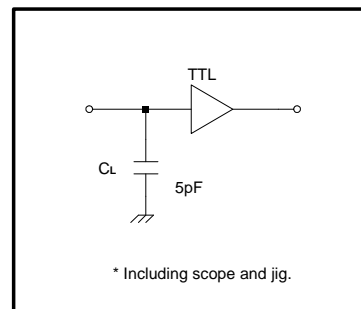
Write Cycle 3
(Byte Enable Controlled)



- Notes:
1. t_{as} is measured from the address valid to the beginning of Write.
 2. A Write occurs during the overlap (t_{wp} , t_{bw}) of a low $\overline{CS1}$, \overline{WE} and (\overline{HB} and , or \overline{LB}) or a high $CS2$.
 3. t_{wr} is measured from the earliest of $\overline{CS1}$ or \overline{WE} or (\overline{HB} and , or \overline{LB}) going high or $CS2$ going Low to the end of the Write cycle.
 4. \overline{OE} level is high or low.
 5. Transition is measured $\pm 200\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

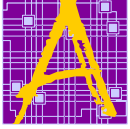
Input Pulse Levels	0.2V to VCC-0.2V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	0.8V
Output Load	See Figures 1 and 2


Figure 1. Output Load

Figure 2. Output Load for t_{CLZ1} , t_{CLZ2} , t_{BHZ} , t_{BLZ} , t_{OLZ} , t_{CHZ1} , t_{CHZ2} , t_{OHZ} , t_{WHZ} , and t_{OW}
Data Retention Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C)

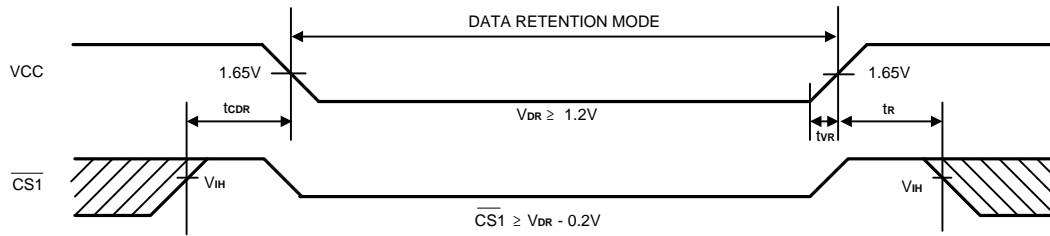
Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	1.2	2.2	V	$\overline{CS}_1 \geq VCC - 0.2V$ or $CS_2 \leq 0.2V$ or $\overline{LB} = \overline{HB} \geq VCC-0.2V$
I_{CCDR}	Data Retention Current	-	0.2*	μA	$VCC = 1.2V$, $\overline{CS}_1 \geq VCC - 0.2V$ or $CS_2 \leq 0.2V$ or $\overline{LB} = \overline{HB} \geq VCC-0.2V$ $V_{IN} \geq VCC-0.2V$ or $V_{IN} \leq 0.2V$
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}	-	ns	
t_{VR}	VCC Rising Time from Data Retention Voltage to Operating Voltage	5	-	ms	

* LP62E16512 - 70LLI

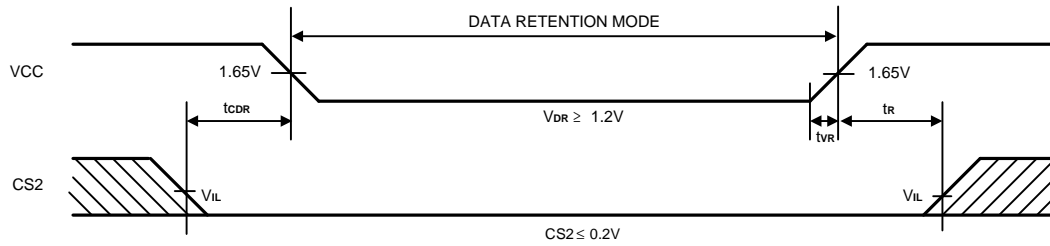
I_{CCDR} : max. $0.1\mu\text{A}$ at $T_A = 25^{\circ}\text{C}$
($0.2\mu\text{A}$ at $T_A = 0^{\circ}\text{C}$ to $+40^{\circ}\text{C}$)



Low VCC Data Retention Waveform (1) (CS1 Controlled)



Low VCC Data Retention Waveform (2) (CS2 Controlled)



Ordering Information

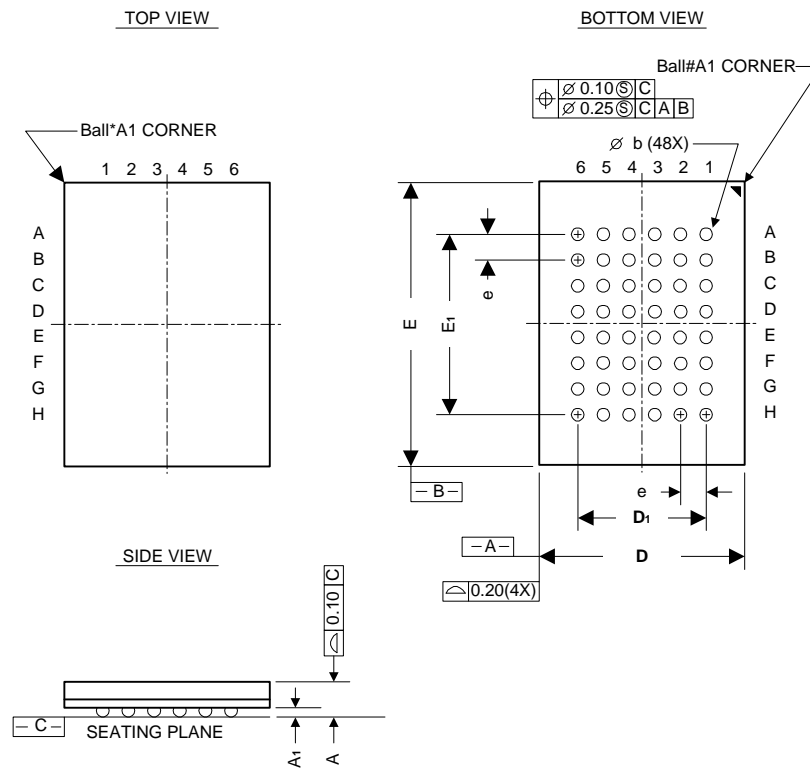
Part No.	Access Time(ns)	Operating Current Max.(mA)	Standby Current Max.(uA)	Package
LP62E16512U-70LLI	70	40	10	48L CSP



Package Information

**48LD CSP (8 x 10 mm) Outline Dimensions
(48TFBGA)**

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	---	---	1.20
A ₁	0.20	0.25	0.30
A ₂	0.48	0.53	0.58
D	7.90	8.00	8.10
E	9.90	10.00	10.10
D ₁	---	3.75	---
E ₁	---	5.25	---
e	---	0.75	---
b	0.30	0.35	0.40

Notes:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. BALL PAD OPENING OF SUBSTRATE IS Φ 0.3mm (SMD)
SUGGEST TO DESIGN THE PCB LAND SIZE AS Φ 0.3mm (NSMD)