National Semiconductor

February 2003

LP8358
150mA, µCap, Low Dropout Voltage Regulator with Power Good

General Description

The LP8358 is a µCap, precise CMOS voltage regulator with low Power good output R_{DSON}.

It provides up to 150mA and consumes a typical of 10nA in shutdown mode. The LP8358 output stage is designed with a push pull output for faster transient recovery response.

The LP8358 is optimized to work with low value, low cost ceramic capacitors. The output typically require only 1µF of output capacitance for stability. The enable pin can be tied to V_{IN} for easy board layout.

The LP8358 is designed for portable, battery powered equipment applications with small space requirements.

The LP8358 is available in a 5-pin SOT-23 package. Performance is specified for the −40˚C to +125˚C temperature range and is available in a fixed 1.2V. For other output voltage options, please contact National Semiconductor.

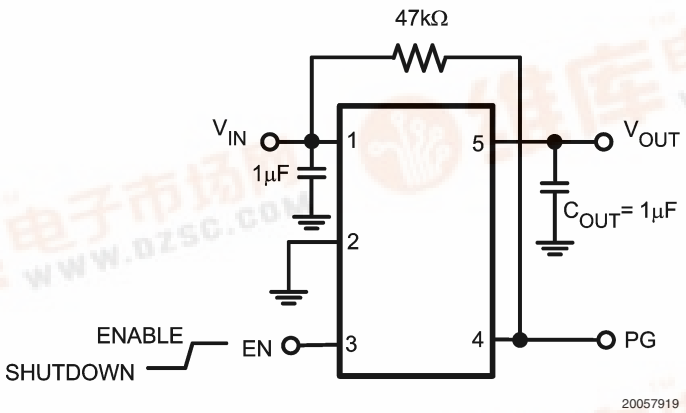
Features

- Low power good R_{DSON}: 20Ω
- Power good indicator
- Stability with low ESR capacitors
- Low ground current: 120µA
- 150mA output current
- "Zero" shutdown current mode
- Fast transient recovery response
- Auto discharge
- Thermal shutdown
- Current limiting

Applications

- Processor power-up sequencing
- Laptop, notebook and palm top computer
- PCMCIA V_{CC} and V_{PP} regulation switching

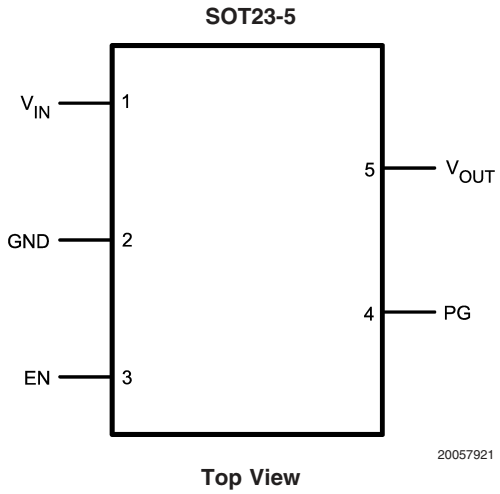
Typical Application



Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT-23	LP8358MF-1.2	LH2B	1k Units Tape and Reel	MF05A
	LP8358MFX-1.2		3k Units Tape and Reel	

Connection Diagram

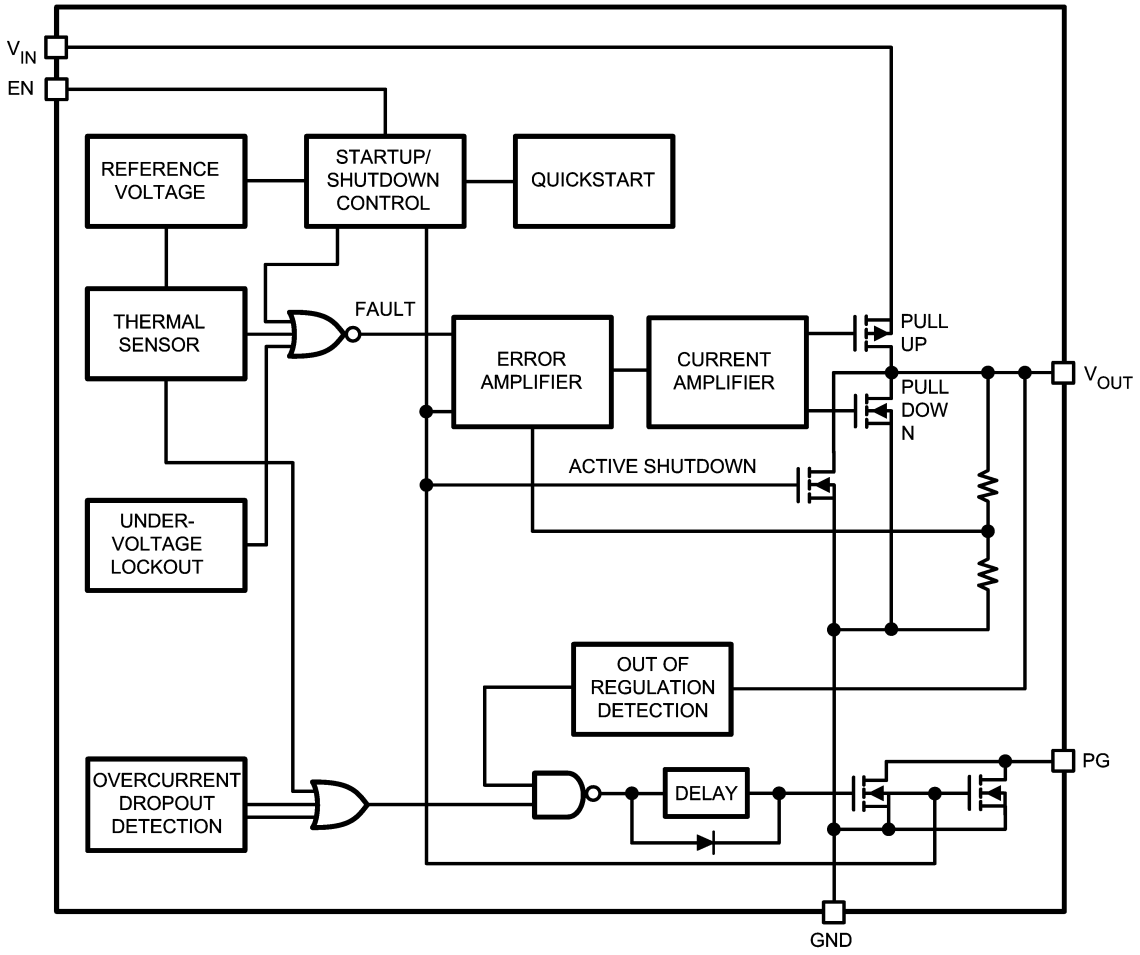


Top View

Pin Description

Pin Number	Pin Name	Pin Function
1	V_{IN}	Input Voltage
2	GND	Ground
3	EN	Enable Input Logic, Logic High = Enabled Logic Low = Shutdown (Do not leave open)
4	PG	Power Good Output
5	V_{OUT}	Output Voltage

Block Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Junction Temperature	150˚C
V_{IN}, V_{OUT}, V_{EN}	–0.3 TO 6.5V
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering (10 sec)	260˚C (lead temp)

Operating Ratings

Supply Voltages	
V_{IN}	2.7V to 6V
V_{EN}	0V to V_{IN}
Junction Temp. Range (Note 3)	–40˚C to +125˚C
Storage Temperature Range	–65˚C to 150˚C
Package Themal Resistance	
SOT23-5	235˚C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V_{IN} = 2.7V, I_L = 100µA, C_{OUT} = 1µF, $V_{EN} \geq$ 2.0V. **Boldface** limits apply over the entire operating temperature range, –40˚C to 125˚C.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_O	Output Voltage Accuracy	I_L = 100µA	-3 **-4**		3 **4**	%
$\Delta V_O/V_O$	Line Regulation	V_{IN} = 2.7V to 6V	**–0.3**		**0.3**	%
$\Delta V_O/V_O$	Load Regulation	I_L = 0.1mA to 150mA (Note 6)		1	4	%
I_Q	Quiescent Current	$V_{EN} \leq$ 0.4V (Shutdown), PG = NC		0.01	1	µA
I_{GND}	Ground Pin Current (Note 5)	I_L = 0mA, $V_{EN} \geq$ 2.0V (active), V_{IN} = 6V		120	180	µA
		I_L = 150mA, $V_{EN} \geq$ 2.0V (active), V_{IN} = 6V		160	225	
PSRR	Power Supply Rejection Ratio	f = 120Hz, C_{OUT} = 4.7µF, I_L= 150mA		62		dB
I_{LIMIT}	Current Limit	V_{OUT} = 0V	**160**	350		mA
Thermal Protection						
	Thermal Shutdown Temperature			150		˚C
Enable Input						
V_{IL}	Enable Input Voltage Level	Logic Low (off) , V_{IN} = 5.5V			**0.4**	V
V_{IH}		Logic High (on), V_{IN} = 5.5V	**2**			V
I_{IL}	Enable Input Current	$V_{IL} \leq$ 0.4V, V_{IN} = 5.5V		0.01		µA
I_{IH}		$V_{IH} \geq$ 2.0V, V_{IN} = 5.5V		0.01		µA
Power Good						
V_{PG}	Low Threshold	% of V_{OUT} (PG ON)	89			%
	High Threshold	% of V_{OUT} (PG OFF)			97	
V_{OL}	PG Output Logic-Low Voltage	$I_{POWERGOOD}$ = 100µA, Fault Condition		2.0	10.0	mV
R_{DSON}	Power Good Output On - Resistance	$I_{POWERGOOD}$ = 1mA, Fault Condition		20		Ω
I_{PG}	Power Good Leakage Current	Power Good Off, V_{PG} = 5.5V		0.01		µA
V_{PG} Delay	Delay Time to Power Good	See Timing Diagram	1	2.1	5	ms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: Typical Values represent the most likely parametric norm.

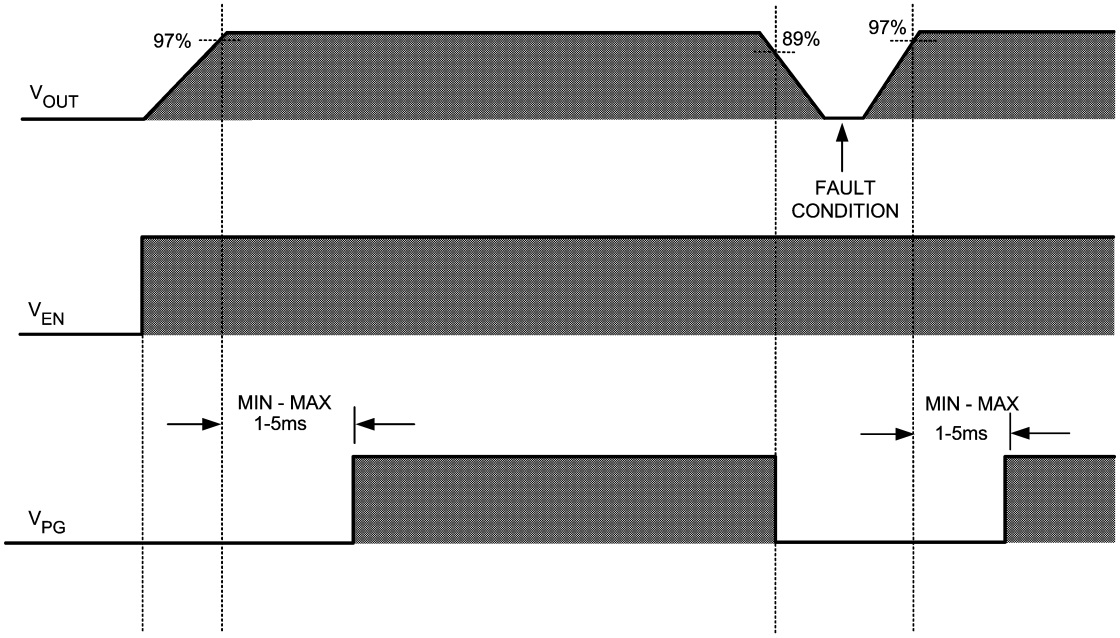
Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: Regulation is measured at constant junction temperature using low duty cycle pulse testing.

Electrical Characteristics (Continued)

Note 7: Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

Timing Diagram



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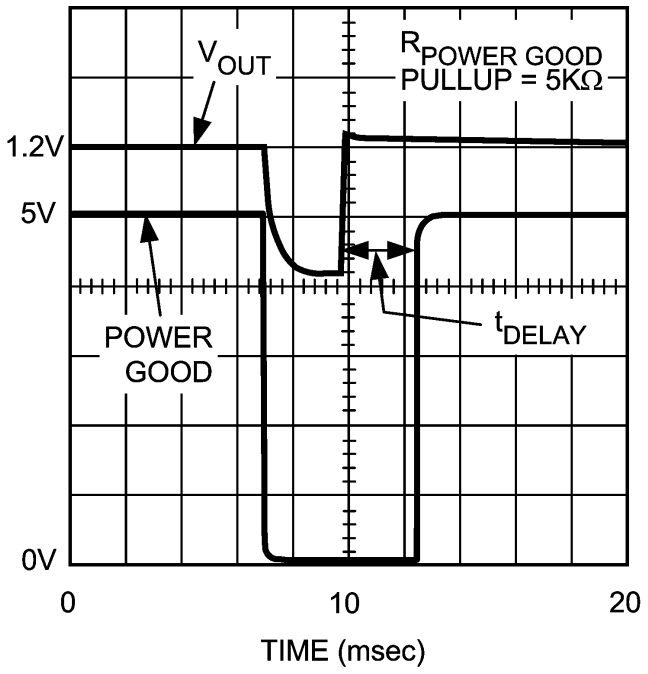
Typical delay time to power good



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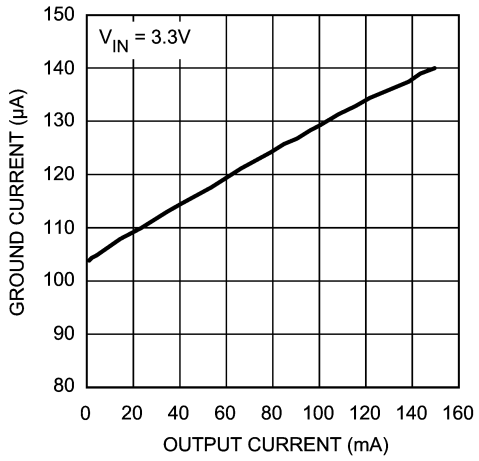
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = 3.3V, C_{OUT} = 1µF, T_A = 25˚C and powergood pull up resistor = 47kΩ.

Ground Current vs. Output Current



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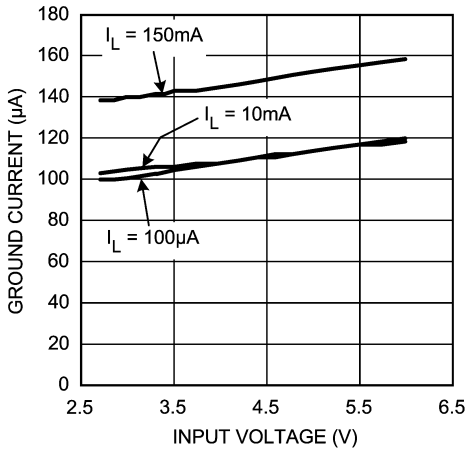
Ground Current vs. Input Voltage



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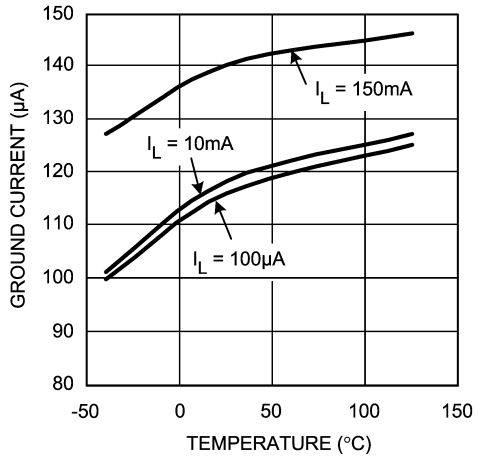
Ground Current vs. Temperature



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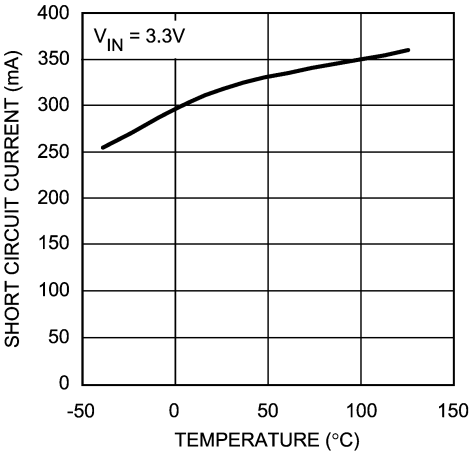
Short Circuit Current vs. Temperature



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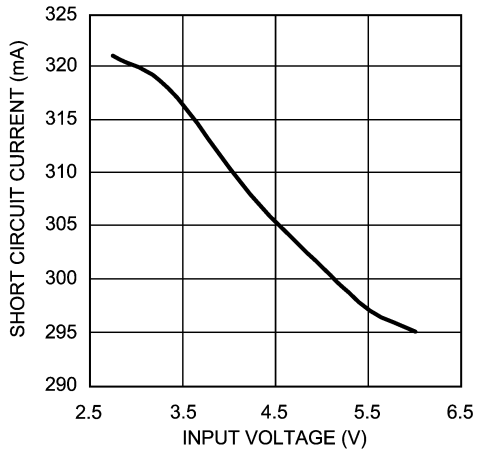
Short Circuit Current vs. Input Voltage



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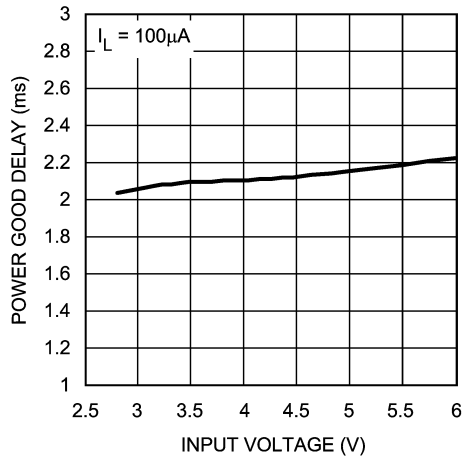
Power Good Delay vs. Input Voltge



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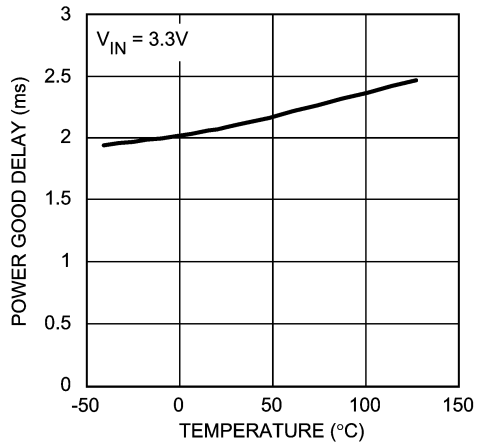
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = 3.3V, C_{OUT} = 1µF, T_A = 25˚C and powergood pull up resistor = 47kΩ. (Continued)

Power Good Delay vs. Temperature



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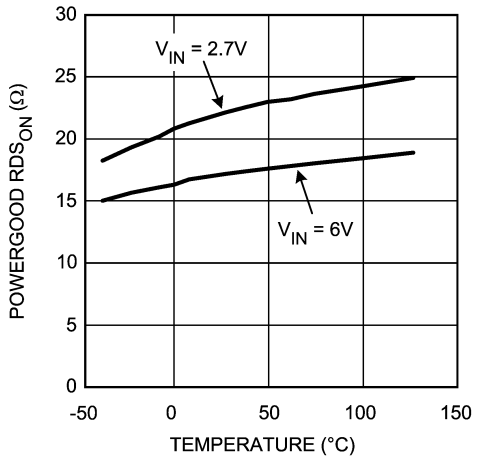
Power Good R_{DSON} vs. Temperature



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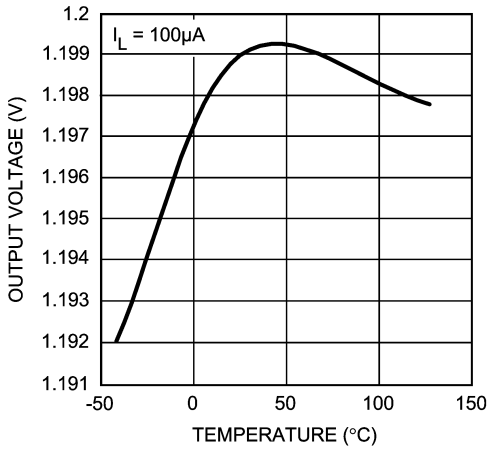
Output Voltage vs. Temperature



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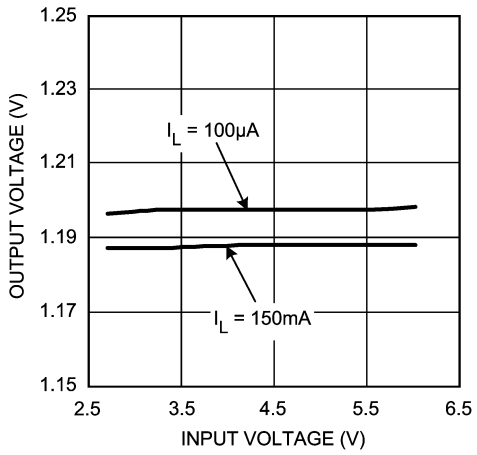
Output Voltage vs. Input Voltage



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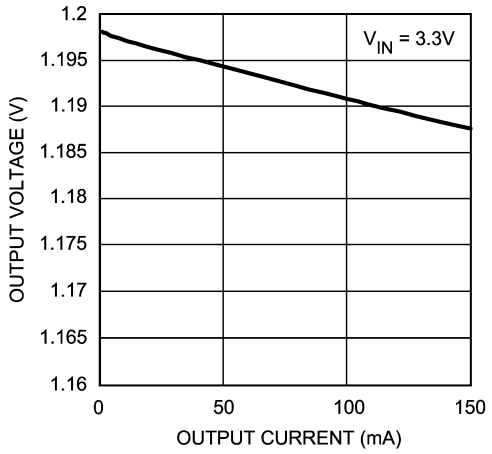
Output Voltage vs. Output Current



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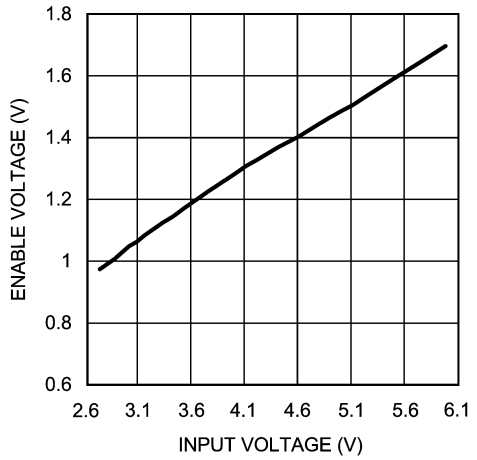
Enable Voltage vs. Input Voltage



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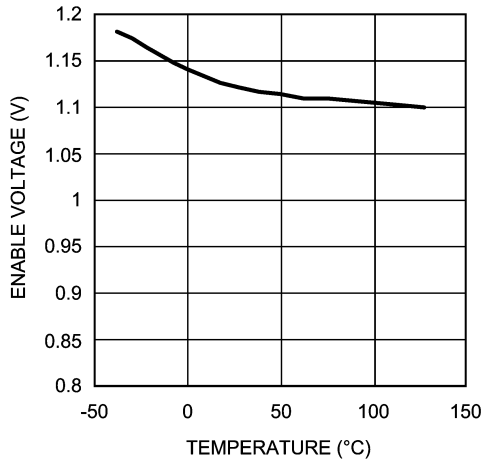
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = 3.3V, C_{OUT} = 1µF, T_A = 25˚C and powergood pull up resistor = 47kΩ. (Continued)

Enable Voltage vs. Temperature



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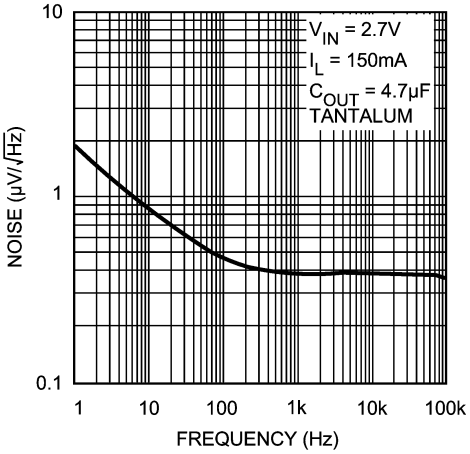
Voltage Noise vs. Frequency



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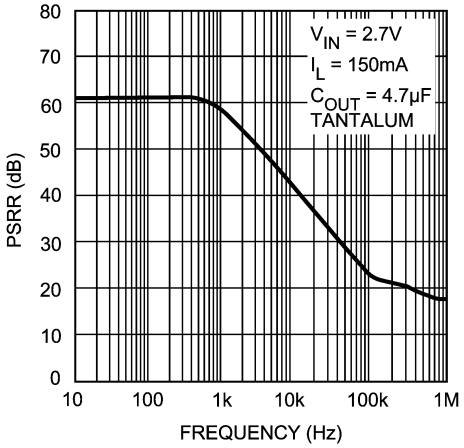
PSRR vs. Frequency



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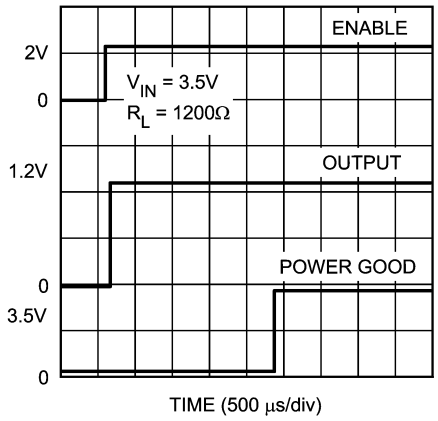
Power On Reset Delay Time



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Application Notes

The LP8358 is a linear regulator with power good output designed to be used with a low ESR, low cost ceramic capacitors.

EXTERNAL CAPACITORS

The LP8358 regulator requires an output capacitor to maintain stability. The capacitor must be at least 1µF or greater. The capacitor can be low-ESR ceramic chip capacitor, however for improved capacitance over temperature, tantalum capacitors can be used.

A 1µF input capacitor is recommend when the supply capacitance is more than 10 inches away from the device, or when the supply is a battery.

X7R dielectric ceramic capacitors are recommended because of their temperature performance. X7R-type capacitor change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much 50% and 60% respectively over their operating temperature range. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than a X7/R ceramic or a tantalum capacitor to ensure the same minimum capacitance value over the operating temperature range. Tantalum capacitors have a very stable dielectric (10% over their operating temperature range) and can also be used with this device.

ENABLE/SHUTDOWN

The LP8358 has an active high enable pin that allows the regulator to be disabled. Applying a Logic Level low (<0.4 V) to the Shutdown pin will cause the output to turn off, in this state current consumed by the regulator goes nearly to zero. Applying a Logic Level high (>2.0V) enables the output voltage. The enable/shutdown pin must not be left floating; a floating enable pin may cause an indeterminate state on the output.

ACTIVE SHUTDOWN

The LP8358 is designed with a N-channel MOSFET that acts as a shutdown clamp. The N-channel turns on when the device is disabled to allow the output capacitor and load to discharge

POWER GOOD

The power good output is an open-drain output with extreme low R_{DSON}. It is designed essentially to work as a power-on reset generator once the regulated voltage is up and/ or a fault condition. When a fault condition occurs, the output of the power good pin goes low. The power good output comes back up once the output has reached 97% of its nominal value and 1ms to 5ms delay has passed , see timing diagram.

The LP8358 internal circuit monitors overcurrent, temperature and falling output voltage. If one of these conditions is flagged this indicates a fault condition.

The flagged condition output is fed into an onchip delay circuit that drives the open drain output transistor.

TRANSIENT RESPONSE

The LP8358 implements a unique output stage to dramatically improve transient response recovery time. The output is a totem-pole configuration with a P-channel MOSFET pass device and a N-channel MOSFET clamp. The N-channel clamp is a significantly smaller device that prevents the output voltage from overshooting when a heavy load is removed. This feature helps to speed up the transient response by significantly decreasing transient response recovery time during the transition from heavy load to light load.

THERMAL BEHAVIOR

The LP8358 regulator has internal thermal shutdown to protect the device from over heating. Under all operating conditions, the maximum junction temperature of the LP8358 must be below 125˚C. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. The maximum power dissipation is

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

θ_{JA} is the junction-to-ambient thermal resistance, 235˚C/W for the LP8358 in the SOT23-5 package. T_A is the maximum ambient temperature $T_{J(MAX)}$ is the maximum junction temperature of the die, 125˚C.

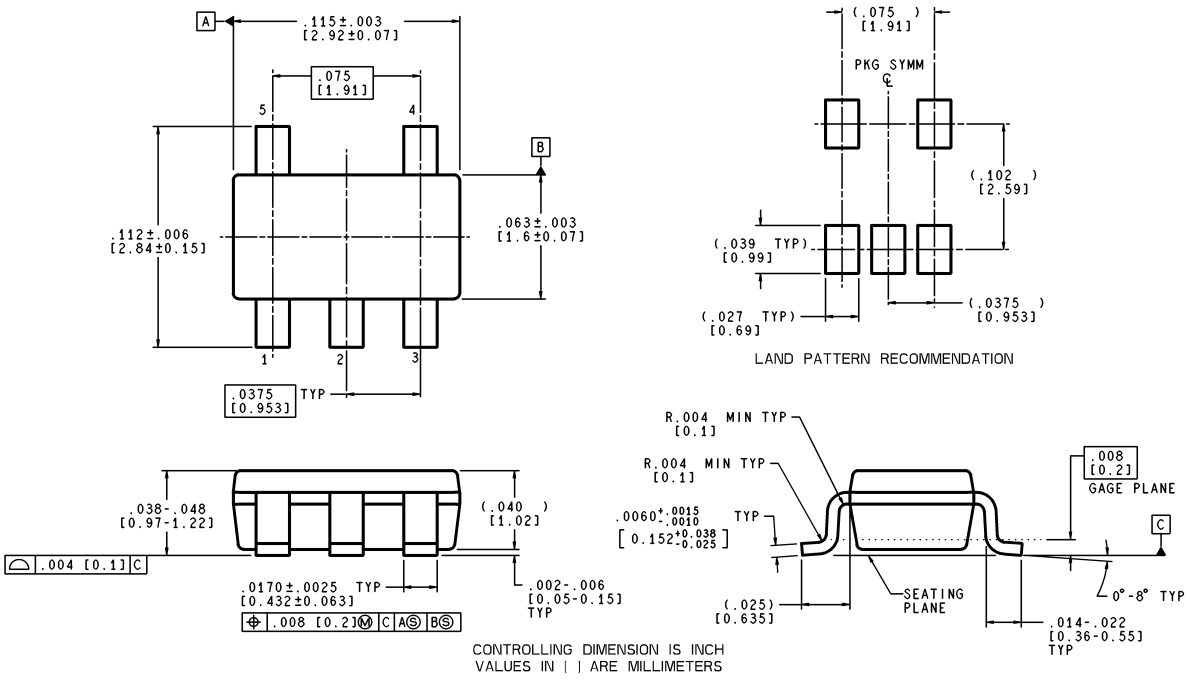
When operating the LP8358 at room temperature, the maximum power dissipation is 425mW.

The actual power dissipated by the regulator is

$$P_D = (V_{IN} - V_{OUT})I_L + V_{IN}\, I_{GND}$$

Substituting $P_{D(MAX)}$, determined above, for P_D and solving for the operating condition that is critical to the application will give the maximum operating condition for the regulator circuit. To prevent the device from entering thermal shutdown, maximum power dissipation cannot be exceeded.

Physical Dimensions inches (millimeters)
unless otherwise noted



MF05A (Rev A)

5-Pin SOT23-5
NSC Package Number MF05A

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