STANDARD
MICROSYSTEMS
CORPORATION

LPC47N252
ADVANCE INFORMATION

Advanced Notebook I/O Controller with On-Board FLASH

FEATURES

- 3.3V Operation with 5V Tolerant Buffers
- ACPI 1.1, PC99/PC2001 Compliant
- LPC Interface with Clock Run Support
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - 15 Direct IRQs
  - Four 8-Bit DMA Channels
  - ACPI SCI Interface
  - nSMI
  - Shadowed write only registers
- Internal 64K Flash ROM
  - Programmed From Direct Parallel Interface, 8051, or LPC Host
  - 2k-Byte Lockable Boot Block
  - Can be Programmed Without 8051 Intervention
- Three Power Planes
  - Low Standby Current in Sleep Mode
  - Intelligent Auto Power Management for Super I/O
- ACPI Embedded Controller Interface
- Configuration Register Set Compatible with ISA Plug-and-Play Standard (Version 1.0a)
- High-Performance Embedded 8051 Keyboard and System Controller
  - Provides System Power Management
  - System Watch Dog Timer (WDT)
  - 8042 Style Host Interface
  - Supports Interrupt and Polling Access
  - 256 Bytes Data RAM
  - On-Chip Memory-Mapped Control Registers
  - Access to RTC and CMOS Registers
  - Up to 16x8 Keyboard Scan Matrix
  - Two 16 Bit Timer/Counters
  - Integrated Full-Duplex Serial Port Interface
  - Eleven 8051 Interrupt Sources
  - Thirty-Two 8-Bit, Host/8051 Mailbox Registers
  - Thirty-six Maskable Hardware Wake-Up Events
  - Fast GATEA20
  - Fast CPU_RESET
  - Multiple Clock Sources and Operating Frequencies
  - IDLE and SLEEP Modes
  - Fail-Safe Ring Oscillator
- Advanced Infrared Communications Controller (IrCC 2.0)
  - IrDA V1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - Two IR Ports
  - Relocatable Base I/O Address
- Real-Time Clock
  - MC146818 and DS1287 Compatible
  - 256 Bytes of Battery Backed CMOS in Two 128-Byte Banks
  - 128 Bytes of CMOS RAM Lockable in 4x32 Byte Blocks
  - 12 and 24 Hour Time Format
  - Binary and BCD Format
  - <2µA Standby Current (typ)
- Two 8584-Style ACCESS.Bus Controllers
  - 8051 Controlled Logic Allows ACCESS.Bus Master or Slave Operation
  - ACCESS.Bus Controllers are Fully Operational on Standby Power
  - 2 Sets of Dedicated Pins per ACCESS.Bus Controller
- Four independent Hardware Driven PS/2 Ports
- 83 General Purpose I/O Pins
  - 36 Maskable Hardware Wake-Event Capable
  - 18 Programmable Open-Drain/Push-Pull Outputs
  - 16 Mapped into 8051 SFR Space
  - 24 LPC/8051-Addressable
- Three Programmable Pulse-Width Modulator Outputs
  - Independent Clock Rates
  - 6 Bit Duty Cycle Granularity
  - VCC1 and VCC2 operation mode
- Dual Fan Tachometer Inputs

- 2.88MB Super I/O Floppy Disk Controller
  - Relocatable to 480 Different Base I/O Addresses
  - 15 IRQ Options
  - 4 DMA Options
  - Open-Drain/Push-Pull Configurable Output Drivers
  - Licensed CMOS 765B Floppy Disk Controller
  - Advanced Digital Data Separator
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Low Power CMOS Design with Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - Supports Two Floppy Drives on the FDD Interface and Two Floppy Drives on the Parallel Port Interface
  - 12 mA FDD Interface Cable Drivers with Schmitt Trigger Inputs
- Licensed CMOS 765B Floppy Disk Controller Core
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
  - 12 mA Drivers and Schmitt Trigger Inputs
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
- Enhanced Digital Data Separator
  - Low Cost Implementation
  - No Filter Components Required
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode IBM PC/XT, PC/AT, and PS/2 Compatible Bi-directional Parallel Port
  - Enhanced Parallel Port EPP 1.7 and EPP 1.9 Compatible (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry to Prevent Printer Power-On Damage
  - Relocatable to 480 Different Base I/O Addresses
  - 15 IRQ Options
  - 4 DMA Options
  - Microsoft and HP compatible High Speed Mode
  - Floppy Disk Interface on Parallel Port
  - 8051-Controlled Parallel Port Mode
- Serial Port
  - High-Speed NS16550A-Compatible UART with 16-Byte Send/Receive FIFOs
  - Programmable Baud Rate Generator
  - Modem Control Circuitry Including 230k and 460k Baud
  - Relocatable to 480 Different Base I/O Addresses
  - 15 IRQ Options
- 208 Pin TQFP and FBGA Package Options

ORDERING INFORMATION

Order Numbers:
LPC47N252-SG for 208 Pin FBGA Package
LPC47N252-SD for 208 Pin TQFP Package

GENERAL DESCRIPTION

The LPC47N252 is a 208-pin 3.3V LPC-based ACPI 1.1 and PC99/PC2001 compliant Notebook I/O Controller with Fast Infrared for mobile applications.

The LPC47N252 incorporates a high-performance 8051-based keyboard controller; a 64k byte internal Flash ROM, four PS/2 ports; a real-time clock; SMSC's true CMOS 765B floppy disk controller with advanced digital data separator and 16-byte data FIFO; an NS16C550A-compatible UART, SMSC's advanced Infrared Communications Controller (IrCC 2.0) with a UART and a Synchronous Communications Engine to provide IrDA v1.1 (Fast IR) capabilities; one Multi-Mode parallel port with ChiProtect circuitry plus EPP and ECP support; two 8584-style Access Bus controllers with two Sets of Dedicated Pins per ACCESS.Bus Controller; a Serial IRQ peripheral agent interface; an ACPI Embedded Controller Interface; General Purpose I/O pins including eight pass through ports; three independently programmable pulse width modulators; two-floppy direct drive support; and maskable hardware wake-up events. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use. The parallel port is compatible with IBM PC/AT architecture, as well as EPP and ECP. The 8051 controller can also take control of the parallel port interface to provide remote diagnostics or "Flashing" of the Flash memory.

The LPC47N252 has three separate power planes to provide "instant on" and system power management functions. Additionally, the LPC47N252 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. Wake-up events and ACPI-related functions are supported through the SCI Interface.

The LPC47N252's configuration register set is compatible with the ISA Plug-and-Play Standard (Version 1.0a) and provides the functionality to support Windows '95.The legacy host Super I/O Configuration and Alternate Super I/O Configuration decode ranges comply with the Low Pin Count Interface Specification, Revision 1.0. Through internal configuration registers, each of the LPC47N252's logical device's I/O address, DMA channel and IRQ channel may be programmed. There are 480 I/O address location options, 15 IRQ options, and four DMA channel options for each logical device.

The LPC47N252 does not require any external filter components and is, therefore, easy to use and offers lower system cost and reduced board area. The LPC47N252 is software and register compatible with SMSC's proprietary 82077AA core.

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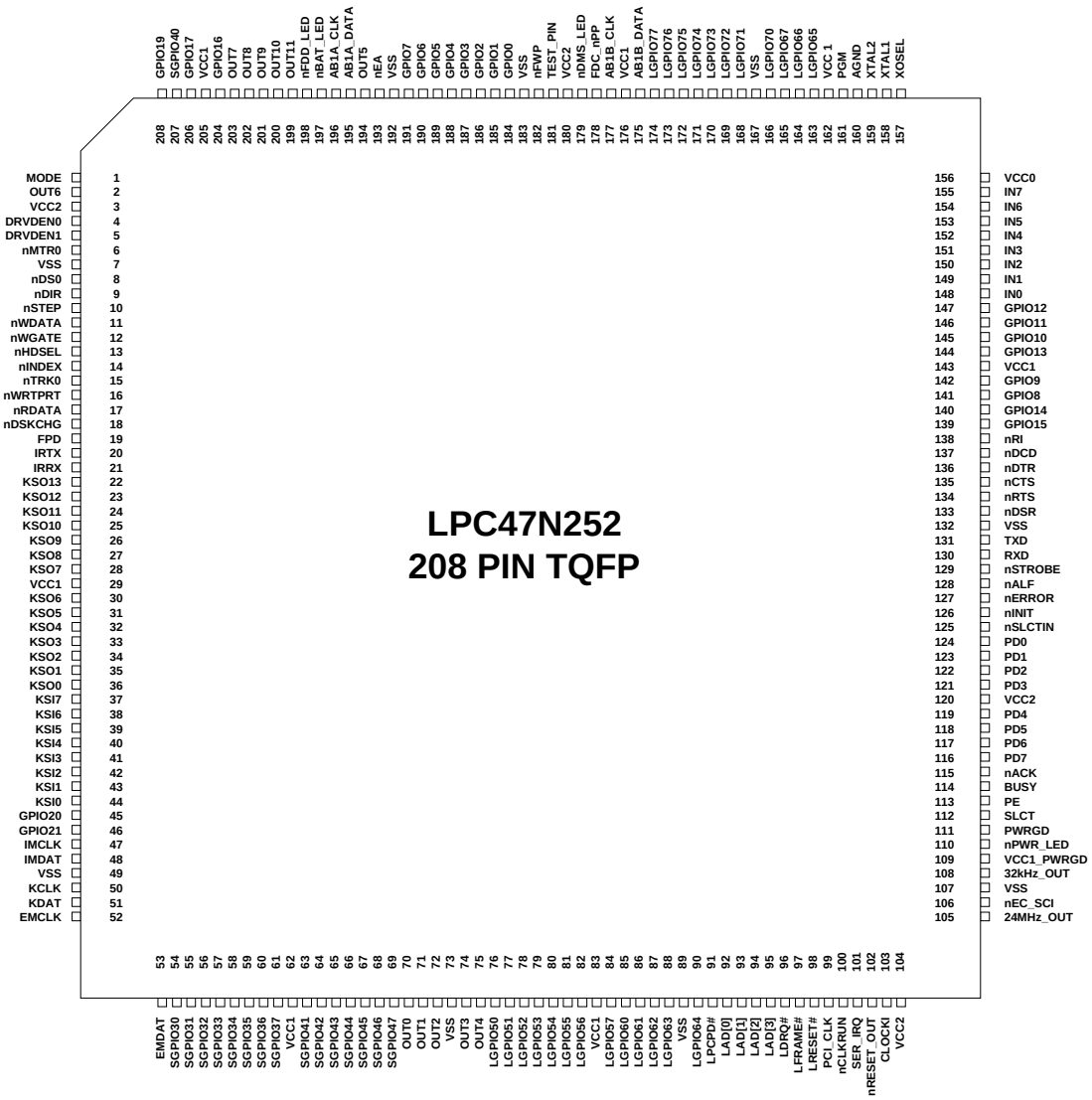

FIGURE 1 - LPC47N252 PIN CONFIGURATION