LR38516

Timing Generator IC for 350 k-pixel Progressive Scan Color CCDs

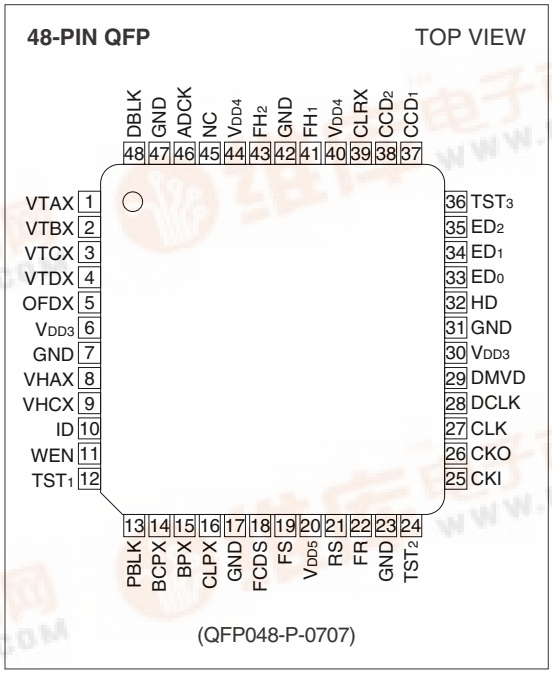
DESCRIPTION

The LR38516 is a CMOS timing generator IC which is designed for video-camcorders, and which generates timing pulses for driving 350 k-pixel progressive scan color CCD area sensors, synchronous pulses for TV signals and processing pulses for video signals.

FEATURES

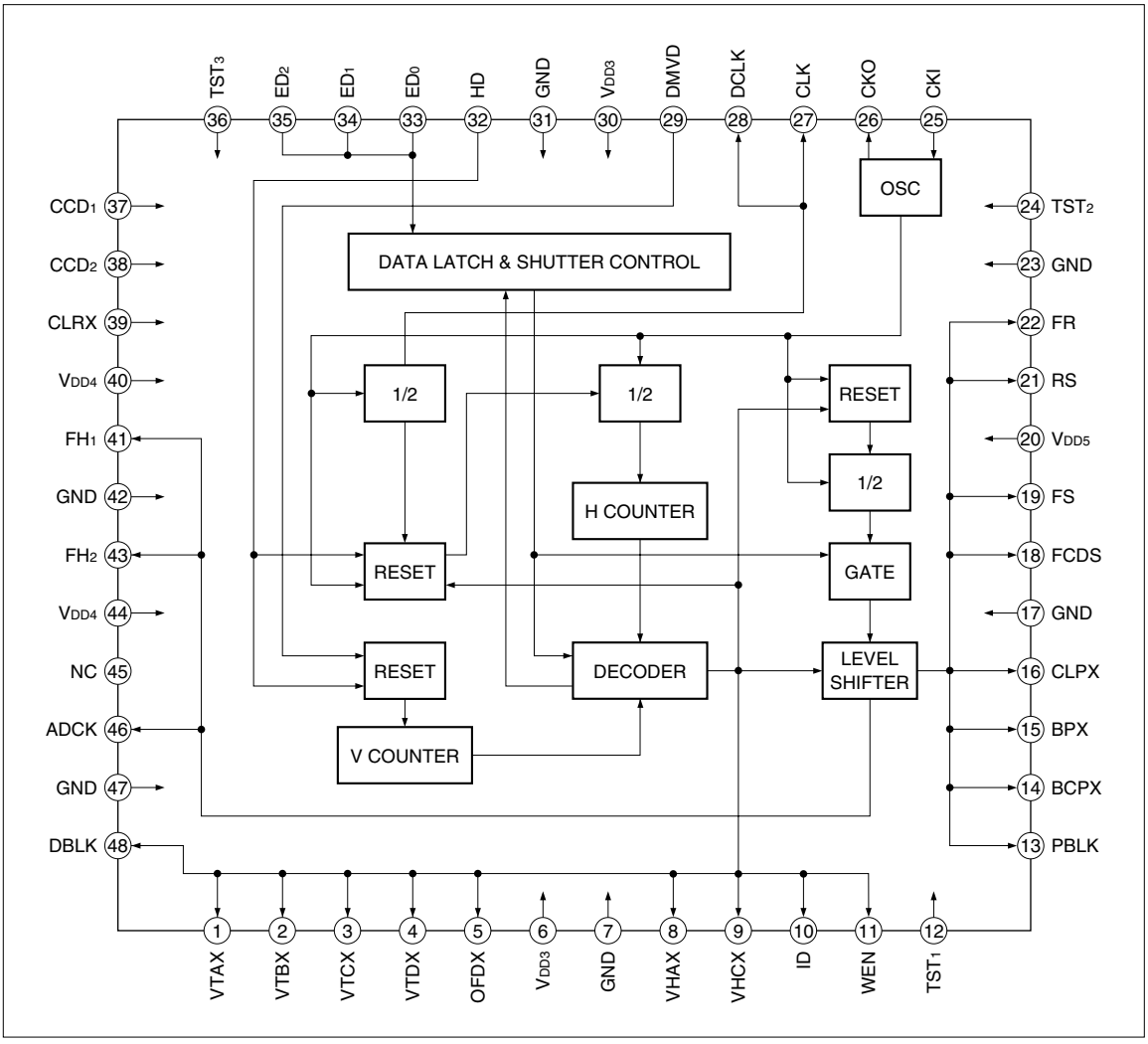
- Designed for 350 k-pixel progressive scan color CCD area sensors
- Frame rate : 30 frame/s
- Shutter speed can be controlled in 1H period using a serial code
- TV mode selection, power mode selection and the phase selection of DCLK can be also controlled by using a serial code
- +3 V, +4.5 V and +5 V power supplies
- Package :
  48-pin QFP (QFP048-P-0707) 0.5 mm pin-pitch

PIN CONNECTIONS



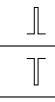
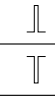
(QFP048-P-0707)

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	DESCRIPTION
1	VTAX	O3	⎍	Vertical transfer pulse output 1	A vertical transfer pulse for CCD. Connect to V_{1AX} pin of the vertical driver IC. For details, see "CONNECTION OF VERTICAL TRANSFER PULSES".
2	VTBX	O3	⎍	Vertical transfer pulse output 2	A vertical transfer pulse for CCD. Connect to V_{2AX} pin of the vertical driver IC. For details, see "CONNECTION OF VERTICAL TRANSFER PULSES".
3	VTCX	O3	⎎	Vertical transfer pulse output 3	A vertical transfer pulse for CCD. Connect to V_{3AX} pin of the vertical driver IC. For details, see "CONNECTION OF VERTICAL TRANSFER PULSES".
4	VTDX	O3	⎎	Vertical transfer pulse output 4	A vertical transfer pulse for CCD. Connect to V_{4AX} pin of the vertical driver IC. For details, see "CONNECTION OF VERTICAL TRANSFER PULSES".
5	OFDX	O3	⎎	OFD pulse output	A pulse that sweeps the charge of the photo-diode for the electronic shutter. Connect to OFD pin of CCD through the vertical driver IC and DC offset circuit. Held at H level at normal mode.
6	V_{DD3}	–	–	Power supply	Supply of +3 V power.
7	GND	–	–	Ground	A grounding pin.
8	VHAX	O3	⎎	Readout pulse output 1	A pulse that transfers the charge of the photo-diode to the vertical shift register. For details, see "CONNECTION OF VERTICAL TRANSFER PULSES".
9	VHCX	O3	⎎	Readout pulse output 3	A pulse that transfers the charge of the photo-diode to the vertical shift register. For details, see "CONNECTION OF VERTICAL TRANSFER PULSES".
10	ID	O3	⎍⎍	Line index pulse output	The pulse is used in color separator. The signal switches H and L at every line. H : R color line L : B color line
11	WEN	O3	⎎	Write enable output	Write enable output for low-speed shutter pulse.
12	TST_1	ICD3	–	Test pin 1	A test pin. Set open or to L level in the normal mode.
13	PBLK	O5	⎎	Pre-blanking pulse output	A pulse that corresponds to the cease period of the horizontal transfer pulse.
14	BCPX	O5	⎎	Optical black clamp pulse output	A pulse to clamp the optical black signal. Output stays low during the absence of effective pixels within the vertical blanking.
15	BPX	O5	⎎	Clamp pulse output	A pulse to clamp the signal. The phase is same as BCPX (pin 14). This pulse is continuous at horizontal cycle.
16	CLPX	O5	⎎	Clamp pulse output	A pulse to clamp the dummy outputs of CCD. The pulse stays high during the sweep-out period.
17	GND	–	–	Ground	A grounding pin.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	DESCRIPTION
18	FCDS	O6MA5		CDS pulse output 1	A pulse to clamp the feed-through level from CCD. The polarity can be changed by serial data. The output phase of FCDS is selected by serial data.
19	FS	O6MA5		CDS pulse output 2	A pulse to sample-hold the signal from CCD. The polarity can be changed by serial data. The output phase of FS is selected by serial data.
20	V_{DD5}	–	–	Power supply	Supply of +5 V power.
21	RS	O6MA5		S/H pulse output	A pulse to sample-hold the signal from CDS circuit. The polarity can be changed by serial data. The output phase of RS is selected by serial data.
22	FR	O6MA52		Reset pulse output	A pulse to reset the charge of output circuit. Connect to ϕ_R pin of CCD through the DC offset circuit. The output phase of FR is selected by serial data.
23	GND	–	–	Ground	A grounding pin.
24	TST_2	ICD3	–	Test pin 2	A test pin. Set open or to L level in the normal mode.
25	CKI	OSCI3	–	Clock input	An input pin for reference clock oscillation. Connect to CKO (pin 26) with R. Frequency : 24.54545 MHz (1 560 fH) fH = Horizontal frequency
26	CKO	OSCO3	–	Clock output	An output pin for reference clock oscillation. The output is the inverse of CKI (pin 25).
27	CLK	O6MA3		Clock output	An output pin to generate HD and VD pulses. Connect to clock input pin of SSG IC. Frequency : 12.27273 MHz (780 fH)
28	DCLK	O6MA3		Clock output	An output pin for DSP IC. The output phase of DCLK is selected by serial data step by 90˚. Frequency : 12.27273 MHz (780 fH)
29	DMVD	IC3		Vertical reference pulse input	An input pin for reference of vertical pulse. Connect to VD pin of DSP IC.
30	V_{DD3}	–	–	Power supply	Supply of +3 V power.
31	GND	–	–	Ground	A grounding pin.
32	HD	IC3		Horizontal reference pulse input	An input pin for reference of horizontal pulse. Connect to HD pin of DSP IC.
33	ED_0	IC3	–	Strobe pulse input	An input pin for the strobe pulse, to control the functions of LR38516. For details, see **"Serial Data Control"**.
34	ED_1	IC3	–	Shift register clock input	An input pin for the clock of the shift register, to control the functions of LR38516. For details, see **"Serial Data Control"**.
35	ED_2	IC3	–	Shift register data input	An input pin for the data of the shift register, to control the functions of LR38516. For details, see **"Serial Data Control"**.
36	TST_3	ICD3	–	Test pin 3	A test pin. Set open or to L level in the normal mode.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	DESCRIPTION
37	CCD_1	ICU4	–	CCD selection input 1	An input pin to select CCD. At CCD_1 = H and CCD_2 = H 1/4-type 350 k-pixel CCD (at NTSC) At CCD_1 = H and CCD_2 = L 1/3-type 350 k-pixel CCD (at NTSC)
38	CCD_2	ICU4	–	CCD selection input 2	
39	CLRX	ICU4	–	Data clear input	An input pin for resetting all serial data at power on. Connect V_{DD} through the diode and GND through the capacitor.
40	V_{DD4}	–	–	Power supply	Supply of +4.5 V power.
41	FH_1	O6MA43	⎍	Horizontal transfer pulse output 1	A horizontal transfer pulse for CCD. Connect to ϕ_{H1} pin of CCD.
42	GND	–	–	Ground	A grounding pin.
43	FH_2	O6MA43	⎍	Horizontal transfer pulse output 2	A horizontal transfer pulse for CCD. Connect to ϕ_{H2} pin of CCD.
44	V_{DD4}	–	–	Power supply	Supply of +4.5 V power.
45	NC	–	–	No connection	No connection.
46	ADCK	O6MA4	⎍	AD clock output	An output pin for A/D converter. The output phase of ADCK is selected by serial data step by 90˚.
47	GND	–	–	Ground	A grounding pin.
48	DBLK	O3	⎍	Dummy composite output	Composite blanking pulse. Vertical : 33H period

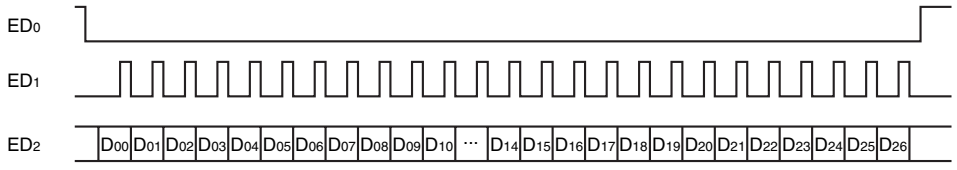
IC3 : Input pin (CMOS level)
ICU4 : Input pin (CMOS level with pull-up resistor)
ICD3 : Input pin (CMOS level with pull-down resistor)
O3 : Output pin
O6MA3 : Output pin
O6MA4 : Output pin
O6MA43 : Output pin
O5 : Output pin
O6MA5 : Output pin
O6MA52 : Output pin
OSCI3 : Input pin for oscillation
OSCO3 : Output pin for oscillation

CONNECTION OF VERTICAL TRANSFER PULSES

OUTPUT PULSE	LEVEL SHIFT, INVERT, MIX	1/4-TYPE 350 k	1/3-TYPE 350 k, 380 k AND 450 k
VTAX	3-level pulse with V driver	ϕ_{V3B}	ϕ_{V1}
VHAX			
VTCX	3-level pulse with V driver	ϕ_{V3A}	ϕ_{V3}
VHCX			
VTBX	2-level pulse with V driver	ϕ_{V2}	ϕ_{V2}
VTDX	2-level pulse with V driver	ϕ_{V1}	ϕ_{V4}

Serial Data Control

SERIAL DATA INPUT TIMING



The data on ED_2 is latched in the register at the rising edge of ED_1.
The data of D_{13} is effective. Other data are effective at next horizontal line of readout horizontal line while VHAX and VHCX are active.
ED_0 has to be kept L level in effective data input period.

SERIAL DATA INPUTS

DATA	NAME	FUNCTION	DATA = L	DATA = H	AT CLRX = L
D_{00}-D_{09}	SD_0-SD_9	Electronic shutter speed control	–		All L
D_{10}	SMD_0	Electronic shutter mode control	–		L
D_{11}	SMD_1				L
D_{12}	TVMD	TV mode selection	NTSC	–	L
D_{13}	PWSA	Power save control	Normal	Power save	–
D_{14}	ML_1	Phase control	–		L
D_{15}	ML_2				L
D_{16}	MA_1		–		L
D_{17}	MA_2				L
D_{18}	PLCH	Polarity control of FCDS, FS and RS pulses	Negative	Positive	L
D_{19}	MR_1	Phase control	–		L
D_{20}	MR_2				L
D_{21}	MC_1		–		L
D_{22}	MC_2				L
D_{23}	MS_1		–		L
D_{24}	MS_2				L
D_{25}	MF_1		–		L
D_{26}	MF_2				L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{DD3}, V_{DD4}, V_{DD5}	−0.3 to +6.0	V
Input voltage	V_{I3}	−0.3 to V_{DD3} + 0.3	V
	V_{I4}	−0.3 to V_{DD4} + 0.3	V
Output voltage	V_{O3}	−0.3 to V_{DD3} + 0.3	V
	V_{O4}	−0.3 to V_{DD4} + 0.3	V
	V_{O5}	−0.3 to V_{DD5} + 0.3	V
Operating temperature	T_{OPR}	−20 to +70	˚C
Storage temperature	T_{STG}	−55 to +150	˚C

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD3} = 3.0±0.3 V, V_{DD4} = 4.5±0.45 V, V_{DD5} = 5.0±0.5 V, T_{OPR} = −20 to +70 ˚C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL3}				0.2V_{DD3}	V	1, 2
Input "High" voltage	V_{IH3}		0.8V_{DD3}			V	
Input "Low" voltage	V_{IL4}				0.2V_{DD4}	V	3
Input "High" voltage	V_{IH4}		0.8V_{DD4}			V	
Input "Low" current	$\lvert I_{IL3-1} \rvert$	V_I = 0 V			1.0	µA	1
Input "High" current	$\lvert I_{IH3-1} \rvert$	V_I = V_{DD3}			1.0	µA	
Input "Low" current	$\lvert I_{IL3-2} \rvert$	V_I = 0 V			1.0	µA	2
Input "High" current	$\lvert I_{IH3-2} \rvert$	V_I = V_{DD3}	2.0		30	µA	
Input "Low" current	$\lvert I_{IL4} \rvert$	V_I = 0 V	4.0		60	µA	3
Input "High" current	$\lvert I_{IH4} \rvert$	V_I = V_{DD4}			2.0	µA	
Output "Low" voltage	V_{OL3-1}	I_{OL} = 2 mA			0.4	V	4
Output "High" voltage	V_{OH3-1}	I_{OH} = −2 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL3-2}	I_{OL} = 2 mA			0.4	V	5
Output "High" voltage	V_{OH3-2}	I_{OH} = −1 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL3-3}	I_{OL} = 3 mA			0.4	V	6
Output "High" voltage	V_{OH3-3}	I_{OH} = −3 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL4-1}	I_{OL} = 4 mA			0.4	V	7
Output "High" voltage	V_{OH4-1}	I_{OH} = −4 mA	V_{DD4} − 0.5			V	
Output "Low" voltage	V_{OL4-2}	I_{OL} = 12 mA			0.4	V	8
Output "High" voltage	V_{OH4-2}	I_{OH} = −12 mA	V_{DD4} − 0.5			V	
Output "Low" voltage	V_{OL5-1}	I_{OL} = 4 mA			0.4	V	9
Output "High" voltage	V_{OH5-1}	I_{OH} = −2 mA	V_{DD5} − 0.5			V	
Output "Low" voltage	V_{OL5-2}	I_{OL} = 6 mA			0.4	V	10
Output "High" voltage	V_{OH5-2}	I_{OH} = −6 mA	V_{DD5} − 0.5			V	
Output "Low" voltage	V_{OL5-3}	I_{OL} = 12 mA			0.4	V	11
Output "High" voltage	V_{OH5-3}	I_{OH} = −12 mA	V_{DD5} − 0.5			V	

NOTES :

1. Applied to inputs (IC3, OSCI3).
2. Applied to input (ICD3).
3. Applied to input (ICU4).
4. Applied to output (OSCO3). (Output (OSCO3) measures on condition that input (OSCI3) level is 0 V or V_{DD3}.)
5. Applied to output (O3).
6. Applied to output (O6MA3).
7. Applied to output (O6MA4).
8. Applied to output (O6MA43).
9. Applied to output (O5).
10. Applied to output (O6MA5).
11. Applied to output (O6MA52).

PACKAGE

(Unit : mm)

48 QFP (QFP048-P-0707)