查询SN74ACT16245QDLREP供应商 捷多邦，专业PCB打样工厂，24小时加急出货

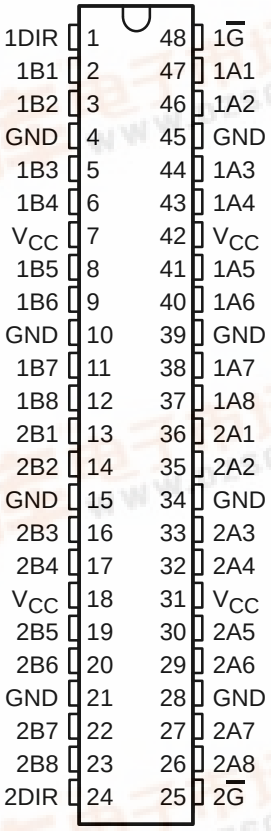
SN74ACT16245Q-EP
16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS677A – MAY 2002 – REVISED JULY 2002

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Member of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, highly accelerated stress test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life.

DL PACKAGE
(TOP VIEW)



description

The SN74ACT16245Q-EP is a 16-bit bus transceiver organized as dual-octal noninverting 3-state transceivers and designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The enable ($\overline{G}$) input can be used to disable the devices so that the buses are effectively isolated.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SSOP – DL	Tape and reel	SN74ACT16245QDLREP	ACT16245QEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

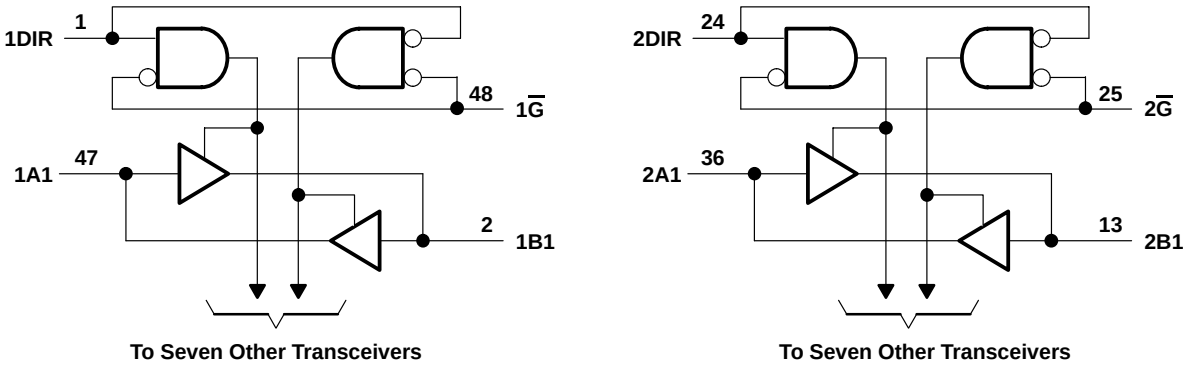
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2002, Texas Instruments Incorporated

FUNCTION TABLE
(each section)

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±24 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±24 mA
Continuous current through V_{CC} or GND . . . . . ±260 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . . 1.2 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage (see Note 4)	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–16	mA
I_{OL}	Low-level output current		16	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	–40	125	°C

NOTES: 3. Unused inputs should be tied to V_{CC} through a pullup resistor of approximately 5 kΩ or greater to keep them from floating. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4. All V_{CC} and GND pins must be connected to the proper-voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}		I_{OH} = –50 μA	4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
		I_{OH} = –16 mA	4.5 V	3.94			3.94		
			5.5 V	4.94			4.94		
		I_{OH} = –24 mA†	5.5 V				3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
		I_{OL} = 16 mA	4.5 V			0.36		0.5	
			5.5 V			0.36		0.5	
		I_{OL} = 24 mA†	5.5 V					0.5	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		16				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current I_I.
§ This is the increase in supply current for each input that is at one of the specified TTL-voltage levels rather than 0 V or V_{CC}.

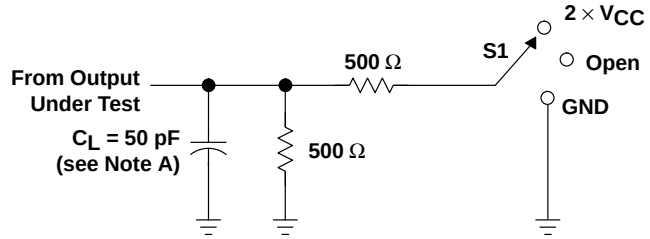
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	3.2	6.9	9.3	3.2	11.5	ns
t_{PHL}			2.6	6.4	9.2	2.6	11.1	
t_{PZH}	$\overline{G}$	B or A	2.7	6.4	9.1	2.7	10.9	ns
t_{PZL}			3.4	7.4	10.5	3.4	12.6	
t_{PHZ}	$\overline{G}$	B or A	5.8	9.2	11.6	5.8	13.4	ns
t_{PLZ}			5.5	8.5	10.8	5.5	12.7	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

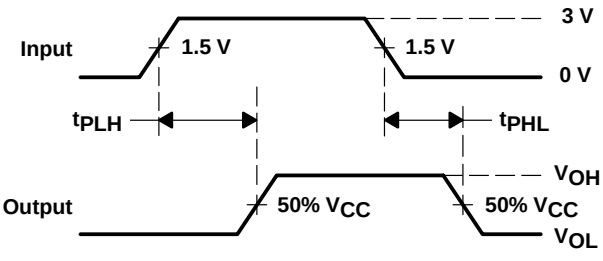
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	52	pF
		Outputs disabled		10	

PARAMETER MEASUREMENT INFORMATION

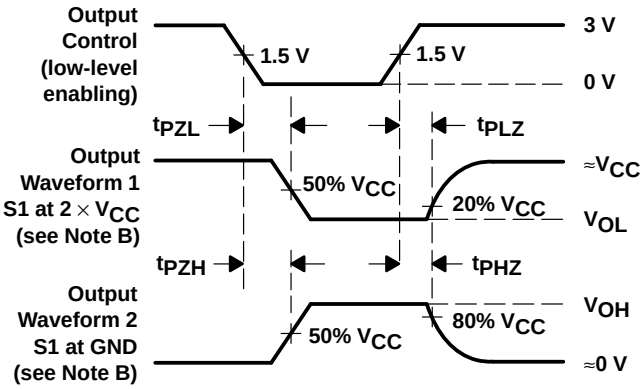


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2002, Texas Instruments Incorporated