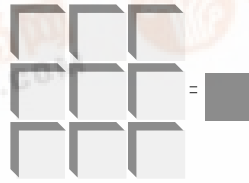


LSI/CSI



LS7213



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PROGRAMMABLE DIGITAL DELAY TIMER

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FEATURES:

- Eight timing ranges • Four modes
- RC controlled on-chip oscillator
- Power-On-Reset (POR)
- Reset input for delay abort
- Complementary outputs
- Delay-in-Progress Indicator output
- LS7213 (DIP), LS7213-S (SOIC) - See Figure 1

APPLICATIONS

Time delay relays for HVAC equipment and industrial controls.

DESCRIPTION

The LS7213 is a monolithic CMOS integrated circuit for generating programmable time-delays. The delay is initiated by a logic transition at the Trigger input and the completion of the delay is marked by a change of status at the Out1 and the Out2 outputs. Three inputs, D1, D2 and D3 select 1-of-8 scale factors, s . The delay, t_d is related to s by the expression, $t_d = s/f_{rc}$, where f_{rc} is the frequency at the RC input produced by an internal oscillator. An external resistor-capacitor pair connected to the RC pin controls the oscillator frequency. There are four modes of operation selected by inputs A and B. The operating modes are:

On-Delay (OND), Off-Delay (OFD), Dual-Delay (DLD) and One-Shot(OST). These modes are described below:

On-Delay (OND) Mode

A positive transition at the Trigger input starts the on-delay timer. At the end of the delay Out1 switches low and Out2 switches high. A negative transition at the Trigger input immediately aborts any on-delay in progress. If the Trigger input is switched low, Out1 if low will switch high and Out2 if high will switch low without delay. The states of Out2 in the preceding description applies only if Flashen input is low at the time of the Trigger input transition. See the Out2 pin section for a complete description.

Off-Delay (OFD) Mode

A negative transition at the Trigger input starts the off-delay timer. At the end of the delay Out1 switches high and Out2 switches low. A positive transition at the Trigger input immediately aborts any off-delay in progress. If the Trigger input is switched high, Out1 if high will switch low and Out2 if low will switch high without delay. The states of Out2 in the preceding description applies only if Flashen input is low at the time of the Trigger input transition. See the Out2 pin section for a complete description.

Dual-Delay (DLD) Mode

In Dual-Delay mode, the delay is generated for both positive and negative transitions at the Trigger input. A positive transition at the Trigger input starts the on-delay timer and aborts any off-delay timing in progress. At the end of the delay Out1 switches low and Out2 switches high. A negative transition at the Trigger input starts the off-delay timer and aborts any on-delay timing in progress. At the end of the delay Out1 switches high and Out2 switches low. The states of Out2 in the preceding description applies only if Flashen input is low at the time of the Trigger input transition. See the Out2 pin section for a complete description.

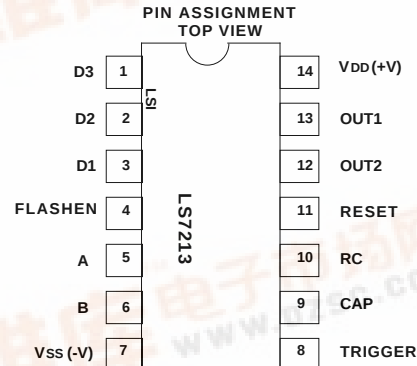


FIGURE 1

One-Shot(OST) Mode

A positive transition at the Trigger input causes Out1 to switch low and Out2 to switch high immediately and start the one-shot delay timer. At the end of the delay Out1 switches high and Out2 switches low. Thus in effect, a positive transition at the Trigger input produces a negative pulse at Out1 and a positive pulse at Out2. The one-shot delay timer is restarted with every positive trigger transition, thus rendering the Out1 and Out2 pulse-widths stretchable to any duration by periodic re-trigger. A negative transition at the Trigger input has no effect. The states of Out2 in the preceding description applies only if Flashen input is low at the time of the Trigger input transition. See the Out2 pin section for a complete description.

INPUTS/OUTPUTS

Following is a description of all the input/output pins and their functions.

Delay Select Inputs: D1, D2, D3 (Pin3, Pin2, Pin1)

The logic states applied to these three inputs enable the user to select a scale factor, s , for generating a delay, t_d , from Trigger input to Out1/Out2 outputs according to Table1. The delay is given by the expression:

$$t_d = s/f_{rc}$$

where, s is the scale factor, and f_{rc} is the oscillator frequency at the RC input. The sample delays in Table1 are based on an oscillator frequency, $f_{rc}=10\text{kHz}$.

TABLE 1. Delay Selection

D3	D2	D1	s	$t_d (=s/f_{rc})$
0	0	0	1×10^3	0.1sec
0	0	1	1×10^4	1.0sec
0	1	0	1×10^5	10.0sec
0	1	1	60×10^3	0.1min
1	0	0	60×10^4	1.0min
1	0	1	60×10^5	10.0min
1	1	0	3600×10^3	0.1hr
1	1	1	3600×10^4	1.0hr

D1, D2 and D3 inputs have internal pull-down resistors

Driver Outputs: Out1, Out2 (Pin 13, Pin 12)

Out1 is an output for driving DC loads requiring high current sink, such as relays, power transistors, etc. In steady-state condition Out1, with the exception of one-shot mode, is always inverse in polarity with respect to the Trigger input. Depending on the operating mode, the steady-state condition is reached immediately or after a specified delay following a change of state at the Trigger input. In one-shot mode, Out1 is always at logic high in the steady state, independent of the logic state of the Trigger input.

Out2 operates in two different modes depending on the state of the Flashen input.

If Flashen is at logic low then:

Out2 operates exactly as Out1 but with inverse polarity. In this mode, Out2 is an output for driving DC loads requiring high current source, such as relays, power transistors, etc. In steady-state condition Out2, with the exception of one-shot mode, is always at the same polarity as the Trigger input. Depending on the operating mode, the steady-state condition is reached immediately or after a specified delay following a change of state at the Trigger input. In one-shot mode Out2 is always at logic low in the steady state, independent of the logic state of the Trigger input.

If Flashen is at logic high then:

Out2 operates as a delay-in-progress indicator by generating periodic positive pulses during a delay timing. The pulse-rate, f_{pf} and the pulse-width t_{pf} at Out2 is controlled by an internal oscillator whose frequency, f_{cf} , is set by a capacitor connected to the Cap input. f_{pf} and f_{cf} are related by the following expressions:

$$f_{pf}=20/f_{cf}$$

for scale factors 1×10^3 and 1×10^4 and

$$f_{pf}=100/f_{cf}$$

for all other scale factors.

The pulse-width, t_{pf} for both pulse-rates is given by:

$$t_{pf}=2/f_{cf}$$

At the end of timeout, Out2 returns to logic low with the cessation of pulses.

Timer Start Input: Trigger (Pin 8)

Any logic transition at the Trigger input, positive or negative causes the outputs Out1 and Out2 to switch with or without delay, depending on the operating mode.

Any transition of the Trigger input also causes the logic states of the following inputs to be strobed into internal latches: A, B, D1, D2, D3 and Flashen. This prevents any changes at any of these inputs from disrupting the timer when a timeout is in progress. See the description of modes on Page1 and Out1, Out2 section on Page 2 for a complete description of the Trigger input. The Trigger input has an internal pull-down resistor.

When Reset is brought to logic high, all timing functions are aborted, the timer is cleared, Out1 is forced high and Out2 is forced low. Switching the Reset input low causes the outputs to be sampled by internal logic. Following this, any inconsistencies between the Trigger input and the Out1, Out2 outputs are resolved and the steady state is reached. Out1 out delay based on the status of the mode select input. For example, if the Trigger input is high, the Flashen input is high, the mode is off-delay when the Reset input is switched to low, Out1 and Out2 will immediately be switched to logic high and low respectively, from its forced reset condition. In this example, the mode is on-delay instead of off-delay, then Out1 and Out2 will be switched after the completion of the programmed delay.

It should be noted here that the states of Out1 and Out2 at reset condition and One-Shot mode steady state condition are the same namely, Out1 = 1 and Out2 = 0. Because of the one-shot mode, no change in Out1 and Out2 takes place when the Reset input is switched low, irrespective of the state of the Trigger input. The Reset input has an internal pull-down resistor. **NOTE:** A POR circuit (See Fig. 2) generates a reset signal that produces the same conditions described for the One-Shot mode (Pin 11).

Timer Oscillator Input: RC (Pin 10)

A resistor-capacitor pair connected to the RC input serves as the basic timing element for the delay timer oscillator. The oscillator frequency is given by the expression:

$$f_{rc}=1/0.9RC,$$

where R and C are the resistor and the capacitor connected to the RC input.

The delay, t_d , is given by the expression:

$$t_d=s/f_{rc},$$

where s is the scale factor selected by inputs D1, D2 and D3.

Flash Oscillator Input: Cap (Pin 9)

A capacitor, C, connected from the Cap input to ground sets the internal flash oscillator frequency according to the expression:

$$f_{cf}=(k/C) \times 10^{-6}$$

where k is a V_{DD} dependent constant ranging in value from 2.1 at $V_{DD}=3V$ to 4.8 at $V_{DD}=5V$. The flash oscillator frequency controls the pulse-rate, f_{pf} and the pulse width, t_{pf} of the outputs in flash mode according to the following relationships:

$$f_{pf}=20/f_{cf}$$

for scale factors 1×10^3 and 1×10^4 and

$$f_{pf}=100/f_{cf}$$

for all other scale factors; and for the pulse-width, $t_{pf}=2/f_{cf}$, for all scale factors.

Power Supplies V_{DD} , V_{SS} (Pin 14, Pin 7)

V_{DD} is the power supply positive terminal and V_{SS} is the power supply negative terminal or ground terminal.

Supply Current	IDD	4	-	125	-	100	-	85	μA	with c
		5	-	190	-	150	-	140	μA	
Input Voltages:										
Trigger High	VTH	3	1.6	-	1.6	2.0	1.6	-	V	-
		4	2.0	-	2.0	2.6	2.0	-	V	
		5	2.7	-	2.7	3.3	2.7	-	V	
Trigger Low	VTL	3	0.8	-	0.8	1.2	0.8	-	V	-
		4	1.2	-	1.2	1.8	1.2	-	V	
		5	1.5	-	1.5	2.1	1.5	-	V	
Trigger Hysteresis		3	-	-	0.4	1.2	-	-	V	-
		4	-	-	0.5	1.4	-	-	V	
		5	-	-	0.5	1.8	-	-	V	
All other inputs, High	VIH	3	1.5	-	1.5	-	1.5	-	V	-
		4	1.9	-	1.9	-	1.9	-	V	
		5	2.4	-	2.4	-	2.4	-	V	
All other inputs, Low	VIL	-	-	1.0	-	1.0	-	1.0	V	-
		-	-	1.3	-	1.3	-	1.3	V	
		-	-	1.6	-	1.6	-	1.6	V	
Input Currents:										
All inputs, Low	IIL	-	-	5	-	5	-	10	nA	Input
All inputs, High	IIH	3	0.9	2.5	0.8	2.0	0.5	1.6	μA	Input
		4	3.5	6.0	3.0	5.0	2.0	4.0	μA	
		5	8.0	12.0	7.0	10.0	5.0	8.0	μA	
Output Current:										
OUT1 Sink	IO1L	3	12.0	-	10.0	-	7.0	-	mA	Vo1 =
		4	14.0	-	12.0	-	9.0	-	mA	
		5	18.0	-	15.0	-	10.0	-	mA	
OUT1 Source	IO1H	3	1.8	-	1.5	-	1.0	-	mA	Vo1 =
		4	3.0	-	2.5	-	1.6	-	mA	
		5	3.5	-	3.0	-	2.0	-	mA	
OUT2 Sink	IO2L	3	5.4	-	4.5	-	3.0	-	mA	Vo2 =
		4	7.8	-	6.5	-	4.5	-	mA	
		5	9.0	-	7.5	-	5.5	-	mA	
OUT2 Source	IO2H	3	9.0	-	8.0	-	6.0	-	mA	Vo2 =
		4	13.0	-	11.0	-	8.0	-	mA	
		5	15.0	-	13.0	-	9.0	-	mA	
RC Oscillator:										
Frequency	frc		-	6.0	-	5.0	-	4.0	MHz	-
Resistor	R	3	6.8k	10M	8.2k	10M	10.0k	10M	W	-
		4	4.7k	10M	5.6k	10M	6.8k	10M	W	-
		5	3.9k	10M	4.7k	10M	5.6k	10M	W	-
Capacitor	C	-	no limit		no limit		no limit		μF	-
Flash Oscillator:										
Capacitor	C	-	no limit		no limit		no limit		μF	-
Constant	K	3	2.1	2.5	2.1	2.5	2.1	2.5	-	-
		4	3.2	3.2	3.2	3.7	3.2	3.7	-	-
		5	4.3	4.8	4.3	4.8	4.3	4.8	-	-

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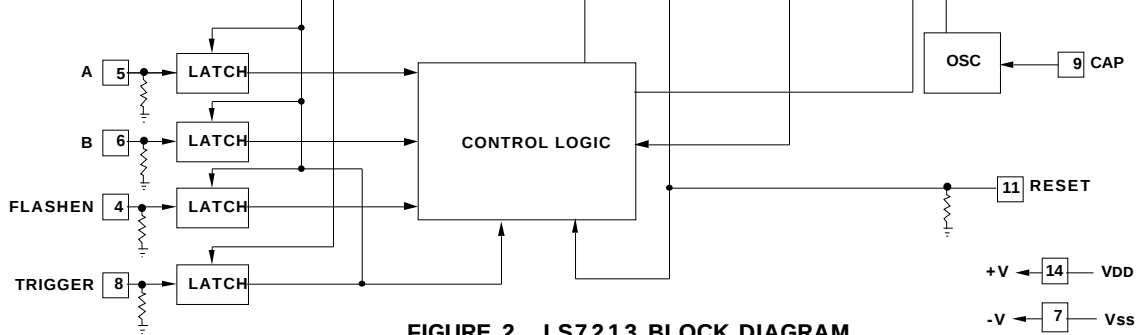


FIGURE 2. LS7213 BLOCK DIAGRAM

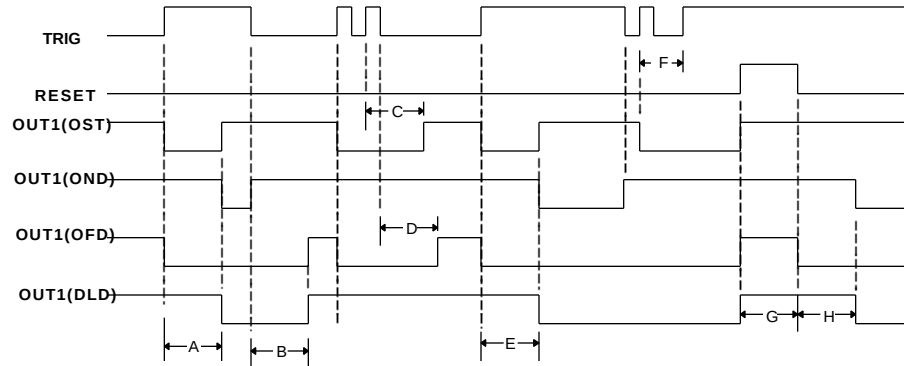


FIGURE 3. MODE ILLUSTRATION WITH TRIG, OUT1 AND RESET

- A. Turn-on delay in OND and DLD modes; Pulse-width in OST mode.
 B. Turn-off delay in OFD and DLD modes.
 C. Pulse-width extended by re-trigger in OST mode. No effect in OND and DLD modes because TRIG switches back low before turn-on delay has timed out.
 D. Turn-off delay in OFD mode.
 E. Turn-on delay in OND and DLD modes; pulse-width.
 F. No effect in OND, OFD and DLD modes because switching back to opposite levels.
 G. Time-out aborted and OUT1 forced high by RESET.
 H. After the removal of RESET, OUT1 switches to the level of TRIG immediately (OFD) or after the timeout (OND). No effect in OST.

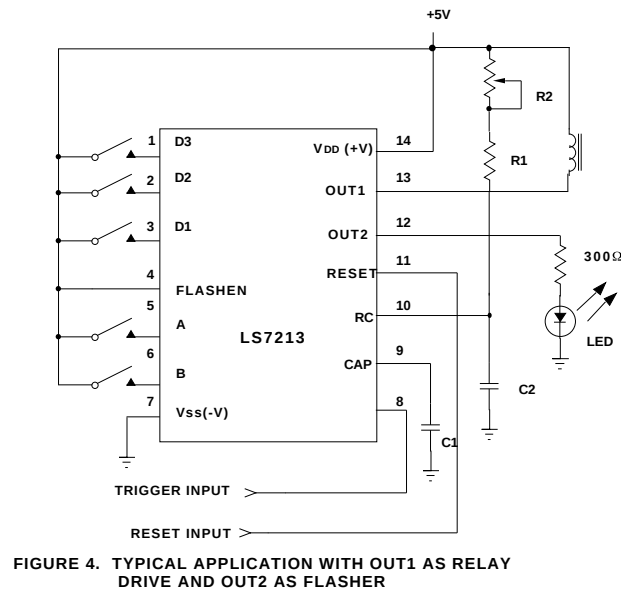


FIGURE 4. TYPICAL APPLICATION WITH OUT1 AS RELAY DRIVE AND OUT2 AS FLASHER

The table below shows the delays obtained with the following components $R1 = 56k\Omega$, $R2 = 500k\Omega$, $C2 = 0.002\mu F$. At any scale factor, the delay varies from minimum to maximum as the potentiometer is varied from minimum to maximum.

D3	D2	D1	TIMING RANGE
0	0	0	0.1 sec - 1 sec.
0	0	1	1 sec. - 10 sec.
0	1	0	10 sec - 100 sec.
0	1	1	0.1 min. to 1 min.
1	0	0	1 min. - 10 min
1	0	1	10 min. - 100 min.
1	1	0	0.1 hr. - 1 hr.
1	1	1	1 hr. - 10 hr.

$C1 = 0.22\mu F$, produces flash pulses of 0.1 sec duration at Out2