

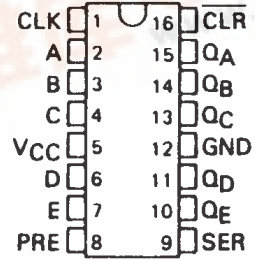
**SN5496, SN54LS96,  
SN7496, SN74LS96  
5-BIT SHIFT REGISTERS**

SDLS946 – MARCH 1974 – REVISED MARCH 1988

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

SN5496, SN54LS96 . . . J OR W PACKAGE  
SN7496 . . . N PACKAGE  
SN74LS96 . . . D OR N PACKAGE  
(TOP VIEW)

TYPE	TYPICAL	
	PROPAGATION DELAY TIME	POWER DISSIPATION
'96	25 ns	240 mW
'LS96	25 ns	60 mW



**description**

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

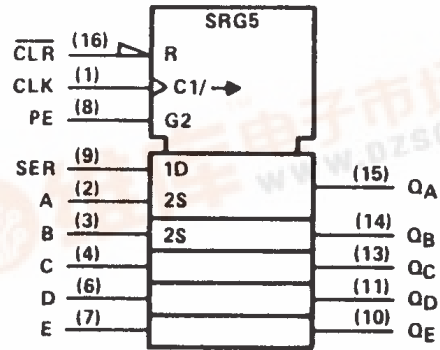
Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

**FUNCTION TABLE**

CLEAR	INPUTS					OUTPUTS							
	PRESET ENABLE	PRESET					CLOCK	SERIAL	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Q <sub>E</sub>
		A	B	C	D	E							
L	L	X	X	X	X	X	X	L	L	L	L	L	
L	X	L	L	L	L	X	X	L	L	L	L	L	
H	H	H	H	H	H	X	X	H	H	H	H	H	
H	H	L	L	L	L	L	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	
H	H	H	L	H	L	L	X	H	Q <sub>B0</sub>	H	Q <sub>D0</sub>	H	
H	L	X	X	X	X	L	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	
H	L	X	X	X	X	†	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	
H	L	X	X	X	X	†	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	

H = high level (steady state), L = low level (steady state)  
X = irrelevant (any input, including transition)  
† = transition from low to high level  
Q<sub>A0</sub>, Q<sub>B0</sub>, etc = the level of Q<sub>A</sub>, Q<sub>B</sub>, etc, respectively before the indicated steady-state input conditions were established.  
Q<sub>An</sub>, Q<sub>Bn</sub>, etc = the level of Q<sub>A</sub>, Q<sub>B</sub>, etc, respectively before the most recent † transition of the clock.

**logic symbol<sup>†</sup>**

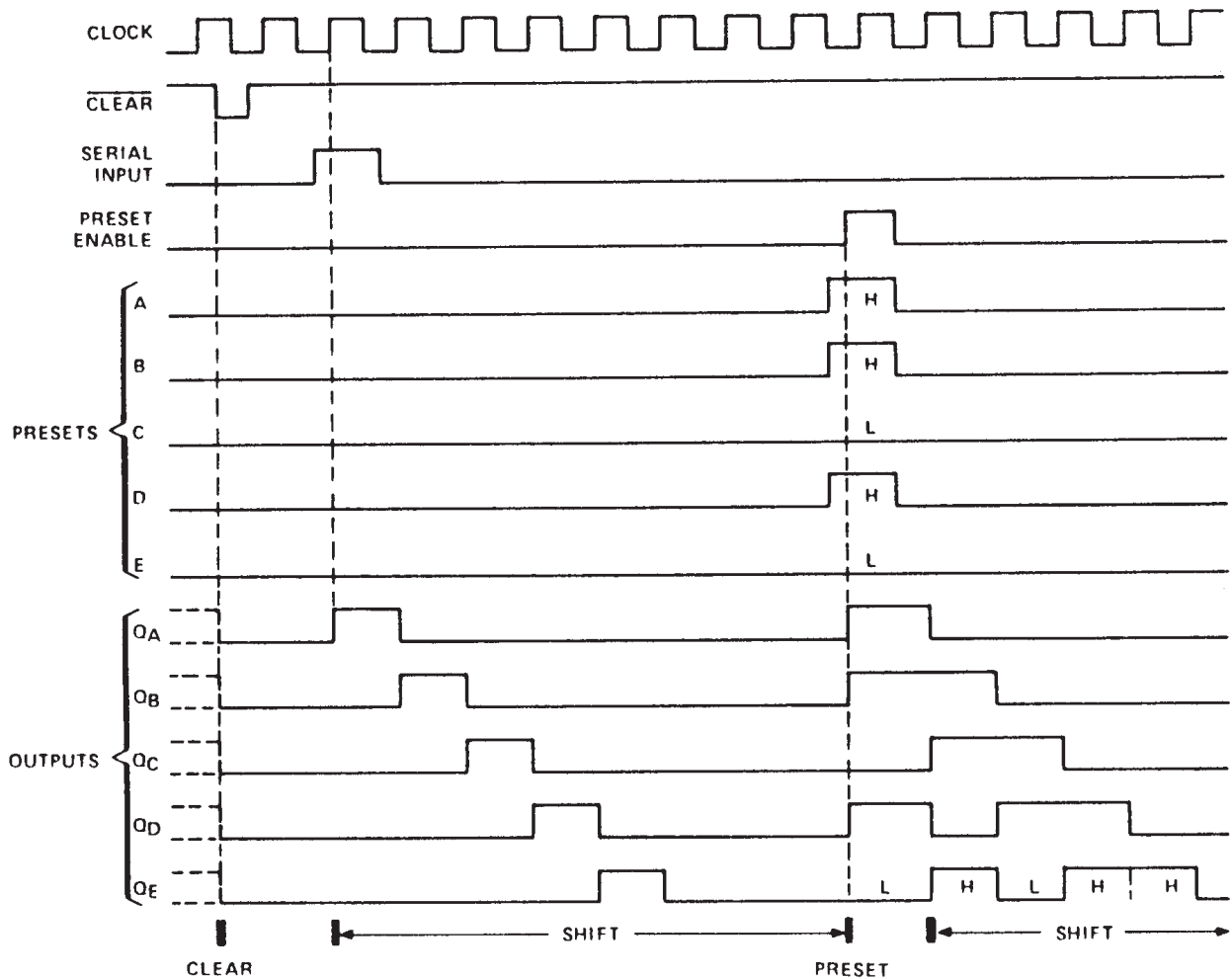


<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

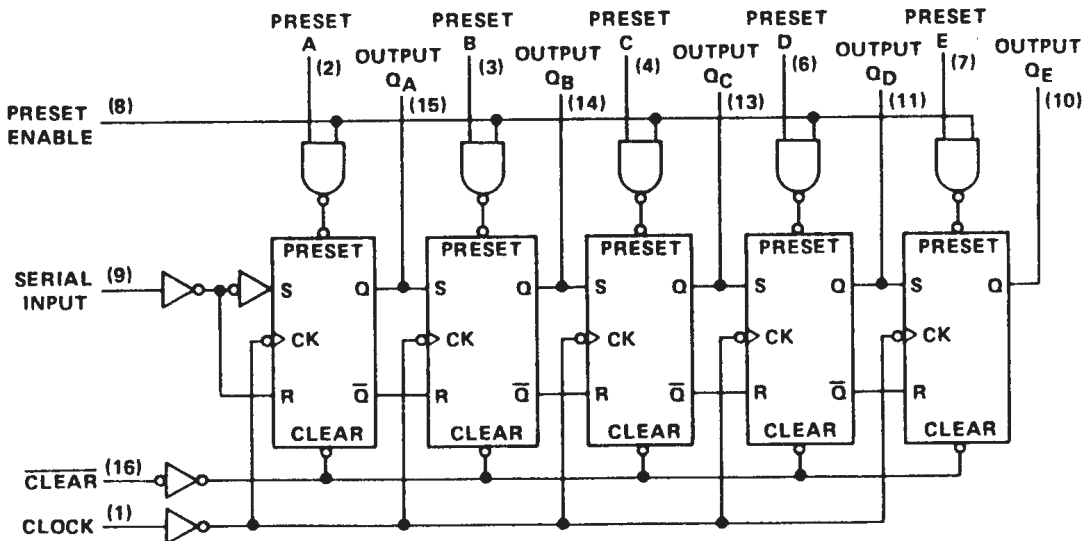


**SN5496, SN54LS96,  
SN7496, SN74LS96  
5-BIT SHIFT REGISTERS**

typical clear, shift, preset, and shift sequences



logic diagram (positive logic)





# SN5496, SN7496 5-BIT REGISTERS

## recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			16			16	mA
Clock frequency, $f_{clock}$	0		10	0		10	MHz
Width of clock input pulse, $t_{W(clock)}$	35			35			ns
Width of preset and clear input pulse, $t_W$	30			30			ns
Serial input setup time, $t_{SU}$ (see Figure 1)	30			30			ns
Serial input hold time, $t_H$ (see Figure 1)	0			0			ns
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN5496			SN7496			UNIT
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$	High-level input voltage		2			2			V
$V_{IL}$	Low-level input voltage				0.8			0.8	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2\text{ V}$ , $V_{IL} = 0.8\text{ V}$ , $I_{OH} = -400\ \mu\text{A}$	2.4	3.4		2.4	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2\text{ V}$ , $V_{IL} = 0.8\text{ V}$ , $I_{OL} = 16\text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5\text{ V}$			1			1	mA
$I_{IH}$	High-level input current	any input except preset enable			40			40	$\mu$ A
		preset enable			200			200	
$I_{IL}$	Low-level input current	any input except preset enable			-1.6			-1.6	mA
		preset enable			-8			-8	
$I_{OS}$	Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ , See Note 3		48	68		48	79	mA

<sup>†</sup>For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 3:  $I_{CC}$  is measured with the clear input grounded and all other inputs and outputs open.

## switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output from clock	$C_L = 15\text{ pF}$ , $R_L = 400\ \Omega$ , See Figure 1		25	40	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clock			25	40	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clear				55	ns

## SN54LS96, SN74LS96 5-BIT SHIFT REGISTERS

### recommended operating conditions

	SN54LS96			SN74LS96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Clock frequency, $f_{clock}$	0		25	0		25	MHz
Width of clock input pulse, $t_{W(clock)}$	20			20			ns
Width of preset and clear input pulse, $t_W$	30			30			ns
Serial input setup time, $t_{setup}$ (see Figure 1)	30			30			ns
Serial input hold time, $t_{hold}$ (see Figure 1)	0			0			ns
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>†</sup>	SN54LS96			SN74LS96			UNIT		
			MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX			
$V_{IH}$	High-level input voltage		2			2			V		
$V_{IL}$	Low-level input voltage				0.7			0.8	V		
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V		
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4	$I_{OL} = 8 \text{ mA}$		0.25	0.4	V
$I_I$	Input current at maximum input voltage	Preset enable	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$						0.5	0.5	mA
		All others							0.1	0.1	
$I_{IH}$	High-level input current	Preset enable	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$						100	100	$\mu$ A
		All others							20	20	
$I_{IL}$	Low-level input current	Preset enable	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$						-2	-2	mA
		All others							-0.4	-0.4	
$I_{OS}$	Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20		-100	-20		-100		mA	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 3}$	12		20	12		20		mA	

<sup>†</sup>For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25 \text{ }^{\circ}\text{C}$

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

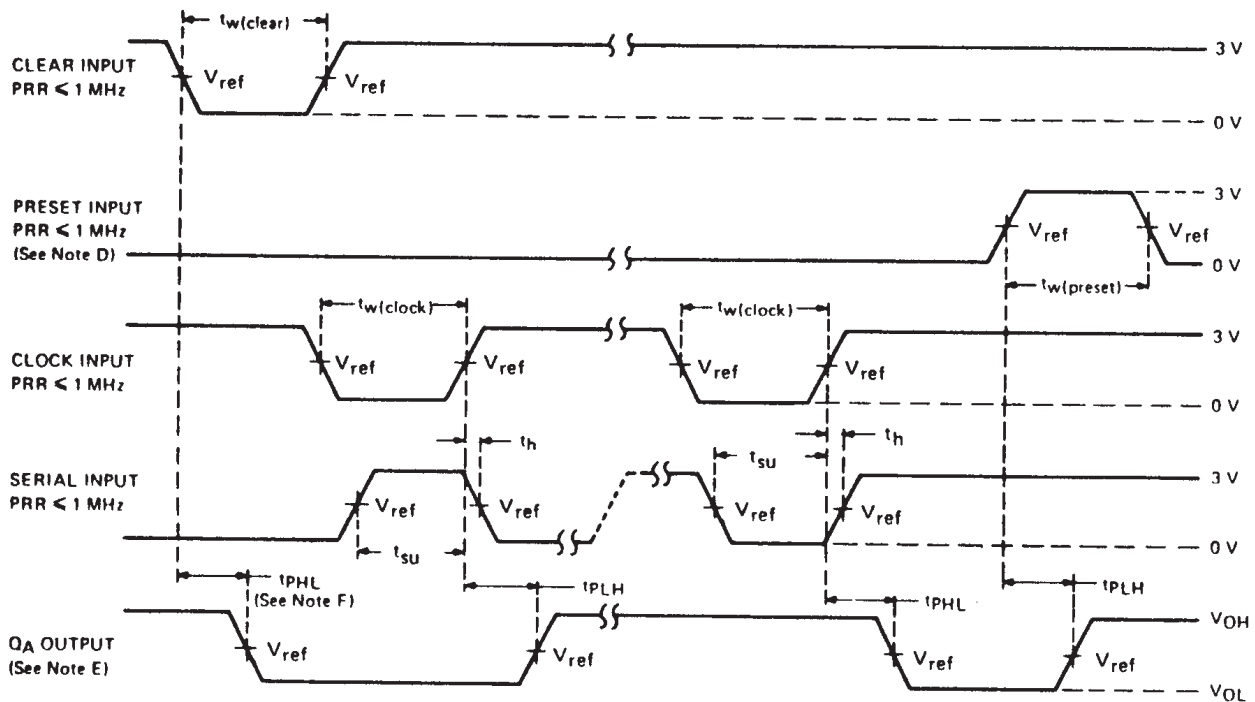
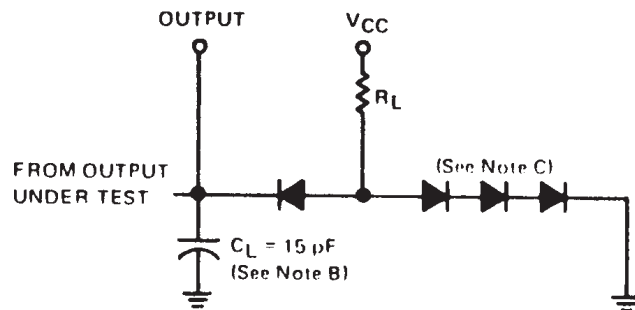
NOTE 3:  $I_{CC}$  is measured with the clear input grounded and all other inputs and outputs open.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Figure 1		25	40	ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock			25	40	ns	
$t_{PLH}$ Propagation delay time, low-to-high-level output from preset or preset enable				28	35	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear					55	ns

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A. Input pulses are supplied by pulse generators having the following characteristics: duty cycle  $\leq 50\%$ ,  $Z_{out} \approx 50 \Omega$ ; for '96,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns, and for 'LS96  $t_r = 15$  ns,  $t_f = 6$  ns.  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3064 or equivalent.  
 D. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.  
 E.  $Q_A$  output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.  
 F. Outputs are set to the high level prior to the measurement of  $t_{PHL}$  from the clear input.  
 G. For '96,  $V_{ref} = 1.5$  V; for 'LS96  $V_{ref} = 1.3$  V.

**FIGURE 1—SWITCHING TIMES**

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