

Ordering number : EN5889

Monolithic Linear IC

SANYO

LV1041M

Dolby Prologic Decoder



Overview

The LV1041M is a Dolby Prologic Surround signal-processing IC that implements in a single chip the functions of the Sanyo LV1016 and LA2786 ICs and a master volume control for the center and surround channels. This IC allows both systems of Dolby Prologic surround and digital surround to be formed into a single IC.

Features

- Implements a Prologic surround decoder in a single chip.
- Wide dynamic range
- All modes can be controlled from control data transmitted serially over four lines: CLOCK, DATA, ENABLE, and ENABLE2. This function is compatible with the LV1016 and the LA2786.

Functions

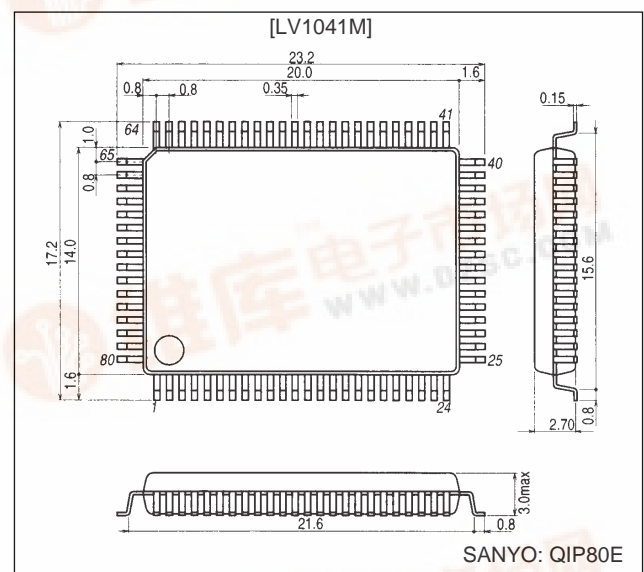
- Adaptive matrix
- Center mode control (normal, phantom, wide)
- 4/3 channel logic control
- Auto-balance (on/off)
- Prologic off mode (bypass and full bypass)
- Center trim (0 to -31 dB in 1-dB steps)
- On-chip memory: (8K SRAM)
- Variable delay time: 15, 20, 25, 30, 40, or 50 ms (15, 20, 25, or 30 ms for Dolby Prologic surround)
- New A/D and D/A converter circuits adopted
- On-chip Dolby B noise reduction
- On-chip input and output filters
- Built-in V_{DD} circuit
- Surround trim (0 to -31 dB in 1-dB steps)
- Input and output muting functions
- Master volume control for the center and surround channels (0 to -44 dB in -2-dB steps, -44 to -76 dB in -4-dB steps, and muted)

Note *: Dolby and the double D symbol are registered trademarks of the Dolby Laboratories Licensing Corporation. This IC can only be used by Dolby licensees. Licensing information and corresponding technical information is available from: Dolby Licensing Corporation
San Francisco, CA 94103-4813
USA

Package Dimensions

unit: mm

3174-QFP80E



LV1041M

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		12	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 70^\circ\text{C}$ When mounted on a $114.3 \times 76.1 \times 1.6$ mm fiberglass epoxy printed circuit board.	1300	mW
Operating temperature	T_{opr}		-20 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +150	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		9	V
Operating supply voltage range	$V_{CC\text{ op}}$		8 to 10	V
Input high-level voltage	V_{IH}		3.5 to 5.5	V
Input low-level voltage	V_{IL}		0 to 1.0	V
Dolby level	$V_O\text{ Dolby}$		300	mVrms

Operating Conditions

at $T_a = 25^\circ\text{C}$, $V_{CC} = 9\text{ V}$, $V_{IN} = 300\text{ mV rms}$ (left and right inputs), $0.707 \times 300\text{ mV rms}$ (center and surround inputs), $f = 1\text{ kHz}$, center trim = 0 dB, surround trim = 0 dB, delay time = 20 ms, in wide mode, and with the center and surround master volume set to 0 dB.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CC}	No signal		80	110	mA
Center channel output level	V_{OC}	C input	-2	0	+2	dB
Output level deviation	V_{OL}	L, R, Sch from Cch, matrix output	-0.5	0	+0.5	dB
Matrix rejection (L)	R_{jL}	L input		-40	-25	dB
Matrix rejection (C)	R_{jC}	C input		-40	-25	dB
Matrix rejection (R)	R_{jR}	R input		-40	-25	dB
Matrix rejection (S)	R_{jS}	S input		-40	-25	dB
Total harmonic distortion (L)	THD_L	L 24-pin output		0.02	0.09	%
Total harmonic distortion (C)	THD_C	C 31-pin output		0.02	0.09	%
Total harmonic distortion (R)	THD_R	R 21-pin output		0.02	0.09	%
Total harmonic distortion (S)	THD_{S2}	S delay 33-pin output		0.1	0.7	%
Signal-to-noise ratio (L)	SN_L	L 24-pin output, CCIR/ARM, $R_S = 10\text{ k}\Omega$		-76	-71	dB
Signal-to-noise ratio (C)	SN_C	C 31-pin output, CCIR/ARM, $R_S = 10\text{ k}\Omega$		-77	-71	dB
Signal-to-noise ratio (R)	SN_R	R 21-pin output, CCIR/ARM, $R_S = 10\text{ k}\Omega$		-76	-71	dB
Signal-to-noise ratio (S)	SN_S	S delay 33-pin output		-75	-65	dB
Signal handling (L)	SH_L	L 24-pin output, $V_{CC} = 8.5\text{ V}$, THD = 1%	15	16		dB
Signal handling (C)	SH_C	C 31-pin output, $V_{CC} = 8.5\text{ V}$, THD = 1%	15	17		dB
Signal handling (R)	SH_R	R 21-pin output, $V_{CC} = 8.5\text{ V}$, THD = 1%	15	16		dB
Signal handling (S)	SH_S	$V_{CC} = 8.5\text{ V}$, THD = 3%, output 33-pin S delay	15	16		dB
Noise sequencer output level	V_{ns}	Each matrix out	53	60	90	mV
Noise reduction frequency characteristics	Dec1	0 dB, 1 kHz	-1.5	0.0	+1.5	dB
	Dec2	-20 dB, 1 kHz	-24.0	-22.5	-21.0	dB
	Dec3	0 dB, 5 kHz	-1.5	0.0	+1.5	dB
	Dec4	-20 dB, 5 kHz	-23.3	-21.8	-20.3	dB
	Dec5	-40 dB, 5 kHz	-46.8	-45.3	-43.8	dB
[Prologic Off Mode]						
Left and right channels total harmonic distortion	THD_{OFF}	L, R, 400 to 30 kHz BPF		0.01	0.03	%
Left and right channels signal-to-noise ratio	S/N_{OFF}	L, R, CCIR/ARM		-90	-80	dB
Left and right channels signal handling	Sh_{off}	L, R, $V_{CC} = 8.5\text{ V}$, THD = 1%	15	16		dB
Master volume muting attenuation	V_{MUTE}	$V_{IN} = 1\text{ Vrms}$		-92	-80	dB

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Sample Application Circuit

LL: Low leak capacitor

