Ordering number: EN4876B

Bi-CMOS LSI

LV2105V

530 MHz PLL Frequency Synthesizer LSI

Overview

The LV2105V is a PLL frequency synthesizer Bi-CMOS LSI that provides low-voltage operation and low current drain, and that is suitable for use in a variety of radio equipment.

Functions

- PLL function
- Data input by serial transfer (CCB format)
- Input amplifier for crystal oscillation circuit
- Data output port

Features

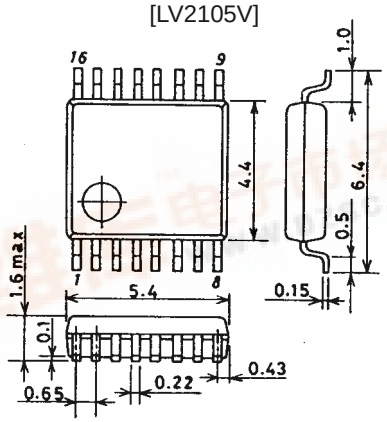
- Low operating voltage: (V_{CC} = 2.5 to 5.5 V)
- Low current drain (5.5 mA)
- Compact package (SSOP16, 0.65 mm pitch)
- VCO band switching data output port on chip
- Data can be input while in power saving mode
- Data input pin high level can be input at V_{CC} or higher
- Independent setting of CP ON/OFF (high impedance) possible

Package Dimensions

unit: mm

3178-SSOP16

[LV2105V]



SANYO : SSOP16

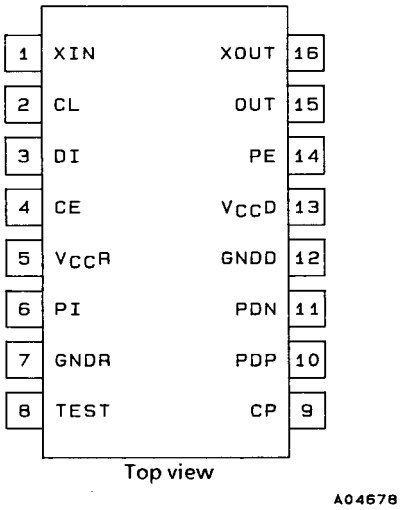
- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Specifications

Absolute Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	V_{CC}R, V_{CC}D	–0.3 to +6.0	V
Maximum input voltage	V_{IN} max(1)	CE, CL, DI	–0.3 to +6.0	V
	V_{IN} max(2)	XIN, TEST	–0.3 to V_{CC}+0.3	V
Maximum output voltage	V_{OUT} max(1)	PDP	–0.3 to +9.0	V
	V_{OUT} max(2)	PDN, OUT, PE	–0.3 to V_{CC}+0.3	V
Maximum output current	I_{OUT} max	PDP	0 to +1.0	mA
Allowable power dissipation	Pd max	114 × 76 × 1.6 mm^3 When using glass epoxy board	230	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

Pin Assignment



Allowable Operating Ranges at Ta = –40 to +85 °C

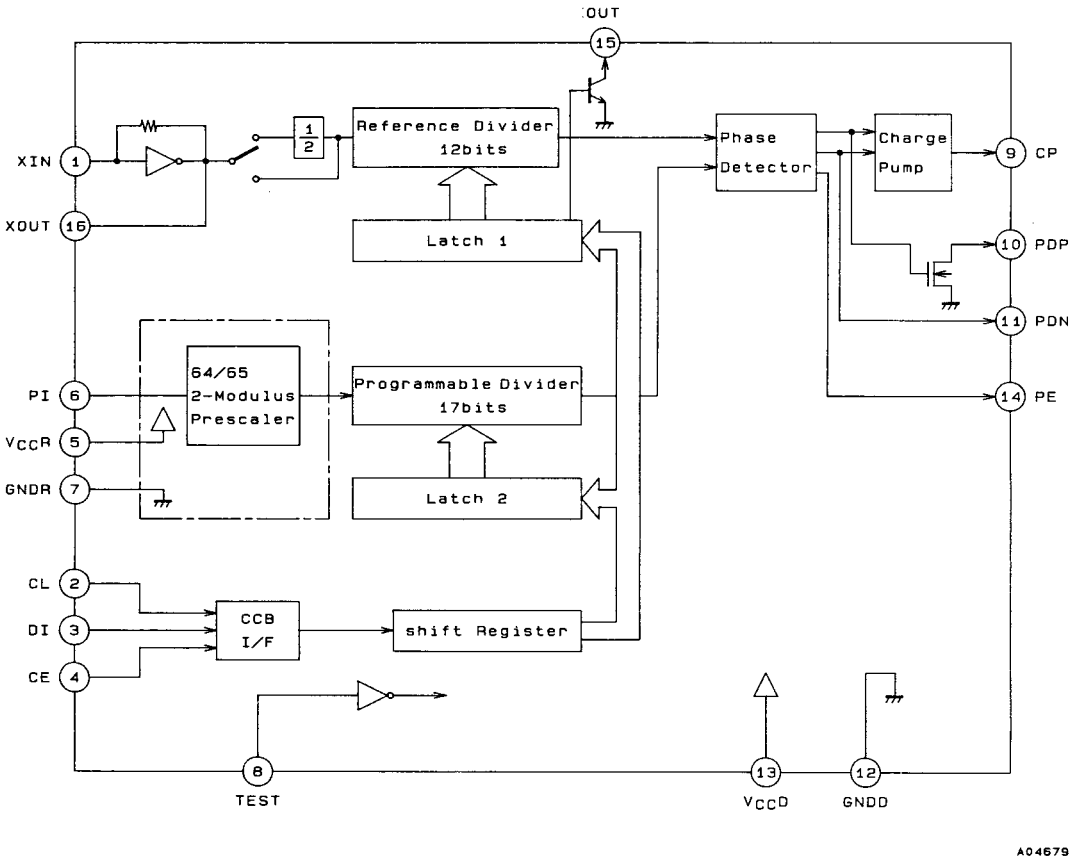
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}	$V_{CC}R$, $V_{CC}D$	2.5		5.5	V
High-level input voltage	V_{IH}	CE, CL, DI	$V_{CC}R \times 0.7$		5.5	V
Low-level input voltage	V_{IL}	CE, CL, DI	0		+0.6	V
Output voltage	V_{OUT}	PDP	0		+7.0	V
Input frequency	$f_{IN}(1)$	XIN: Sine wave capacitive coupling	5		22	MHz
	$f_{IN}(2)$	PI: Sine wave capacitive coupling	100		530	MHz
Input amplitude	$V_{IN}(1)$	XIN: Sine wave capacitive coupling	–12		+10	dBm
	$V_{IN}(2)$	PI: Sine wave capacitive coupling	–18		0	dBm
Crystal oscillation condition	Xtal	XIN, (XOUT)	5		13	MHz

Electrical Characteristics at Ta = 25 °C, $V_{CC}R$ = 3.0 V, $V_{CC}D$ = 3.0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Low-level output voltage	$V_{OL}(1)$	PDP: I_O = 0.5 mA			0.5	V
	$V_{OL}(2)$	PDN: I_O = 0.5 mA			0.5	V
	$V_{OL}(3)$	PE: I_O = 0.5 mA			0.5	V
	$V_{OL}(4)$	OUT: I_O = 2.0 mA			0.5	V
High-level output voltage	$V_{OH}(1)$	PE: I_O = –0.5 mA	V_{CC} –0.5			V
	$V_{OH}(2)$	PDN: I_O = –0.5 mA	V_{CC} –0.5			V
Output off leak current	$I_{OFF}(1)$	PDP: V_O = 3.0 V			1.0	µA
	$I_{OFF}(2)$	CP: V_O = 1.5 V			100	nA
C.P output current	I_{CP}	CP: V_O = 1.5 V	±4.0	±7.5	±11	mA
High-level input current	$I_H(1)$	CE, CL, DI: V_I = 3.0 V			5.0	µA
	$I_H(2)$	XIN: V_I = 3.0 V	2.3	3.0	4.3	µA
	$I_H(3)$	TEST: V_I = 3.0 V			5.0	µA
Low-level input current	$I_L(1)$	CE, CL, DI: V_I = 0 V			5.0	µA
	$I_L(2)$	XIN: V_I = 0 V	2.3	3.0	4.3	µA
	$I_L(3)$	TEST: V_I = 0 V			5.0	µA
Internal feedback resistance	Rf	XIN		1.0		MΩ
Supply current	$I_{CC}(1)$	$V_{CC}R$, $V_{CC}D$: *1		5.5	9.0	mA
PS supply current	$I_{CC}(2)$	$V_{CC}R$, $V_{CC}D$: *1		0.4	0.6	mA

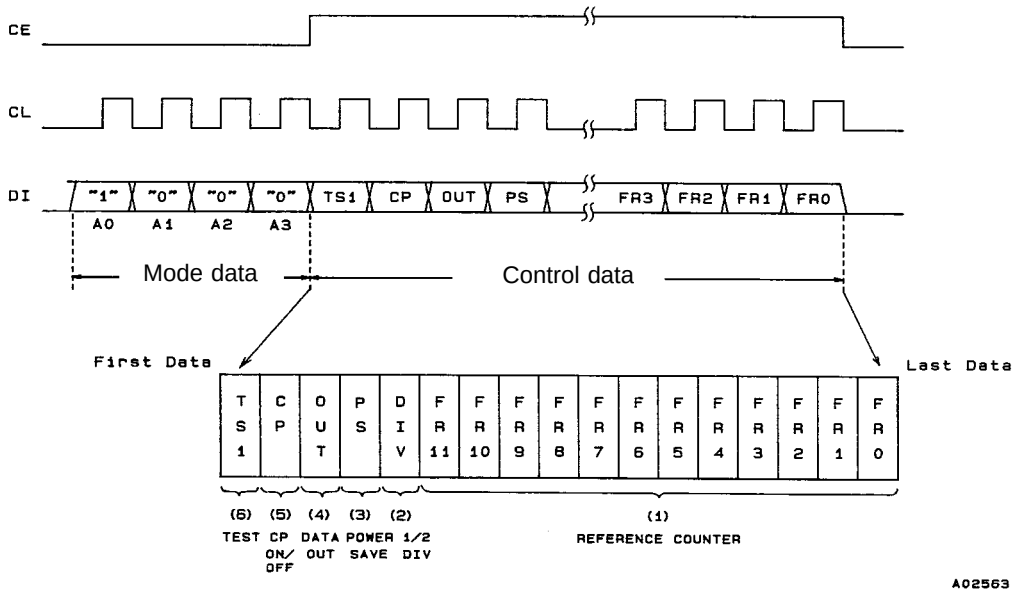
*1: XIN = 12.8 MHz, 10 dBm, PI = 400 MHz, 0 dBm, other input pins = 0 V, output, I/O pins = OPEN CP OFF

Equivalent Circuit Block Diagram

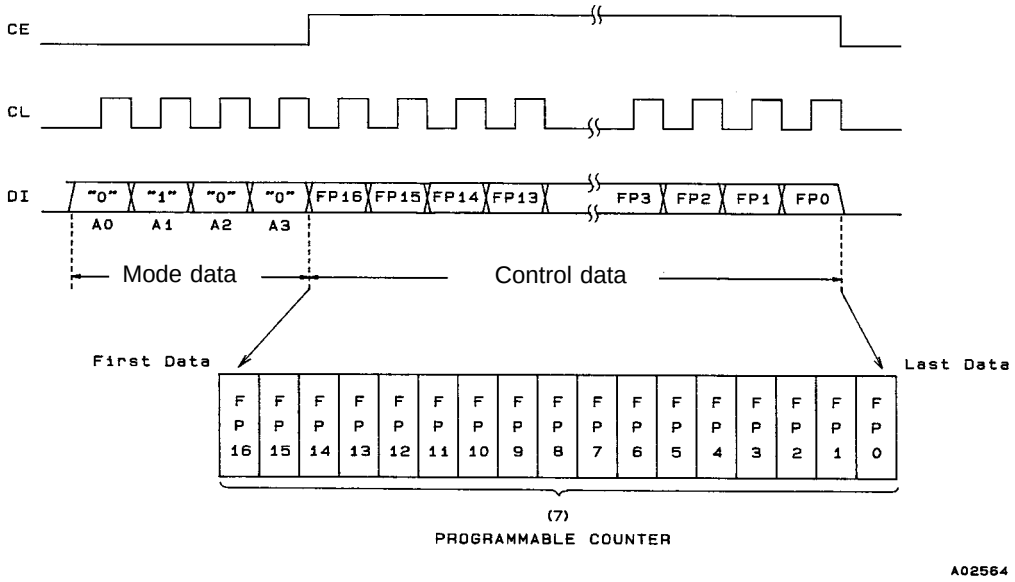


Serial Data (PLL Control Data) Configuration

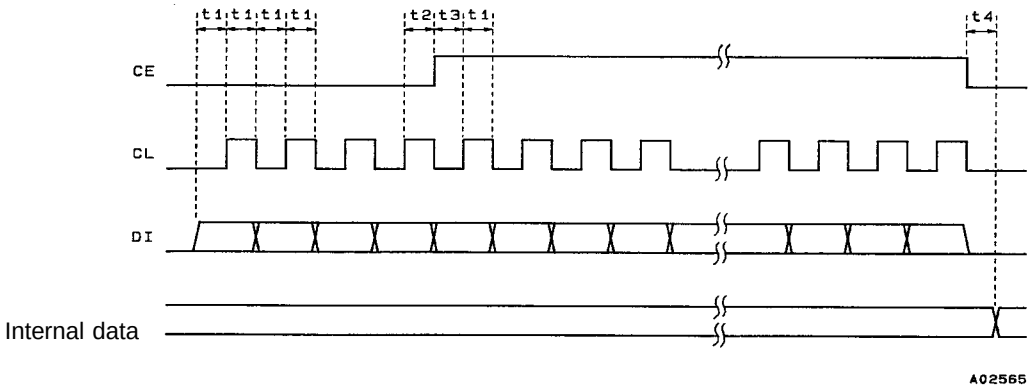
1) Mode 1: Latch-1 data (Reference divider, other data)



2) Mode 2: Latch-2 data (Programmable divider data)



Serial Data (Transfer) Timing



$t1 \geqq 1.0\mu s$
$t2 \geqq 1.0\mu s$
$t3 \geqq 1.0\mu s$
$t4 < 1.0\mu s$

Serial Data Explanation

Pin No.	Control block/data	Internal block
(1)	Reference frequency data FR0 to FR1	▪ Data that sets the division ratio of the reference divider. Binary value with FR0 as the LSB. However, the settable division ratio factor is up to 4095. (Actual division ratio) = (Set division ratio) (×2: when DIV is "1")
(2)	1/2 divider data DIV	▪ Data that sets whether to use 1/2 DIV or to enter the through state. DIV data: 0 — Through; 1 — 1/2 DIV

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<table>
<tr><th>Pin No.</th><th>Control block/data</th><th>Internal block</th></tr>
<tr><td>(3)</td><td>Power save data
PS</td><td>▪ Data that sets the power save mode on or off
<table><tr><th>PS data</th><th>Item</th></tr><tr><td>0</td><td>Power save mode</td></tr><tr><td>1</td><td>Normal operation</td></tr></table></td></tr>
<tr><td>(4)</td><td>Output port data
OUT</td><td>▪ Data that sets the output of the output port
<table><tr><th>OUT data</th><th>OUT Pin</th></tr><tr><td>0</td><td>Low</td></tr><tr><td>1</td><td>High</td></tr></table></td></tr>
<tr><td>(5)</td><td>Charge pump ON/OFF data
CP</td><td>▪ Data that sets whether to operate the charge pump or to implement high impedance.
<table><tr><th>CP data</th><th>Item</th></tr><tr><td>0</td><td>High impedance</td></tr><tr><td>1</td><td>Normal operation</td></tr></table></td></tr>
<tr><td>(6)</td><td>LSI test data TS1</td><td>▪ LSI test mode switch.
Set TS1 = 0. Normally, the TEST pin is connected to GND.</td></tr>
<tr><td>(7)</td><td>Programmable divider data
FP0 to FP16</td><td>▪ Data that sets the division ratio of the programmable divider.
Binary value with FP0 as the LSB. However, the settable division ratio factor is up to 131071.</td></tr>
</table>

Pin Functions

	Pin Name	Pin Function	I/O Style
1	XIN	Reference signal input pin (Xtal oscillation pin)	CMOS input
2	CL	Data input pin	CMOS, No pull-down
3	DI	Data input pin	CMOS, No pull-down
4	CE	Data input pin	CMOS, No pull-down
5	$V_{CC}R$	ECL block power supply pin	
6	PI	Comparison signal input pin	BIP input
7	GND R	ECL block GND pin	
8	TEST	LSI test pin. Must be connected to GND.	CMOS, No pull-down
9	CP	Built-in charge pump output pin	BIP
10	PDP	Phase comparator output for an external charge pump. If not to be used, connect to GND.	CMOS, Nch open-drain output
11	PDN	Phase comparator output for an external charge pump.	CMOS output
12	GND D	GND pin for circuits except the ECL block	
13	$V_{CC}D$	Power supply pin for circuits except the ECL block	
14	PE	Phase error output pin for phase comparator	CMOS output
15	OUT	Output port pin for switching external SW.	BIP NPN open-collector output
16	XOUT	Output pin for Xtal oscillation	CMOS output

Sample Application Circuit