

SL74LV573

OCTAL D-TYPE TRANSPARENT LATCH (3-State)

By pinning SL74LV573 are compatible with SL74HC573 and SL74HCT573 series. Input voltage levels are compatible with standard CMOS levels.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL ICs
- Voltage supply range from 1.2 to 5.5 V
- LOW input current: 1.0 μA ; 0.1 μA at $\text{V}_\text{O} = 25^\circ\text{C}$
- Output current 8 mA
- Latch current: not less than 150 mA at $\text{V}_\text{O} = 125^\circ\text{C}$
- ESD acceptable value: not less than 2000 V as per HBM and not less than 200 V as per MM



FUNCTION TABLE

Inputs			Outputs
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

H - HIGH voltage level
 L - LOW voltage level
 X - don't care
 Z - High impedance state

PIN ASSIGNMENT

OE	1	20	V _{CC}
D0	2	19	Q0
D1	3	18	Q1
D2	4	17	Q2
D3	5	16	Q3
D4	6	15	Q4
D5	7	14	Q5
D6	8	13	Q6
D7	9	12	Q7
GND	10	11	LE

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit	Conditions
V _{CC}	Supply voltage	-0.5 to +7.0	V	
I _{IK}	Input diode current	±20	mA	V _I <-0.5 V or V _I >V _{CC} +0.5 V
I _{OK}	Output diode current	±50	mA	V _O <-0.5 V or V _I >V _{CC} +0.5 V
I _O	Output current bus drivers	±35	mA	-0.5 V<V _O <V _{CC} +0.5 V
I _{CC}	DC V _{CC} or GND current for types bus driver outputs	±70	mA	
I _{GND}	GND current	±50	mA	
T _{stg}	Storage temperature range	-65 to +150	°C	
P _D	Power dissipation per package: DIP SO	750 500	mW	

Notes:

Power dissipation value decreases for:
 DIP - 12 mW/°C the range from 70 to 125°C
 SO - 8 mW/°C the range from 70 to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	Conditions
V _{CC}	Supply voltage	1.0	5.5	V	
V _I	Input voltage	0	V _{CC}	V	
V _O	Output voltage	0	V _{CC}	V	
T	Operating temperature range	-40	+125	°C	
t _r , t _f	Input rise and fall times		500 200 100 50	ns/V	V _{CC} = 1.0 ÷ 2.0 V V _{CC} = 2.0 ÷ 2.7 V V _{CC} = 2.7 ÷ 3.6 V V _{CC} = 3.6 ÷ 5.5 V

Note - The IC function down to V_{IL} = 1.0 V (input levels - V_{IL}=0 V, V_{IH}=V_{CC}); DC characteristics are guaranteed at V_{CC}=1.2 ÷ 5.5 V.

DC CHARACTERISTICS

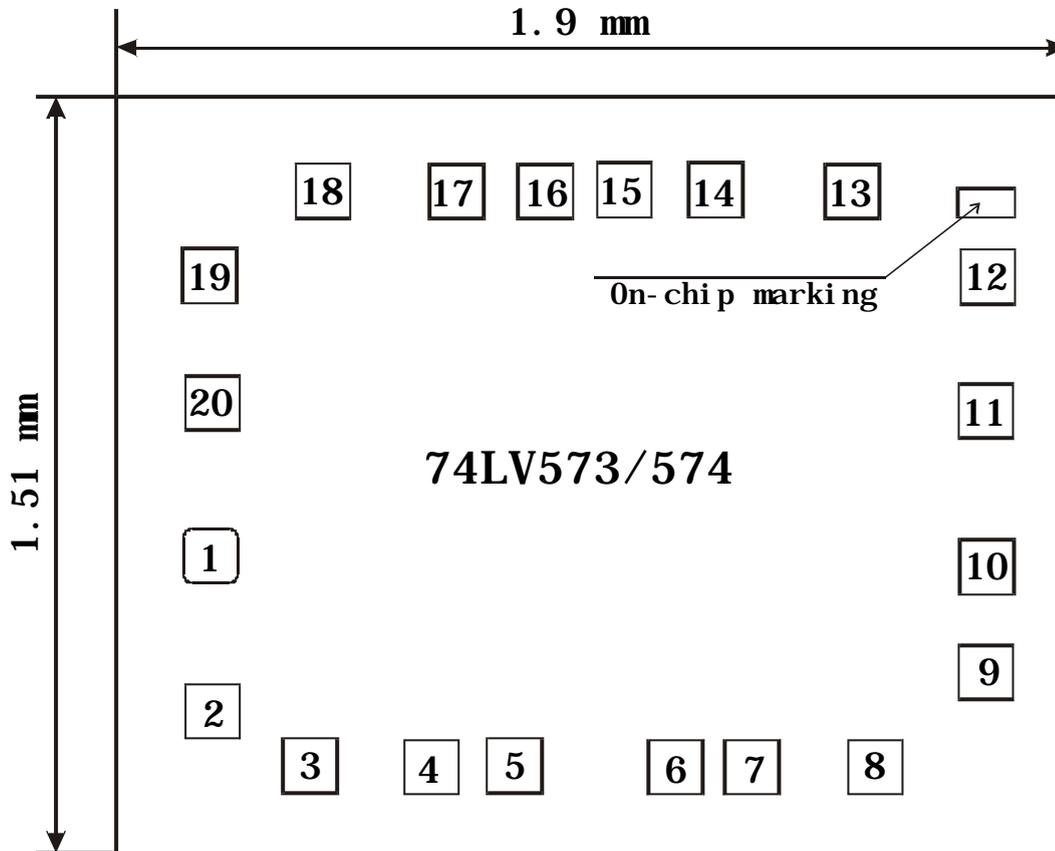
Sym bol	Parameter	Conditions			Limits						Unit
		V _{cc} (V)	V _I		-40 to +25°C		+85 °C		+125 °C		
					Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH level input voltage	1.2 2.0 2.7 to 3.6 4.5 to 5.5			0.9 1.4 2.0 0.7 V _{cc}	- - - -	0.9 1.4 2.0 0.7 V _{cc}	- - - -	0.9 1.4 2.0 0.7 V _{cc}	- - - --	V
V _{IL}	LOW level output voltage	1.2 2.0 2.7 to 3.6 4.5 to 5.5			- - - -	0.3 0.6 0.8 0.3 V _{cc}	- - - -	0.3 0.6 0.8 0.3 V _{cc}	- - - -	0.3 0.6 0.8 0.3 V _{cc}	V
V _{OH}	HIGH level output voltage	1.2 2.0 2.7 3.6 5.5	V _{IH} or V _{IL}	I _o =-100 μA	1.05 1.85 2.55 3.45 5.35	- - - - -	1.0 1.8 2.5 3.4 5.3	- - - - -	1.0 1.8 2.5 3.4 5.3	- - - - -	V
V _{OH}	HIGH level output voltage; BUS driver outputs	3.0 4.5	V _{IH} or V _{IL}	I _o =-8 mA I _o =-16 mA	2.48 3.70	- -	2.40 3.60	- -	2.20 3.50	- -	V
V _{OL}	LOW level output voltage	1.2 2.0 2.7 3.6 5.5	V _{IH} or V _{IL}	I _o =100 μA	- - - - -	0.15 0.15 0.15 0.15 0.15	- - - - -	0.2 0.2 0.2 0.2 0.2	- - - - -	0.2 0.2 0.2 0.2 0.2	V
V _{OL}	LOW level voltage; BUS driver outputs	3.0 4.5	V _{IH} or V _{IL}	I _o =8 mA I _o =16 mA	- -	0.33 0.40	- -	0.40 0.55	- -	0.50 0.65	V
I _I	Input leakage current	5.5	V _{IH} or GND		-	±1.0		±1.0	-	±1.0	μA
I _{OZ}	OFF-state current	5.5	V _{IH} or V _{IL}		-	±0.5		±5.0	-	±10.0	μA
I _{CC}	Supply current	5.5	V _{IH} or GND	I _o = 0		8.0		80		160	μA
I _{CC}	Additional supply current per input	2.7 to 3.6	V _I = V _{cc} -0.6V		-	0.2		0.5	-	0.85	mA

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AC CHARACTERISTICS (C_L=50 pF, R_L=1 KΩ, t_{LH} = t_{HL} = 2.5 ns)

Sym bol	Parameter	Conditions		Limits						Unit
		Vcc		-40 to +25° C		+85° C		+125° C		
				Min	Max	Min	Max	Min	Max	
t _{PHL/PLH}	Propagation delay Dn to Qn	1.2	V _I = Vcc or GND	-	150	-	160	-	170	ns
		2.0		-	30	-	39	-	49	
		2.7		-	23	-	29	-	36	
		3.0		-	18	-	23	-	29	
		4.5		-	15	-	19	-	24	
t _{PHL/PLH}	Propagation delay LE to Qn	1.2	V _I = Vcc or GND	-	160	-	180	-	190	ns
		2.0		-	34	-	43	-	53	
		2.7		-	28	-	31	-	34	
		3.0		-	20	-	25	-	31	
		4.5		-	17	-	21	-	26	
t _{PZH/PZL}	3-state output enable time OE to Qn	1.2	V _I = Vcc or GND	-	140	-	160	-	170	ns
		2.0		-	28	-	37	-	48	
		2.7		-	22	-	28	-	35	
		3.0		-	17	-	22	-	28	
		4.5		-	14	-	18	-	23	
t _{PHZ/PLZ}	3-state output disable time OE to Qn	1.2	V _I = Vcc or GND	-	160	-	160	-	170	ns
		2.0		-	31	-	39	-	48	
		2.7		-	23	-	29	-	36	
		3.0		-	20	-	24	-	29	
		4.5		-	17	-	20	-	24	
t _w	LE pulse width HIGH	1.2		100	-	125	-	150	-	ns
		2.0		29	-	34	-	41	-	
		2.7		21	-	25	-	30	-	
		3.0		17	-	20	-	24	-	
		4.5		15	-	18	-	21	-	
t _{su}	Setup time Dn to LE	1.2		50	-	75	-	100	-	ns
		2.0		15	-	17	-	20	-	
		2.7		11	-	13	-	15	-	
		3.0		8	-	10	-	12	-	
		4.5		6	-	8	-	10	-	
t _h	Hold time Dn to LE	1.2		40	-	40	-	40	-	ns
		2.0		8	-	8	-	8	-	
		2.7		8	-	8	-	8	-	
		3.0		8	-	8	-	8	-	
		4.5		8	-	8	-	8	-	
C _I	Input capacitance	5.0	0 to +25 °C		7.0				-	ns
C _{PD}	Power dissipation capacitance per package	5.5	0 to +25 °C V _I = Vcc or GND		52				-	ns





Drawing of the chip

Pads allocation Table

Pad number	coordinates (counted from lower left corner), mm		Pad size, mm
	X	Y	
01	0.128	0.545	0.108 x 0.108
02	0.128	0.229	0.108 x 0.108
03	0.330	0.120	0.108 x 0.108
04	0.576	0.120	0.108 x 0.108
05	0.738	0.120	0.108 x 0.108
06	1.054	0.120	0.108 x 0.108
07	1.216	0.120	0.108 x 0.108
08	1.466	0.120	0.108 x 0.108
09	1.682	0.314	0.108 x 0.108
10	1.682	0.533	0.108 x 0.108
11	1.682	0.839	0.108 x 0.108
12	1.682	1.108	0.108 x 0.108
13	1.422	1.274	0.108 x 0.108
14	1.149	1.274	0.108 x 0.108
15	0.971	1.274	0.108 x 0.108
16	0.811	1.274	0.108 x 0.108
17	0.633	1.274	0.108 x 0.108

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18	0.360	1.274	0.108 x 0.108
19	0.128	1.108	0.108 x 0.108
20	0.128	0.854	0.108 x 0.108