DATA SHEET

MAY 1996
REVISION 0.0

LXT325

T1/E1 Integrated Quad Receiver

General Description

The LXT325 quad receiver is a fully-integrated, quadruple-PCM receiver for both 1.544 Mbps, and 2.048 Mbps applications. It incorporates four independent receivers in a single 28-pin DIP or PLCC, or a 44-pin QFP. Each LXT325 receiver also incorporates a Loss Of Signal (LOS) detection circuit and output driver. The operating frequency is pin selectable.

These receivers perform data and timing recovery, and use peak detection and a variable threshold to reduce impulsive noise. Receiver sensitivity down to 500 mV allows for up to 13.6 dB of attenuation.

The LXT325 quad receiver is an advanced, double-poly, double-metal CMOS device and requires only a single 5-volt power supply.

Applications

- High-density T1/E1 line cards
- M13, E13 line interfaces
- Test equipment
- Line monitoring
- Receive line interface

Features

- Four independent 1.544/2.048 Mbps receivers
- Loss Of Signal (LOS) output for each receiver
- Circuit functions include data and clock recovery
- Single Master Clock input
- Meets or exceeds AT&T PUB 62411 ITU-T G.703 and ITU G.823 requirements for jitter tolerance
- Unipolar RPOS and RNEG outputs
- Minimum receive signal of 500 mV
- Selectable slicer levels (DSX-1/E1) to provide improved SNR
- CMOS technology requires only single 5 V power input
- Available in 28-pin plastic DIP and PLCC and 44-pin QFP packages
- -40 °C to 85 °C operating temperature range

LXT325 Block Diagram

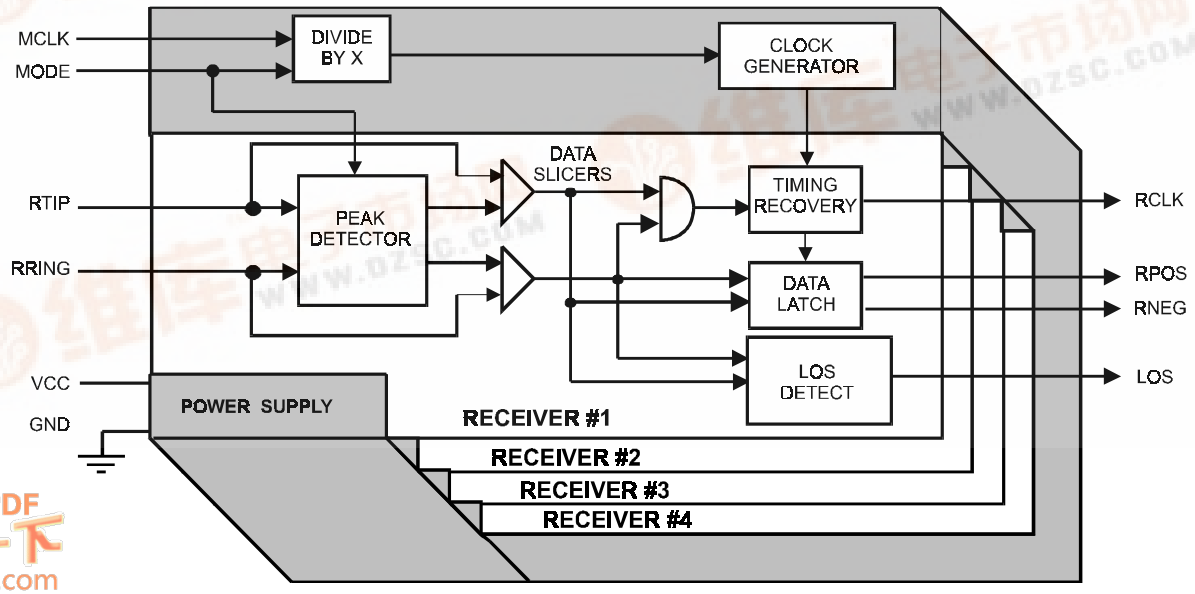

Figure 1: LXT325 Pin Assignments

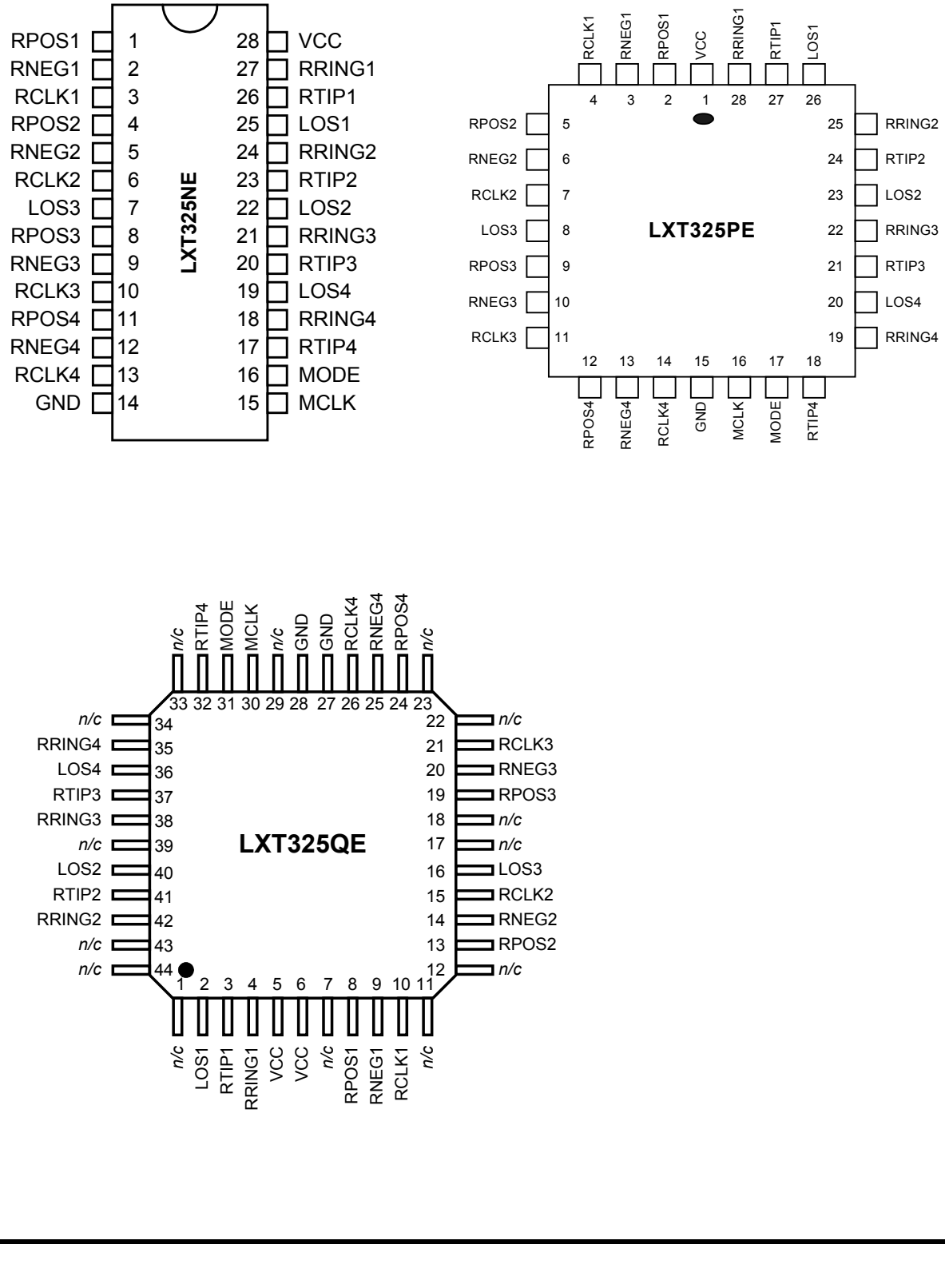

Table 1: Pin Assignments and Descriptions

Pin #			Symbol	I/O[2]	Description
DIP	PLCC	QFP[1]			
1 2	2 3	8 9	RPOS1 RNEG1	DO	**Receiver 1 Positive and Negative Data outputs**. A signal on RNEG*x* corresponds to receipt of a negative pulse on RTIP*x* and RRING*x*. A signal on RPOS*x* corresponds to receipt of a positive pulse on RTIP*x* and RRING*x*. RNEG*x* and RPOS*x* outputs are Non-Return-to-Zero (NRZ) signals. Both outputs are stable and valid on the rising edge of RCLK*x*.
3	4	10	RCLK1	DO	**Receiver 1 Recovered Clock**. Clock recovered from the inputs to RTIP1 and RRING1. See RPOS1/RNEG1.
4 5 6	5 6 7	13 14 15	RPOS2 RNEG2 RCLK2	DO	**Receiver 2 Data and Clock outputs.** Signals recovered from the inputs to RTIP2 and RRING2. See RPOS1/RNEG1/RCLK1.
7	8	16	LOS3	DO	**Receiver 3 Loss of Signal Detector**. LOS*x* pins go high when the associated receiver detects 175 consecutive spaces. The LOS output returns low when a mark is received.
8 9 10	9 10 11	19 20 21	RPOS3 RNEG3 RCLK3	DO	**Receiver 3 Data and Clock outputs.** Signals recovered from the inputs to RTIP3 and RRING3. See RPOS1/RNEG1/RCLK1.
11 12 13	12 13 14	24 25 26	RPOS4 RNEG4 RCLK4	DO	**Receiver 4 Data and Clock outputs**. Signals recovered from the inputs to RTIP4 and RRING4. See RPOS1/RNEG1/RCLK1.
14	15	27 28	GND	–	**Ground.**
15	16	30	MCLK	DI	**Master Clock**. A 1.544 MHz or 2.048 MHz clock input used to generate internal clocks. Upon loss of signal, MCLK serves as the source for all the RCLK*x* signals.
16	17	31	MODE	DI	**Mode Selection**. Set MODE high for 50% slicer level. This setting is mandatory for 2.048 Mbit/s operation and provides maximum sensitivity in 1.544 Mbit/s designs. Where undershoot will exceed 45% in 1.544 MHz applications, pull MODE low to set the slicer levels to 70%.
17 18	18 19	32 35	RTIP4 RRING4	AI	**Receiver 4 Tip and Ring**. The AMI signal received from the 4th twisted-pair line is applied at these pins. A center-tapped, center-grounded transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS*x*/RNEG*x*, and RCLK*x* pins.
19	20	36	LOS4	DO	**Receiver 4 Loss of Signal Detector**. See LOS3.
20 21	21 22	37 38	RTIP3 RRING3	AI	**Receiver 3 Tip and Ring Inputs**. See RTIP4/RRING4.
22	23	40	LOS2	DO	**Receiver 2 Loss of Signal detector**. See LOS3.

1. Pins 1, 7, 11, 12, 17, 18, 22, 23, 29, 33, 34, 39, 43 and 44 have no function in the 44-pin QFP package. All applications should leave them unconnected.
2. Entries in the I/O column are DI = Digital Input; DO = Digital Output; AI = Analog Input.

Table 1: Pin Assignments and Descriptions – continued

Pin #			Symbol	I/O[2]	Description
DIP	PLCC	QFP[1]			
23 24	24 25	41 42	RTIP2 RRING2	AI	**Receiver 2 Tip and Ring Inputs**. See RTIP4/RRING4.
25	26	2	LOS1	DO	**Receiver 1 Loss of Signal Detector**. See LOS3.
26 27	27 28	3 4	RTIP1 RRING1	AI	**Receiver 1 Tip and Ring Inputs**. See RTIP4/RRING4.
28	1	5,6	VCC	–	+5 VDC Power Supply

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2. Entries in the I/O column are DI = Digital Input; DO = Digital Output; AI = Analog Input.

FUNCTIONAL DESCRIPTION

The LXT325 quad receiver is a fully-integrated, PCM receiver for both 1.544 Mbit/s (DSX-1) and 2.048 Mbit/s (E1) applications. The MCLK frequency and the MODE pin input level set the mode of operation. The LXT325 is a low-power CMOS device operating from a single +5 V power supply.

The figure at the front of the Data Sheet shows a simplified block diagram of the LXT325. The input signal is received from the twisted-pair line on each side of a center-grounded transformer. (Positive pulses are received at RTIP and negative pulses are received at RRING.) This differential signal is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio.

For E1 applications the threshold is set to 50% of the peak value (MODE set High). In 1.544 Mbit/s applications where undershoot does not exceed 45%, MODE may be set High (50% of the peak value) for the maximum sensitivity and noise margin. In applications where the undershoot exceeds 45% the MODE must be set Low. With MODE Low, the slicer threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 consecutive zeros over the range of specified operating conditions.

The slicer threshold is maintained through a capacitive storage arrangement and a combination of Refresh and Bleed-off circuitry. This design balance prevents the refresh circuitry from driving the threshold too high, while ensuring that it is maintained over long strings of successive zeros.

These receivers are capable of accurately recovering signals with up to 13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of 500 mV. Maximum cable length is 1500 feet of ABAM cable (approximately 6 dB), with the additional attenuation being resistive flat loss. Regardless of received signal level, the peak detectors are held above a minimum level of 150 mV to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections. Recovered clock signals are supplied to the data latch. The recovered data is synchronized with the recovered clock (RCLK), then output at RNEG and RPOS. RPOS and RNEG outputs are valid on the rising edge of RCLK.

LINE INTERFACE

The LXT325 quad receiver interfaces with four twisted-pair lines (one twisted-pair for each receiver) through standard pulse transformers and appropriate resistors. Recommended transformer characteristics are listed in Table 2.

Table 2: Recommended Transformer Characteristics

Parameter		1:1:1	1:2:2	Unit
DC Resistance	Primary	1.0 Maximum	1.0 Maximum	Ω
	Secondary	1.0 Maximum	1.0 Maximum	Ω
Primary inductance (Line Side)		1.2 typical	0.5 Maximum	mH
Leakage inductance		0.5 Maximum	1.0 Maximum	µH
Interwinding capacitance		25 Maximum	40 Maximum	pF

APPLICATION INFORMATION

The LXT325 quad receiver is compatible with both DSX-1 and E1 systems. Low, +5 V only, power consumption simplifies design considerations where multiple receivers are required. The LXT325 is well-suited for use in both line interface equipment and monitor applications. The primary difference in circuit design between these two applications is the input transformer. The typical DSX-1 pulse seen in test equipment requires a 1:1:1 transformer at the receiver input. The attenuated pulse seen in monitor applications may require a 1:2:2 transformer to boost the input signal. Figure 2 is a typical 1.544 Mbit/s DSX-1 application. The LXT325 is shown tapped into the cross connect frame with 800 Ω resistors across each leg of the center-tapped, center-grounded, 1:2:2 step-up transformer.

Figure 2: Typical T1 Test/Monitor Equipment Application

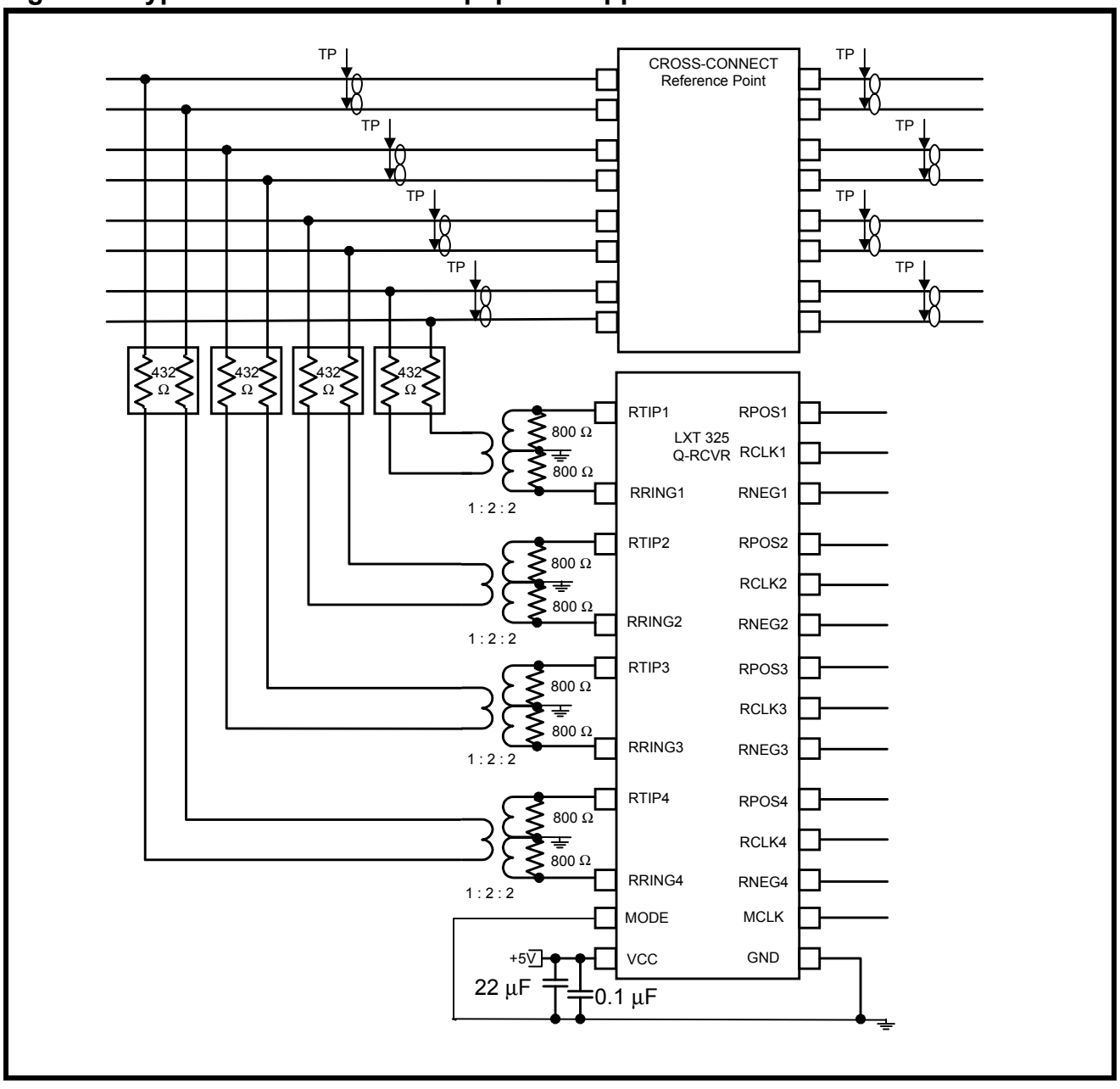
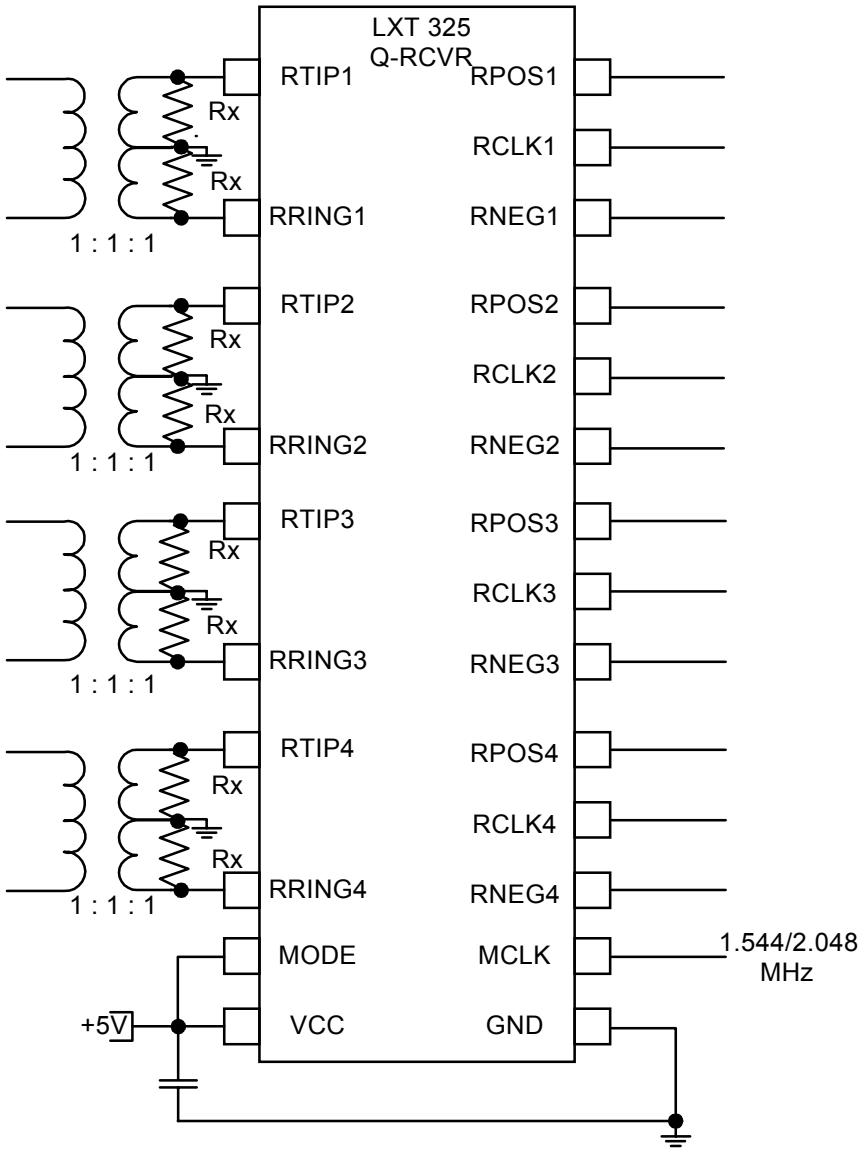


Figure 3: Typical DSX-1/E1 Receiver Application



NOTES:
Rx = 200 Ω for DSX-1 (100 Ω, TP, T1) applications
Rx = 240 Ω for E1 (120 Ω, TP, E1) applications
Rx = 150 Ω for E1 (75 Ω, coax, E1) applications

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 6 and Figures 4 represent the performance specificatons of the LXT325 and are guaranteed by test, except where noted by design.

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{CC}	-0.3 V	6 V	V
Input voltage, any I/O pin[1]	$V_{I/O}$	GND - 0.3 V	VCC + 0.3 V	V
Input current, any I/O pin[2]	$I_{I/O}$	-10	10	mA
Storage temperature	T_{ST}	-65	150	°C

CAUTION

Exceeding these values may cause permanent damage to the device. Operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Excluding RTIP and RRING which must stay within -6 V to VCC +0.3 V
2. Transient currents of up to 100 mA will not cause SCR latch-up.

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage[1]	V_{CC}	4.75	5	5.25	V
Power dissipation	P_D	1	–	1	W
Operating Temperature	T_{OP}	-40	–	85	°C

1. Voltages are with respect to ground unless otherwise stated.

Table 5: DC Electrical Characteristics[1]

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Supply current	I_{CC}	–	–	40	mA	
Input High voltage	V_{IH}	2.0	–	–	V	Digital Inputs
Input Low voltage	V_{IL}	–	–	0.8	V	Digital Inputs
Output High voltage	V_{OH}	2.4	–	–	V	I_O = 0.4 mA
Output Low voltage	V_{OL}	–	–	0.4	V	I_O = 1.6 mA
Input leakage current	I_{LL}	–	–	±10	µA	Digital inputs
Output current	I_H	–	–	1.6	mA	V_O = 0.4 V
Output rise/fall time	T_{RF}	–	–	25	ns	15 pF load

1. Clocked operation over recommended temperature and power supply ranges.

Table 6: Receiver Characteristics

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Slicer ratio	Mode=Low	SRD	63	70	77	%	
	Mode=High	SRC	43	50	57	%	
Dynamic Range		DR	0.50	–	3.6	VPEAK	
Undershoot		US	–	–	62	%	
Sensitivity below DSX (0 dB = 2.4 V)		–	13.6	–	–	dB	maximum of 6 dB cable loss, with balance being resistive loss.
		–	500	–	–	mV	
Error-Free Signal-to-Crosstalk ratio	2.048 MHz	S/X	14	–	–	dB	Single frequency interference production test guarantees error-free operation as specified in G.703, *f* 6.3.4 (Testing for 1.544 MHz systems uses a 1.544 Mbit/s QRSS interfering signal; MODE = 1.)
	1.544 MHz	S/X	12	–	–	dB	

1. Typical figures are at 25 °C and are design aids only; not guaranteed and not subject to production testing.

Figure 4: Clock Timing Diagram

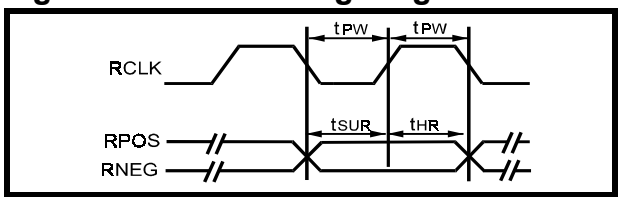


Table 7: Master and Receive Clock Timing Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Master Clock Frequency	DSX-1	MCLK	–	1.544	–	MHz	
	E1	MCLK	–	2.048	–	MHz	
Master Clock Tolerance		MCLKt	–	±100	–	ppm	
Master Clock duty cycle		MCLKd	40	50	60	%	
Receive Clock duty cycle		RCLKd	40	50	60	%	
Receive Clock pulse width	1.544 Mbit/s	tPW	270	325	378	ns	
	2.048 Mbit/s	tPW	203	244	285	ns	
RPOS/RNEG to RCLK rising setup time	1.544 Mbit/s	tSUR	50	270	–	ns	
	2.048 Mbit/s	tSUR	50	203	–	ns	
RCLK rising to RPOS/RNEG hold time	1.544 Mbit/s	tHR	50	270	–	ns	
	2.048 Mbit/s	tHR	50	203	–	ns	
Rise/fall time–any digital output		TRF	–	–	25	ns	

1. Typical figures are at 25 °C and are design aids only; not guaranteed and not subject to production testing.

NOTES