DATA SHEET

APRIL 1997
Revision 3.1

LXT400

All Rate Extended Range Switched 56/DDS Transceiver

General Description

The LXT400 is an integrated line interface circuit for Switched 56 (SW 56) and Digital Data Service (DDS), compatible with any combination of 19 to 26 AWG cable. The LXT400 operates at any of 17 preset data rates from 2.4 kbps to 72.0 kbps, providing appropriate transmit pulse shaping, receive signal detection and timing recovery at the metallic interface between the carrier and the customer installation. The LXT400 offers a variety of diagnostic features including loopback, line status and equalizer monitor outputs, while conforming to AT&T, ANSI and Bellcore specifications.

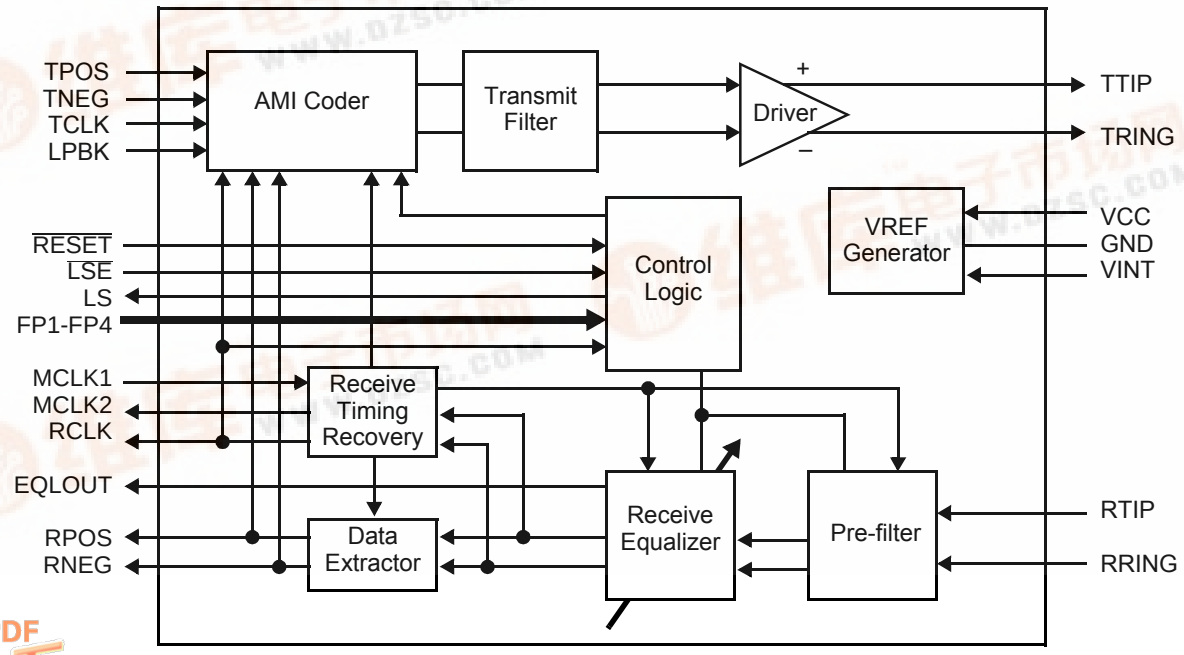
The LXT400 transmit section includes switched capacitor filters, continuous reconstruction filters, and a 50% AMI encoder. The AMI pulse is synchronized with the transmit clock.

The LXT400 receive section performs line equalization, data extraction and timing recovery. The LXT400 has a BER of less than 10^{-7} with up to 49 dB of cable attenuation at the Nyquist frequency for 56, 64 and 72 kbps, and 40 dB at the lower rates. The LXT400 is an advanced CMOS device which requires only a single +5 V power supply.

Features

- Enhancements:
  - Three new data rates: 38.4, 51.2, and 64.0 kbps
  - Improved accuracy in line attenuation reporting
  - Simplified transmit digital timing
- Integrated transmitter, receiver and timing recovery on a single CMOS chip
- Transparent to framing and coding
- Receive equalizer filters allow data recovery from signals with up to 40 dB of attenuation at the Nyquist frequency at line rates below 56 kbps, and up to 49 dB at the 56, 64 and 72 kbps line rates
- Single 4.096 MHz crystal or master clock input
- Digital back-end loopback
- Equalizer output monitor pin
- Line status (loop length, RLOS, etc.) information available for maintenance purposes
- Low power consumption (200 mW typical)
- Available in 28-pin plastic DIP and PLCC
- Single 5 V only CMOS technology

LXT400 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT400 Pin Assignments

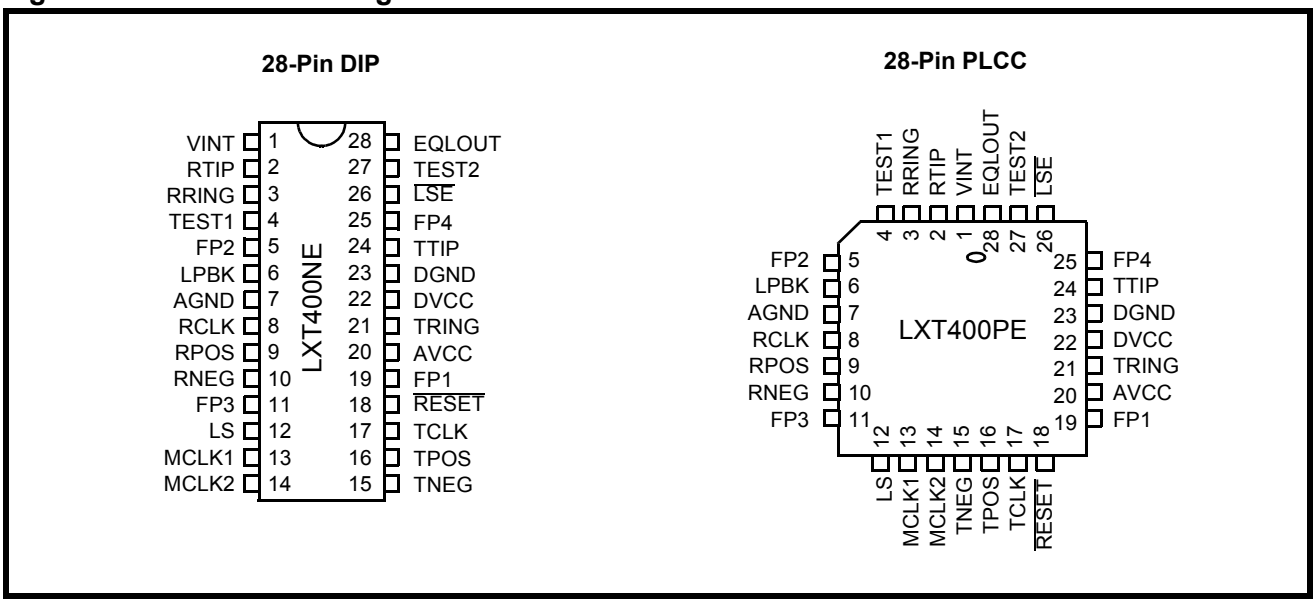


Table 1: LXT400 Signal Descriptions

Pin #	Sym	I/O	Description
1	VINT	I	**Intermediate Voltage Reference.** Reference voltage used for internal analog circuits. This pin must be connected through a 1kΩ resistor (Rv) to the center node between the two termination resistors, Rr, as shown in Figure 8 and 9.
2 3	RTIP RRING	I	**Receive Tip** and **Receive Ring.** Receive data input pair. RTIP and RRING are a fully differential input for the receive line interface.
4	TEST1	I	**Test 1.** Factory Test Pin. *Do not connect.*
19 5 11 25	FP1 FP2 FP3 FP4	I I I I	**Frequency Programming Inputs 1 through 4.** The LXT400 data rate is set by the logic levels present at the FP1 through FP4 inputs as shown in Table 2. For operation at 38.4, 51.2, and 64.0 kbps, the RCLK output must be applied to the FP3 input.
6	LPBK	I	**Loopback.** When set High, activates digital back-end loopback.
7	AGND	-	**IC Ground.** Ground for all IC circuitry except the transmit driver.
8	RCLK	O	**Recovered Clock.** Clock recovered from signal input at RTIP and RRING, based on the data rate setting on the FP1 - FP4 inputs.
9 10	RPOS RNEG	O O	**Receive Data Positive** and **Negative.** Receive data outputs. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. A signal on RNEG corresponds to a negative pulse on RTIP and RRING. Both outputs transition on the rising edges of RCLK, and are never High simultaneously.

Table 1: LXT400 Signal Descriptions – continued

Pin #	Sym	I/O	Description
12	LS	O	**Line Status Output.** A 16-bit serial word indicating activation state, line loss, and loss of signal (LOS). LS transitions occur on falling edges of RCLK. LS goes to a high impedance state when $\overline{\text{LSE}}$ is High. If $\overline{\text{LSE}}$ is tied Low, the LS output represents LOS only.
13 14	MCLK1 MCLK2	I O	**Master Clock 1** and **Master Clock 2**. The required 4.096 MHz master clock may be provided by a crystal connected across these pins, or by a digital clock connected to MCLK1. If a clock is provided on MCLK1, MCLK2 must be left unconnected.
15 16	TNEG TPOS	I I	**Transmit Data Negative** and **Positive.** These inputs are sampled on the falling edges of TCLK. AMI pulses are encoded as follows: **TPOS TNEG Transmit Signal** 0 0 Space 0 1 Negative Pulse 1 0 Positive Pulse 1 1 Space
17	TCLK	I	**Transmit Clock.** Transmit clock at the data rate set by the FP1 - FP4 inputs.
18	$\overline{\text{RESET}}$	I	**Reset**. Hardware reset pin. Must be pulsed Low on power-up to initialize all internal circuits. Must also be pulsed Low after changing the data rate setting, and after forcing or releasing any loopback condition.
20	AVCC	-	**IC Power**. Power supply for all IC circuits except the transmit driver. +5 V (±5%).
21 24	TRING TTIP	O O	**Transmit Ring** and **Transmit Tip.** Differential driver outputs. Designed to drive the 135Ω twisted-pair cable through the transmit line interface shown in application diagrams (see Figure 8 and 9).
22	DVCC	-	**Driver Power.** Transmit driver power supply. +5 V (±5%). Tie to AVCC, pin 20.
23	DGND	-	**Driver Ground**. Transmit driver ground. Tie to AGND, pin 7.
26	$\overline{\text{LSE}}$	I	**Line Status Enable.** Active Low enable for the LS serial port. This pin must transition from High to Low to read LS serial data. $\overline{\text{LSE}}$ is sampled on the rising edges of RCLK.
27	TEST2	I	**Test 2.** Analog test pin. *Must be tied to ground*.
28	EQLOUT	O	**Equalizer Output Monitor.** Monitors Equalizer. *Must be left open when not used.*

FUNCTIONAL DESCRIPTION

Introduction

The LXT400 comprises three basic sections: transmit, receive and control logic.

The transmit section includes a 50% AMI encoder, a programmable switched-capacitor low-pass filter, a low-pass notch filter, a transmit timing re-synchronizer and a continuous reconstruction filter. An on-chip CMOS driver is also incorporated to drive a 135Ω line through a transformer.

The receive section includes pre-filters and line equalizers, and the timing recovery and data extraction blocks. An internal digital phase-locked loop (DPLL) is used in conjunction with the MCLK input to synchronize the recovered clock and data.

The control logic block initializes the transceiver, selects receive filters and reports status information on the serial port. Control logic inputs FP1 through FP4 determine the data rate as specified in Table 2. The control logic executes the initialization procedure upon automatic re-synchronization or external $\overline{\text{RESET}}$. Filter selection optimizes the receive signal-to-noise ratio (SNR) by matching the filter in the equalizer section to the strength of the received signal (a function of loop length/line loss). The control logic block also reports receiver status, estimated line length (as indicated by filter selection) and a receive loss of signal (RLOS) alarm on the serial port.

Initialization

Upon power-up, or after changing the baud rate or loopback condition of the line interface, a $\overline{\text{RESET}}$ pulse is required to initialize the LXT400. On receipt of the $\overline{\text{RESET}}$ pulse, the LXT400 executes an iterative cycle of level detection and offset cancellation to select the appropriate equalizer settings for the received signal. Receiver initialization can be monitored on the serial channel. When received data has a 50% ones density, full operation is achieved within one second after $\overline{\text{RESET}}$. Under the minimum ones density condition specified in Table 3, full operation is achieved within eight seconds after $\overline{\text{RESET}}$. Correct initialization assumes the presence of an AMI-coded signal at the RTIP and RRING inputs. The LXT400 will not correctly initialize unless a stable signal which meets the network interface specifications of AT&T Pub 62310 is present at the RTIP and RRING inputs during the entire initialization process. The RPOS/RNEG outputs are not valid until full operation is achieved. During offset cancellation, the RPOS/RNEG outputs do not adhere to the AMI rule. However, once initialized (assuming that a proper baud rate is selected), RPOS and RNEG outputs are never simultaneously High.

Reset

A hardware reset is required after any of the following changes in transceiver configuration:

1. A change in Data Rate setting
2. A change in the local analog loopback configuration
3. A local change in the line upon which the transceiver is communicating (for example, configurations for changing lines in a “1 for n” redundancy scheme).

Table 2: Data Rate Programming

FP4	FP3	FP2	FP1	Data Rate[1]
Low	Low	Low	Low	2.4 kbps
Low	Low	Low	High	3.2 kbps
Low	Low	High	Low	4.8 kbps
Low	Low	High	High	6.4 kbps
Low	High	Low	Low	9.6 kbps
Low	High	Low	High	12.8 kbps
Low	High	High	Low	19.2 kbps
Low	High	High	High	25.6 kbps
High	Low	Low	Low	56.0 kbps
High	Low	Low	High	72.0 kbps
High	Low	High	Low	3.5 kbps
High	Low	High	High	7.0 kbps
High	High	Low	Low	14.0 kbps
High	High	Low	High	28 kbps
Low	RCLK[1]	Low	Low	38.4 kbps
Low	RCLK[1]	Low	High	51.2 kbps
Low	RCLK[1]	High	Low	64.0 kbps

1. These data rates are activated when RCLK output on pin 8 is applied to the FP3 input on pin 11.

Table 3: Ones Density Requirements

Data Rate (kbps)	Minimum Average Ones Density
2.4, 4.8, 9.6, 19.2, 38.4	1 / 12
3.2, 6.4, 12.8, 25.6, 51.2	1 / 16
56.0	1 / 14
64.0	1 / 16
72.0	1 / 18
3.5, 7.0, 14.0, 28.0	≈ 1 / 16

Automatic re-initialization may be triggered by changes in received signal strength as follows:

- If received signal strength increases by more than about 6 dB after full operation is achieved, automatic re-initialization occurs.
- If received signal strength decreases by more than about 4 dB, re-initialization occurs. If the decrease in received signal strength exceeds 6 dB, the LXT400 reports an LOS condition and performs an automatic re-initialization.

The time required to achieve full operation after re-initialization, is the same as required for power-on initialization (i.e., 1 second max with 50% ones density, 8 seconds under minimum ones density conditions). Re-initialization is not triggered by impulse noise events.

Transmission

TPOS and TNEG must have transitions coincident with the rising edges of TCLK. The transmit section generates a 50% AMI pulse according to the pulse encoding rules, which is synchronized with the TCLK input. In DSU applications, RCLK is typically routed back into the TCLK input. The instantaneous baud period varies with the receive DPLL phase adjustments, however, the pulse duty cycle is maintained at 50% of the nominal baud period by internal re-synchronization to TCLK. The AMI pulse is then processed through a set of frequency dependent filters.

Initial filtering at all rates is accomplished by a programmable, switched-capacitor, low-pass filter. This filter is a single-pole type with the pole set at 1.3 times the bit rate (as determined by inputs FP1 - FP4).

For data rates of 2.4, 3.2, 4.8, 6.4, 9.6 and 12.8 kbps, the filtered pulses go through an additional low-pass notch filter. The notch filter is required to protect other DDS services with specific band requirements, and provides the attenuation listed in Table 4. The additional rejection requirement is weighted within each band by "C-Message" weighting over double speech sidebands around a carrier in the middle of each band (28 kHz and 76 kHz). The C-Message weighting function is graphed in Figure 2. Depending on the data rate, the frequency template extends to different limits as shown in Table 5. (An alternate notch filter is used for data rates of 3.5 and 7.0 kbps.) The single pole, low-pass filter would maintain the frequency within ± 5%. The notch filter attenuation is added to this.

A continuous filter, common to all data rates, is the final stage. The continuous filter removes high frequency components which remain after processing by the low-pass filter stages. The pulse is then applied to the line driver for transmission onto the twisted-pair line.

Figure 2: C-Message Weighting

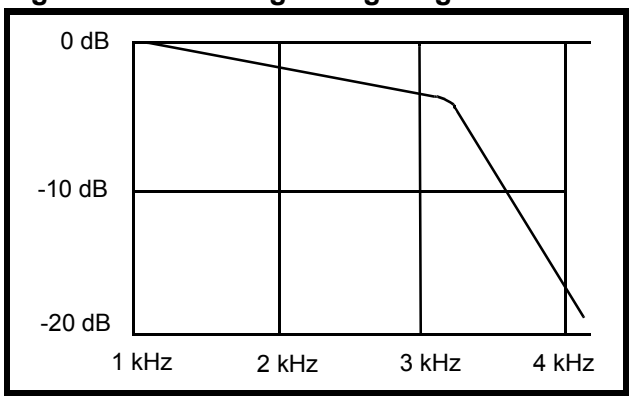


Table 4: Notch FIlter Attenuation

OCU/Loop Data Rate (kbps)	Customer (Primary Channel) Data Rate (kbps)	Rejection Band	
		22 - 32 kHz	72 - 80 kHz
2.4 or 3.2	2.4	5 dB	1 dB
4.8 or 6.4	4.8	13 dB	9 dB
9.6 or 12.8	9.6	17 dB	8 dB

Reception

RTIP and RRING inputs are differentially detected, then processed through the pre-filters and equalizer section. The continuous pre-filter removes high frequency noise and prevents aliasing problems for the switched capacitor (SC) line equalizers which follow. Pulse reshaping is achieved by the receive equalizer, which consists of an SC step equalizer and an adaptive decision feedback equalizer (DFE). The DFE eliminates residual inter-symbol interference (ISI) due to echoing by multiple bridged tap connections and the quantized frequency responses of the SC step filters. The DFE is continuously adapted to compensate for ISI due to time-varying line characteristics such as temperature, humidity and age. Nine different filter selections based on signal strength are available.

Changes in Received Signal Strength

During initialization, the LXT400 selects filters appropriate to the strength of the received signal. After initialization, the LXT400 continually monitors the receive signal strength to ensure the optimum signal/filter match. Data reception is not affected by impulsive noise events or by slow changes in signal amplitude, such as may be caused by temperature and humidity changes on the line. (The maximum constant rate of change which the LXT400 can track is 6 dB per minute.) However, instantaneous "step" changes (see Figure 3) may temporarily interfere with data reception. Step changes may be due to sudden changes in loop loss, far end transmitter output, etc.

After normal operation has been established, an instantaneous single-step change may cause one of three conditions, as shown in Figure 4.

Under Condition 1, the LXT400 automatically adapts to minor step changes in signal strength (assuming that the new input is a valid DDS signal).

Under Condition 3, the LXT400 responds to significant step changes by re-initializing.

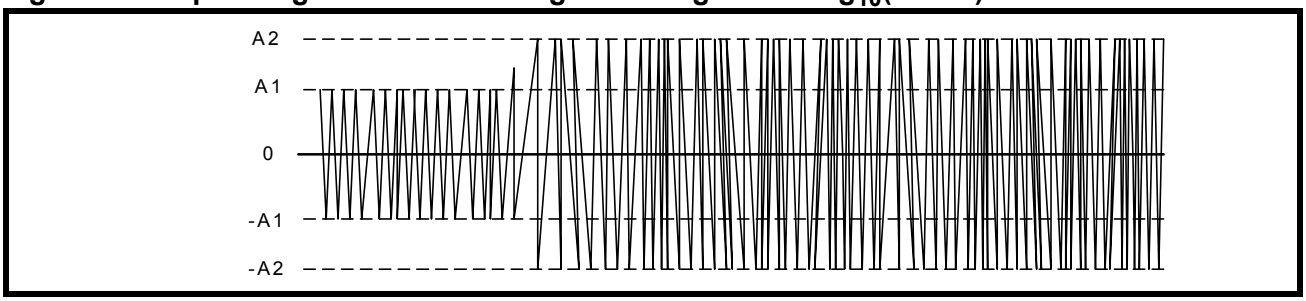
Condition 2, while unlikely to occur in an actual DDS implementation, may be observed in the laboratory due to artificial line simulators. Condition 2, which results from a 6 - 20 dB step increase in received signal strength, may result in a signal/filter mismatch. This condition is characterized by excessive bipolar violations (BPVs) which can be observed on RPOS and RNEG. External signal quality detection circuitry can be used to detect excessive BPVs that are not recognized as standard DDS BPV code words. Upon detection of unrecognized BPVs, the user may force a reset on the LXT400 to resume error-free operation.

Under normal operating conditions, step changes in received signal strength are all under local control. Thus, the user can reset the LXT400 once the new receive signal has stabilized at the chip inputs. Remote changes typically involve disconnecting one line and re-connecting another line of different length. These changes trigger the RLOS report and automatic re-initialization. Any remote changes in line length or transceiver configuration are beyond the local user's control. Remote changes in data rate are not detected.

Table 5: Frequency Limits per Data Rate

Data Rate (kbps)	Upper Frequency Limit (kHz)
2.4 (3.2)	100
4.8 (6.4)	150
9.6 (12.8)	150
19.2 (25.6)	150
38.4 (51.2)	150
56.0 (72.0)	150
64.0	150
3.5	100
7.0	150
14.0	150
28.0	150

Figure 3: Step Changes in Received Signal Strength = 20 $\log_{10}$(A2/A1) dB

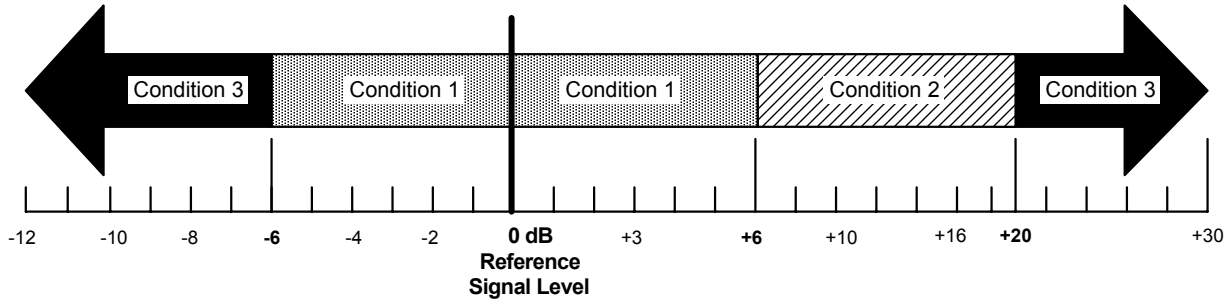


Receive Loss of Signal

RLOS goes High when more than 32 consecutive zeros are received, caused either by a true loss of signal, or a signal strength drop greater than 6 dB. The LXT400 automatically re-initializes when RLOS goes High, and 40 consecutive zeros are counted. Figure 5 shows the RTIP/RRING input and RLOS output timing relationships for a true loss of signal. When signal energy returns to the chip input, the LXT400 executes one full activation cycle in the presence of this signal. The result is that RLOS will remain High for a period of time (0.13 s < tH < 16 s) after signal energy reappears.

Figure 6 shows the RTIP/RRING input timing and RLOS output timing relationship for a signal strength decrease greater than 6 dB. In this case, RLOS will go High for a time 0.26 s < tP < 16 s.

Figure 4: Conditions Based on Changes in Received SIgnal Strength



Condition 3: > 20 dB Increase or > 6 dB Decrease.
Automatic re-initialization. No action required. If the condition is due to a signal strength decrease, the LXT400 also reports RLOS.

Condition 1: 0 - 6 dB Increase or Decrease.
Automatic compensation (may re-initialize). May pass erroneous data temporarily before resuming error-free performance. No action required.

Condition 2: 6 - 20 dB Increase.
Re-initialization not guaranteed. The device may continue to pass erroneous data until reset. RESET pulse required to ensure accurate data reception.

Figure 5: RLOS Timing for a True Loss of SIgnal

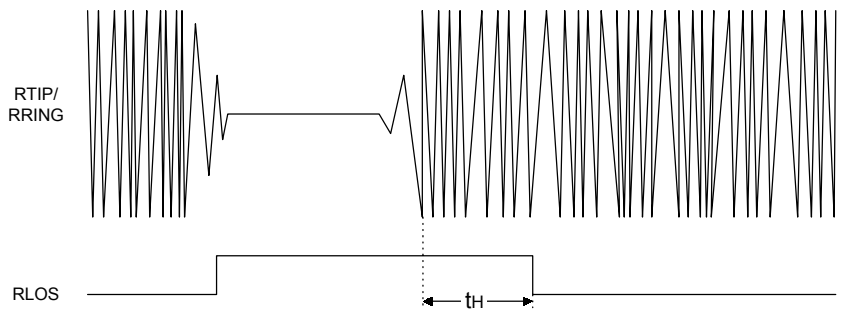
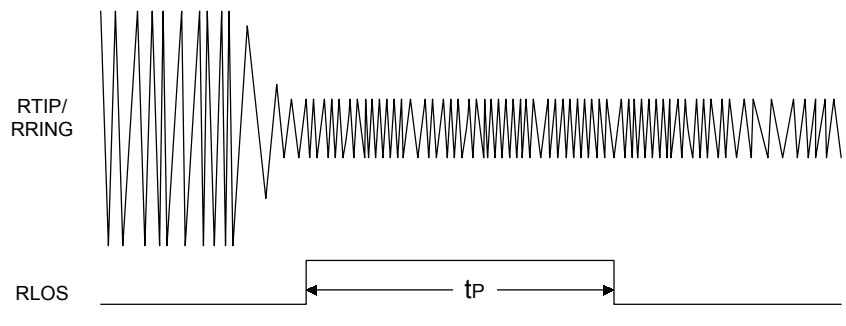


Figure 6: RLOS Timing for a Drop in Signal Strength > 6 dB



Timing Recovery

The timing recovery circuit uses a rate synchronizer to generate a high frequency internal clock from the MCLK input. A DPLL is used to synchronize this internal clock to the received data pulses. The output clock from the DPLL is divided down to generate RCLK and all other required clocks (except TCLK which is an external input).

Data Extraction

The data extraction block provides RPOS and RNEG outputs. A positive differential pulse received between RTIP and RRING results in a High on RPOS. A negative differential pulse between RTIP and RRING results in a High on RNEG. RPOS and RNEG are output at the received data rate and are valid on the falling edge of RCLK.

Receiver operation is not affected by the data patterns, provided the ones density requirements of Table 3 are met with no more than 26 consecutive zeros. RLOS is declared after 32 consecutive zeros. However, the RCLK output remains synchronized to the RTIP/RRING input for up to 40 consecutive zeros, after which re-initialization occurs. Bipolar violations are received properly. The bipolar violation coding rule that successive violations be of alternating polarity must be followed. However, if this rule is temporarily broken (due to channel noise, etc.), long term LXT400 data reception will not be adversely affected.

Loopback Operation

When the LPBK pin is set High, the recovered data and clock are sent back through the transmit section and onto the line interface, as well as being output on the RPOS/RNEG and RCLK pins. TPOS/TNEG and TCLK inputs are ignored in the loopback mode.

Serial Port Operation

The line status (LS) output is an 8-bit or 16-bit serial word enabled by pulling $\overline{\text{LSE}}$ Low for 8 or 16 bit-periods as shown in Figures 12 and 13. Refer to Test Specifications for Serial Port Timing. Bit assignments are listed in Table 6. Approximate line loss and loop length (based on received signal strength/filter selection, assuming far-end pulse transmission compliant with AT&T Pub 62310 or T1E1/90-051) are reported via bits b0 through b3 as listed in Table 7. When combined with the receive signal magnitude bits in positions b8-b15, the line attenuation may be calculated to within ±1 dB of actual value using the following equation:

$$\text{Insertion loss} = \left[\begin{array}{l}\text{Insertion loss value in}\\ \text{dB from Table 7 based}\\ \text{on LL3-LL0 value.}\end{array}\right] + 20\,\text{Log}_{10}\left(\frac{\text{3c hex}}{\text{Mag<7:0>hex}}\right);\text{dB}$$

Bits b4 through b6 indicate the receiver activation state. Bit b7 is the RLOS alarm.

Figure 7 shows the serial output for a typical LXT400 initialization sequence. Bits b0 - b3 report filter selection and bits b4 - b6 report receiver status. Bit b6 toggles to indicate that the receiver is alternating between offset cancellation (b6 - b4 = 100) and receive level detection (b6 - b4 = 000). The receiver starts with the highest-gain filter (b3 - b0 = 0111), cancels systematic voltage offset at the filter output, and then detects the receive signal level at the filter output. If the signal exceeds the threshold for that filter, the LXT400 steps down to the filter with the next-highest gain (b3 - b0 = 1000). This process is repeated until the receive signal level does not exceed the filter threshold.

Once the appropriate filter is selected, the receiver phase-locked loop (PLL) and slicer levels converge to match the receive signal for optimum SNR. During receiver convergence (b6 - b4 = 001), the PLL adapts to sample the peak of the receive pulses and the slicer level adapts to the midway point between zero and the pulse peak voltage. Once convergence is complete, the LXT400 begins full operation (b6 - b4 = 010).

Figure 7: Typical Serial Port Output for Receive Activation @ 72 kbps

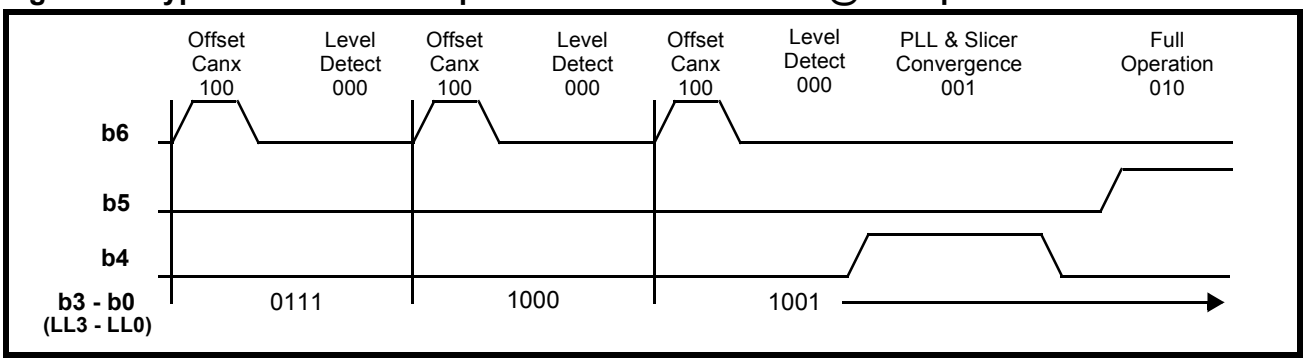


Table 6: LS Word Bit Assignments

Bit #	Name	Description	Bit #	Name	Description
b0	LL0	Loop Length Indication, bit 0	b8	MAG0	Rx signal magnitude bit 0
b1	LL1	Loop Length Indication, bit 1	b9	MAG1	Rx signal magnitude bit 1
b2	LL2	Loop Length Indication, bit 2	b10	MAG2	Rx signal magnitude bit 2
b3	LL3	Loop Length Indication, bit 3	b11	MAG3	Rx signal magnitude bit 3
b4	S1	Receiver Converging when High	b12	MAG4	Rx signal magnitude bit 4
b5	S2	Full Operation when High	b13	MAG5	Rx signal magnitude bit 5
b6	S0	Level Detection when High	b14	MAG6	Rx signal magnitude bit 6
b7	RLOS	Receive Loss of Signal when High	b15	MAG7	Rx signal magnitude bit 7

Table 7: LS Loop Length Bits LL3 - LL0

Rate kbps	Insertion Loss @ fb/2 in dB / Line Range in km (24 AWG PIC, no bridged taps) for LL3 - LL0 Values are for optimum receiver slicer level, with MAG7 - MAG0 = 3C hex								
	0111	1000	1001	1010	1011	1100	1101	1110	1111
2.4	N/A	42.3 / 23	36.0 / 19.2	30.0 / 15.3	24.2 / 11.5	20.0 / 8.6	15.5 / 5.0	10.6 / 2.4	3.4 / 0.8
3.2	N/A	42.0 / 19.9	36.0 / 16.9	30.7 / 14.3	25.2 / 11.6	20.0 / 7.8	15.0 / 4.9	10.3 / 2.4	3.0 / 0.7
4.8	N/A	42.3 / 17.3	36.3 / 14.7	30.5 / 12.0	24.7 / 9.3	18.8 / 6.7	13.5 / 4.0	9.3 / 2.0	3.1 / 0.7
6.4	N/A	42.4 / 15.4	36.5 / 13.2	31.2 / 11.0	25.6 / 8.8	20.0 / 6.6	15.0 / 4.4	10.0 / 2.2	3.3 / 0.7
9.6	N/A	40.0 / 12.5	35.0 / 10.7	29.6 / 8.9	24.2 / 7.1	18.9 / 5.4	13.8 / 3.6	9.0 / 1.8	2.5 / 0.5
12.8	N/A	42.3 / 11.7	36.2 / 10.0	30.7 / 8.3	25.0 / 6.7	19.3 / 5.0	13.8 / 3.3	8.8 / 1.7	2.6 / 0.5
19.2	N/A	42.2 / 10.0	36.2 / 8.6	30.5 / 7.1	24.9 / 5.7	14.0 / 4.3	13.0 / 2.9	7.7 / 1.4	1.0 / 0.2
25.6	N/A	42.0 / 9.0	36.0 / 7.7	30.2 / 6.4	24.5 / 5.1	18.4 / 3.9	13.6 / 2.6	7.5 / 1.3	0.5 / 0.1
38.4	N/A	42.5 / 8.4	36.5 / 7.1	30.7 / 6.0	25.0 / 4.7	18.9 / 3.6	14.0 / 2.4	7.4 / 1.2	1.0 / 0.2
51.2	N/A	43.0 / 7.7	37.0 / 6.6	31.2 / 5.5	25.5 / 4.4	19.4 / 3.3	14.0 / 2.2	7.4 / 1.1	0.5 / 0.1
56.0	50.5 / 8.5	44.4 / 7.5	38.4 / 6.4	32.3 / 5.3	26.0 / 4.2	19.7 / 3.2	13.6 / 2.1	7.3 / 1.1	0.0 / 0.0
72.0	50.7 / 8.0	45.0 / 7.0	38.8 / 6.0	32.5 / 5.0	26.3 / 4.0	20.0 / 3.0	14.0 / 2.0	7.4 / 1.0	0.0 / 0.0
64.0	50.0 / 8.3	44.0 / 7.2	38.0 / 6.2	32.0 / 5.3	26.0 / 4.1	19.7 / 3.1	14.0 / 2.1	7.4 / 1.1	0.0 / 0.0
3.5	N/A	43.0 / 20.4	37.4 / 17.3	31.5 / 14.2	26.0 / 11.2	20.2 / 8.1	15.0 / 5.0	10.3 / 2.5	4.1 / 1.0
7.0	N/A	43.8 / 15.4	37.8 / 13.2	32.3 / 11.0	26.4 / 8.8	20.5 / 6.6	15.0 / 4.4	10.0 / 2.2	3.6 / 0.8
14.0	N/A	43.0 / 11.7	37.5 / 10.1	31.9 / 8.34	25.6 / 6.67	19.8 / 5.0	13.9 / 3.3	8.5 / 1.7	2.5 / 0.5
28.0	N/A	43.7 / 9.0	37.5 / 7.7	31.9 / 6.4	25.7 / 5.1	19.5 / 3.9	13.0 / 2.6	7.5 / 1.3	0.5 / 0.1
NOTE: A MAG7 - MAG0 value of 3C hex represents a 1V slicer level at the point of receive data detection.									

APPLICATION INFORMATION

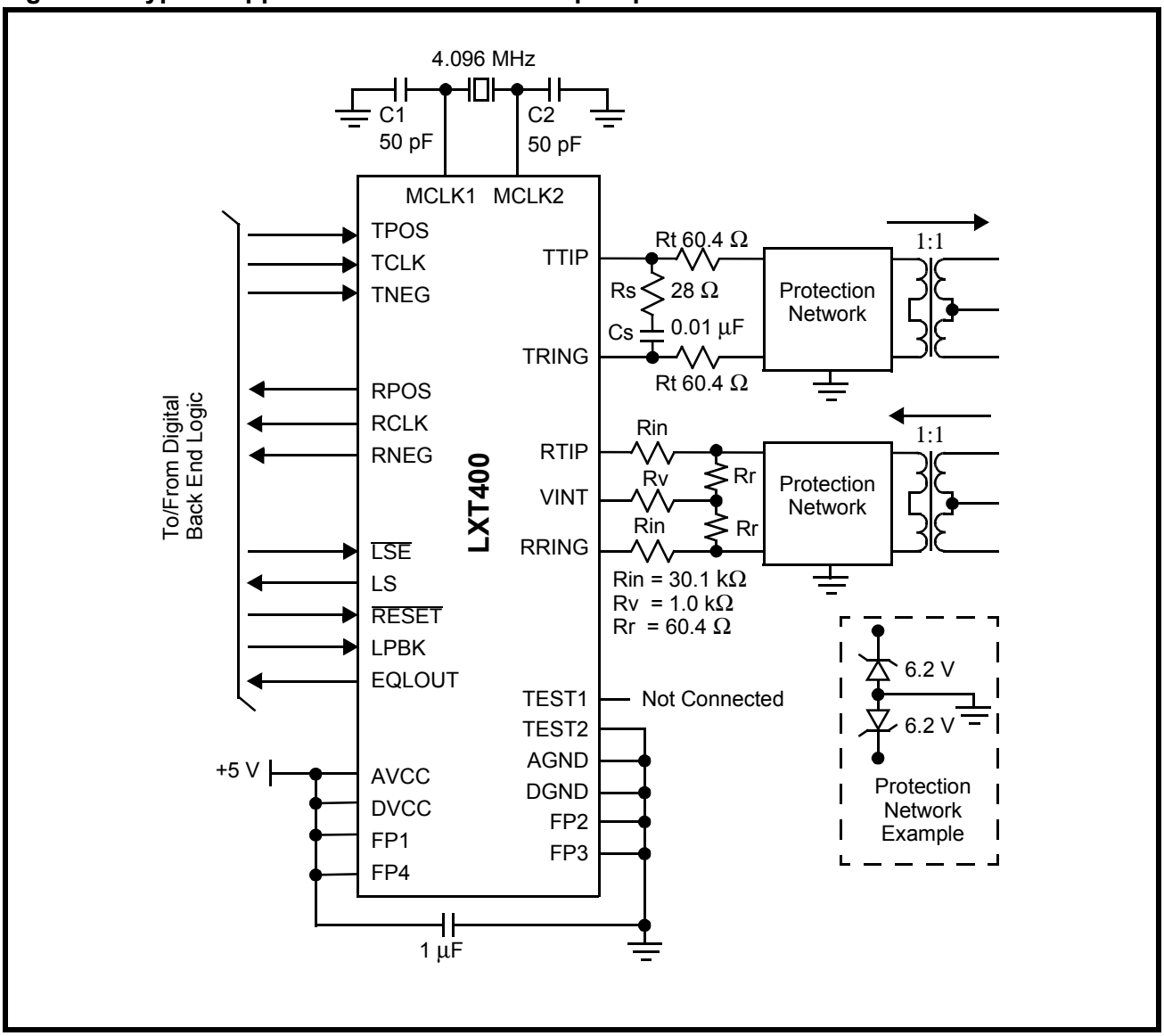
Introduction

Figure 8 shows a typical LXT400 application circuit. A DSU crystal (4.096 MHz) is connected across MCLK1 and MCLK2, with two grounded loading capacitors. The line interface consists of a pair of 1:1 transformers, center-tapped on the line side, with appropriate load resistors. The Rs/Cs shunt network provides high frequency compensation for the transmit driver. The input signal is developed across the Rr/Rin network. Rv limits current into the low-impedance VINT driver during over-voltage conditions on the line. Table 8 lists external component recommendations.

Crosstalk

It is important to prevent crosstalk between the transmitter and receiver circuits. Steps were taken to reduce this interference inside the LXT400, but precautions must be taken with the line interface circuitry outside the chip as well. Crosstalk is especially high when the idle pattern (alternate positive and negative pulses) is being transmitted because the transmit power is concentrated around the Nyquist frequency (half the baud rate).

Figure 8: Typical Application Circuit for 72 kbps Operation



PCB Layout

The external line interface circuit must be laid out to minimize coupling of other digital and analog signals into RTIP and RRING (see Figure 9). These inputs, pins 2 and 3, are high impedance nodes which can pick up interference from adjacent PCB traces. The line interface circuit must be designed for loops with up to 50 dB of loss at the Nyquist frequency, even if the product will never be used on such long lines. When no receive signal is present, the LXT400 will switch to the highest gain filter, which at 56, 64 and 72 kbit/s produces an internal gain of about 50 dB. Unless precautions are taken, substantial interference coupling into RTIP and RRING could exceed the internal slicer levels and prevent the RLOS report. Layout considerations for LXT400 application circuits include:

1. Minimum PCB trace lengths between the LXT400 and the 4.096 MHz crystal and loading capacitors.
2. Minimum PCB trace lengths between resistors Rin and the RTIP and RRING pins. Shield these connections with ground traces.
3. Minimum PCB trace lengths between the receive transformer and the receive termination network.

Even with good PCB layout practices, RLOS reporting can be unreliable if the twisted pair line cable is not connected to the OCU or CSU/DSU when the LXT400 is set for operation at 56, 64, or 72 kbit/s. The unterminated receive lines can pick up enough noise to trip the data detectors and force RLOS Low. However, equipment designers can safely assume that the highest-gain filter with 50 dB of signal amplification will never be selected for normal operation on lines with up to 45 dB of attenuation at the Nyquist frequency. Therefore, the status word on the LS output can be used as a secondary LOS indicator - the occurrence of RLOS=0 and LL3-0 = 0111 at 56, 64 or 72 kbps reliably indicates the loss of carrier condition.

The 50dB filters were designed for applications in which the line attenuation is 48 dB or greater. The DDS specification requires an insertion loss at 56, 64, and 72 kbit/s of 43 dB or less. The LXT400 incorporates built-in headroom up to 45 dB. So for standard applications, the highest-gain filter will never be selected. The critical element is operating frequency. The highest gain filter (50 dB) is only available at 56, 64, and 72 kbit/s settings. At the lower operating frequencies, the highest-gain filter is about 44 dB, well above the interference levels arising from unterminated lines.

Figure 9: Suggested LXT400 PCB Layout

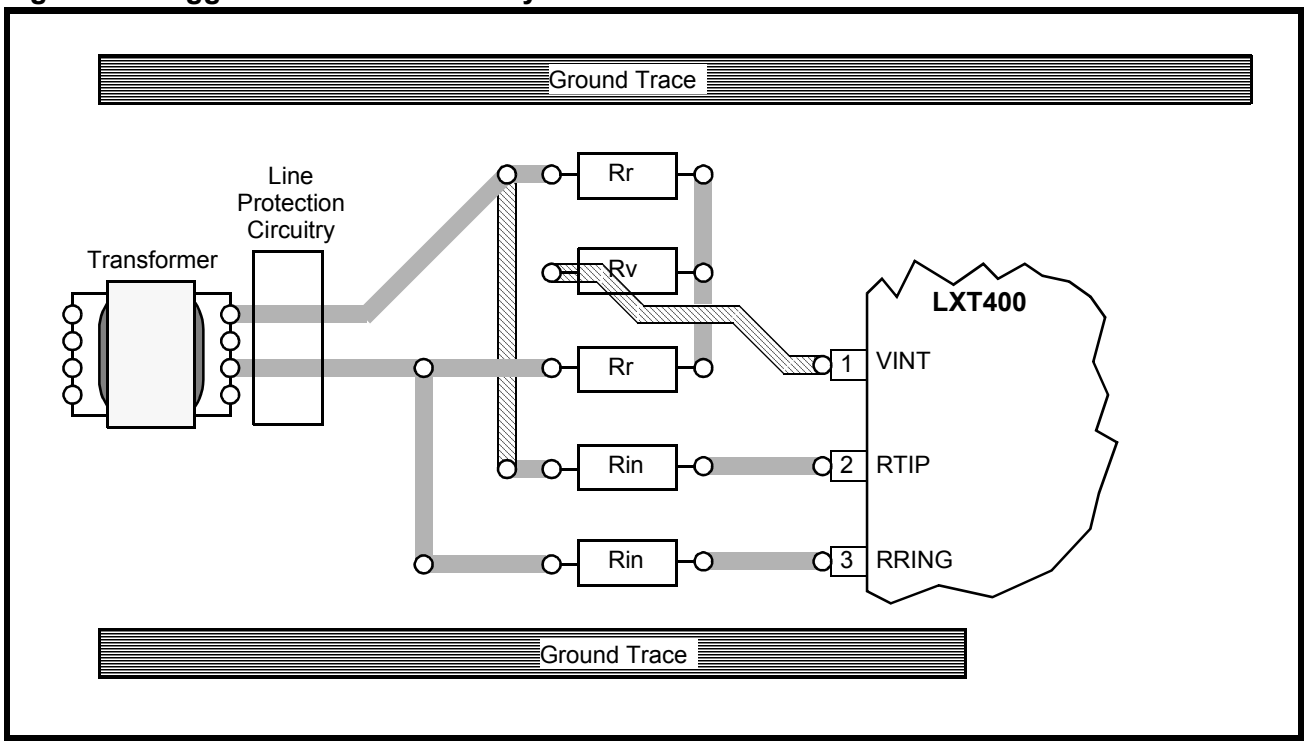


Table 8: External Component Recommendations

Component	Parameter	Recommended Value
Line Transformer	Turns ratio	1:1, ± 1%
	Structure	Center tapped (line side only)
Suggested Manufacturers	Primary Inductance	200 mH minimum
Midcom - Phone 800/643-2661	Leakage Inductance	22 to 43 µH maximum
Schott - Phone 615/889-8800	Interwinding Capacitance	350 pF maximum
	DC Resistance (Primary, Rwp)	7 to 15 Ω
	DC Resistance (Secondary, Rws)	7 to 15 Ω, See Rt, Rr calculation
Rin	Resistance, Tolerance, Rating	30.1 kΩ, ± 1%, 1/4 W
Rt, Rr	Resistance, Tolerance, Rating	(135 Ω - Rwp - Rws) / 2, ± 1%, 1/4 W
Rv	Resistance, Tolerance, Rating	1 kΩ, ± 5%, 1/4 W
DSU Crystal	Nominal frequency	4.096 MHz
	Holder style	HC-49/U
Suggested Manufacturers	Operating Mode	Fundamental, parallel resonant
Fox - Phone 813/693-0099	Load Capacitance	28 pF nominal
Monitor - Phone 815/432-5296	Tolerance	± 35 ppm @ 25 °C
	Range	± 50 ppm, -40 to 85 °C
	Aging	3 ppm per year maximum
	Maximum ESR	100 Ω
	Drive Level	1 mW maximum
DSU Crystal Loading Capacitors	Capacitance, Tolerance, Rating	50 pF, ±5%, 10 V
	Construction	NPO ceramic or equivalent
Transmit Shunt Network		
Rs	Resistance, Tolerance, Rating	28 Ω, ± 5%, 1/4 W
Cs	Capacitance, Tolerance, Rating	0.01 µF, ± 20%, 10 V

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 9 through 13 and Figures 10 through 14 represent the performance specifications of the LXT400 and are guaranteed by test, except where noted by design.

Table 9: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
DC Supply	AVCC referenced to AGND	-0.3	6.0	V
	DVCC referenced to DGND	-0.3	6.0	V
	DVCC referenced to AVCC	-0.3	0.3	V
	DGND referenced to AGND	-0.3	0.3	V
Input Voltage, any pin[1,2]		AGND - 0.3	AVCC + 0.3	V
Input or output diode current, any pin [2]		–	±20	mA
Continuous output current, any pin [2]		–	±25	mA
Continuous current, VCC or GND pins		–	±60	mA
Storage Temperature		-40	±150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. TTIP and TRING are referenced to DVCC and DGND.
2. Except DC supply pins.

Table 10: Recommended Operating Conditions and Characteristics

Parameter	Sym	Min	Typ	Max	Units
DC supply	AVCC/DVCC	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	–	85	° C

Table 11: DC Electrical Characteristics (Under Recommended Operating Conditions)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Supply current (transmitting spaces)	I_{CC}	–	40	60	mA	270 Ω resistor across TTIP and TRING
Supply current (transmitting all marks)	I_{CC}	–	47.5	60	mA	270 Ω resistor across TTIP and TRING
Input Low voltage	V_{IL}	–	–	0.8	V	Digital inputs
Input High voltage	V_{IH}	2.0	–	–	V	Digital inputs

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: DC Electrical Characteristics (Under Recommended Operating Conditions) – continued

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Low voltage	V_{OL}	–	0.2	–	V	I_{OL} < 10 µA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = 0.4 mA
Output High voltage	V_{OH}	–	4.5	–	µA	I_{OH} < 10 µA
Input leakage current	I_{IL}	-40	–	40	µA	0 < V_{IN} < Vcc

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 12: AC Electrical Characteristics

Parameter		Sym	Min	Typ[1]	Max	Units
Input capacitance		C_{IN}	–	7	–	pF
TCLK jitter at DSU with respect to RCLK		t_{JIT}	–	–	2	% tpr at DSU
RCLK isochronous distortion at DSU		r_{JIT}	–	–	5	% tpt at OCU
Transmit output jitter with respect to TCLK		o_{JIT}	–	–	3	% tpt at DSU
Transmit pulse amplitude at TTIP/TRING 2	at 9.6 and 12.8 kbps	A_T	1.44	1.55	1.75	V
	at all other rates	A_T	2.56	2.74	2.92	V

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. The instantaneous peak amplitude of an isolated pulse (i.e. a mark between two spaces) into a 270 Ω resistive load.

Table 13: Timing Characteristics

Parameter		Sym	Min	Typ[1]	Max	Unit
Receive Timing Figure 10	RCLK period	t_{PR}	–	1/fb	–	ns
	RCLK pulse width High	t_{RWH}	1/ (2 fb) - 150	1/ (2 fb)	1/(2 fb)+150	ns
	RPOS/RNEG delay from RCLK rising edge[2]	t_{DP}	–	–	200	ns
	Transition time on any digital output[2]	t_{TO}	–	10	20	ns
Transmit Timing Figure 11	TCLK period	t_{PT}	–	1/ fb	–	µs
	TCLK pulse width High	t_{TWH}	400	–	–	ns
	TPOS/TNEG setup time to TCLK falling edge	t_{TSU}	200	–	–	ns
	TPOS/TNEG hold time from TCLK falling edge	t_{TH}	200	–	–	ns
	Transition time on any digital input	t_{TI}	–	–	40	ns
	TCLK frequency tolerance	f_{TTOL}	-50	0	+50	ppm

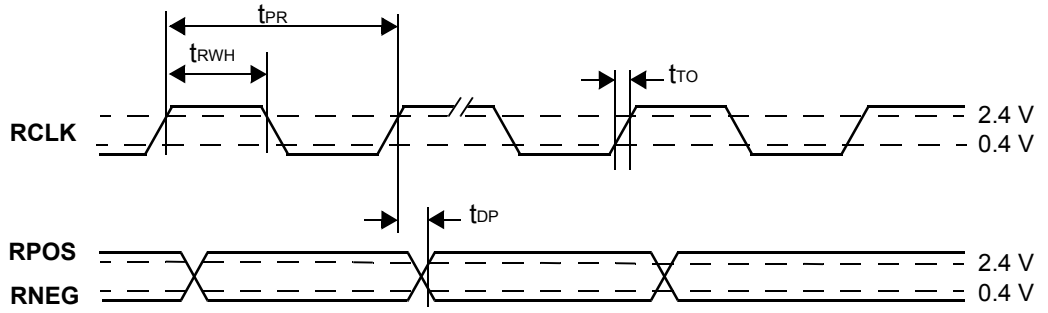
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured with 15pf load.

Table 13: Timing Characteristics – continued

Parameter		Sym	Min	Typ[1]	Max	Unit
LS Serial Port Timing Figure 12 Figure 13	LS delay from RCLK falling edge[2]	t_{LSP}	–	–	200	ns
	$\overline{LSE}$ setup to RCLK rising edge	t_{LSU}	200	–	–	ns
	$\overline{LSE}$ hold time from RCLK rising edge	t_{LSH}	t_{RWH}	–	–	ns
	$\overline{LSE}$ Low to low Z state	t_{LZ}	–	–	100	ns
	$\overline{LSE}$ High to high Z state	t_{HZ}	–	–	100	ns
MCLK & $\overline{RESET}$ Timing Figure 14	MCLK1 input frequency	f_{MCLK}	–	4.096	–	MHz
	MCLK1 frequency tolerance	f_{MTOL}	-100	0	+100	ppm
	MCLK1 pulse width High	t_{MWH}	98	122	146	ns
	$\overline{RESET}$ pulse width Low	t_{RWL}	1000	–	–	ns

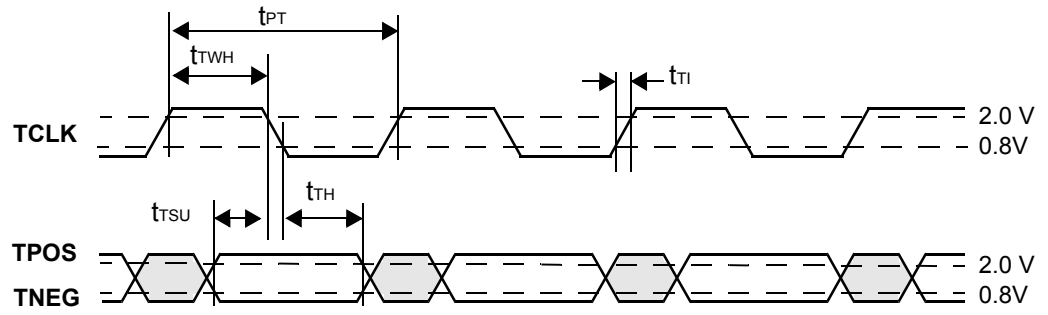
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured with 15pf load.

Figure 10: Receive Digital Timing



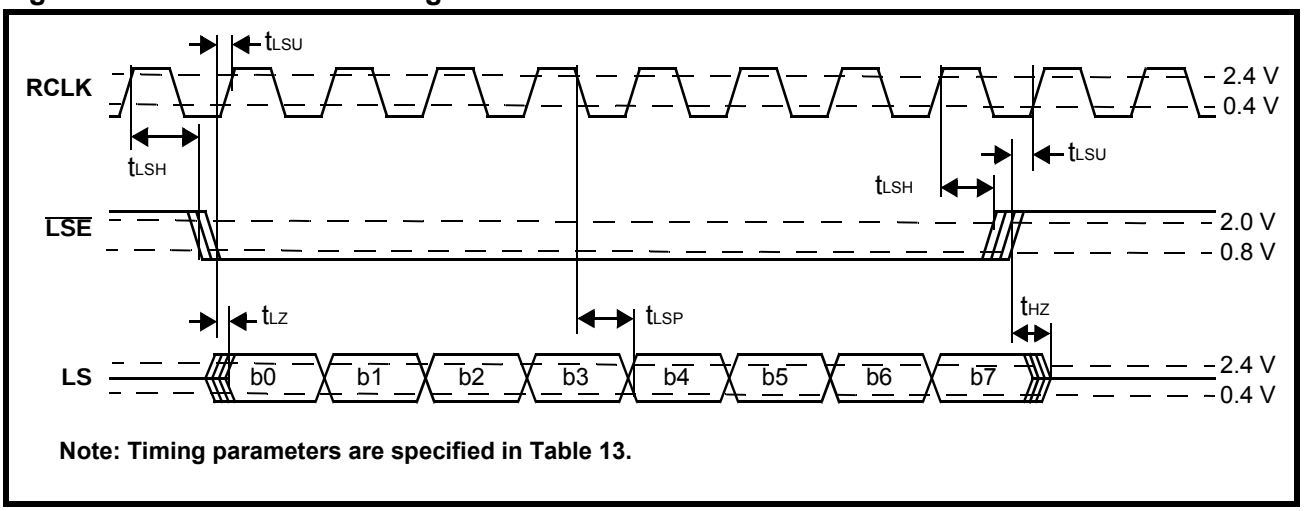
Note: Timing parameters are specified in Table 13.

Figure 11: Transmit Digital Timing



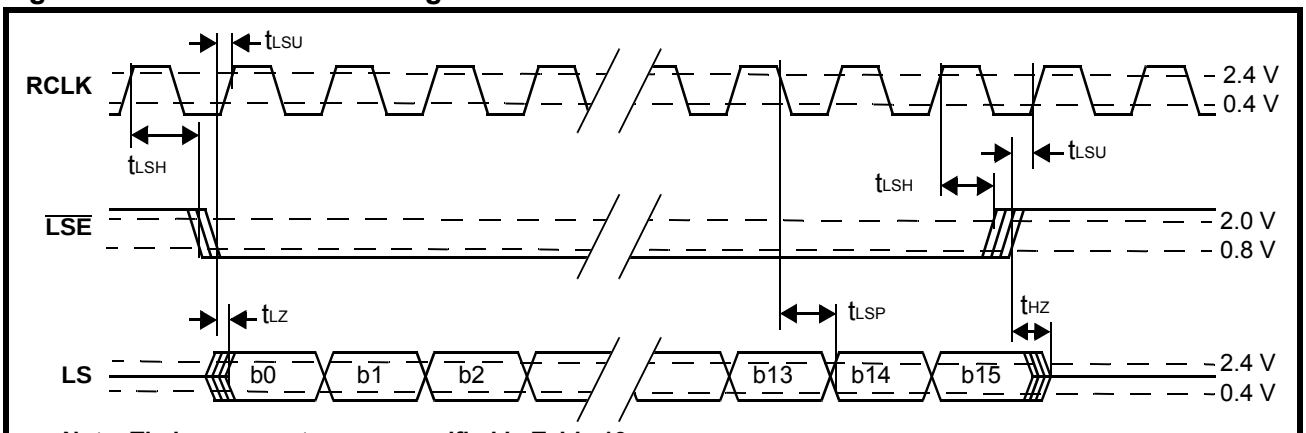
Note: Timing parameters are specified in Table 13.

Figure 12: LS Serial Port Timing - 8-Bit Word



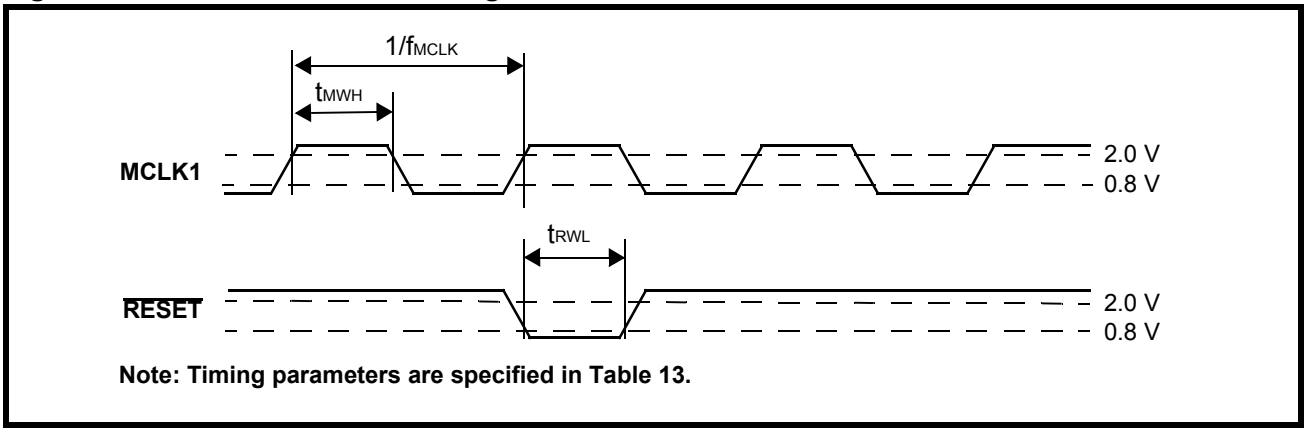
Note: Timing parameters are specified in Table 13.

Figure 13: LS Serial Port Timing - 16-Bit Word



Note: Timing parameters are specified in Table 13.

Figure 14: MCLK and $\overline{\text{RESET}}$ Timing



Note: Timing parameters are specified in Table 13.

NOTES