DATA SHEET

APRIL 1997
Revision 1.2

LXT904

Ethernet Interface Adapter with EnDec and AUI

General Description

The LXT904 Ethernet Interface Adapter is designed for IEEE 802.3 applications. It provides all the active circuitry to adapt most standard 802.3 controllers to the Attachment Unit Interface (AUI). The LXT904 is a pin-compatible replacement for the LXT901 in applications that do not require a twisted-pair port. In addition to standard 10 Mbps Ethernet, the LXT904 also supports full-duplex operation at 20 Mbps.

LXT904 functions include Manchester encoding/decoding and AUI driving/receiving. The LXT904 can also be used to drive the AUI drop cable.

The LXT 904 is fabricated using an advanced CMOS process and requires only a single 5-volt power supply.

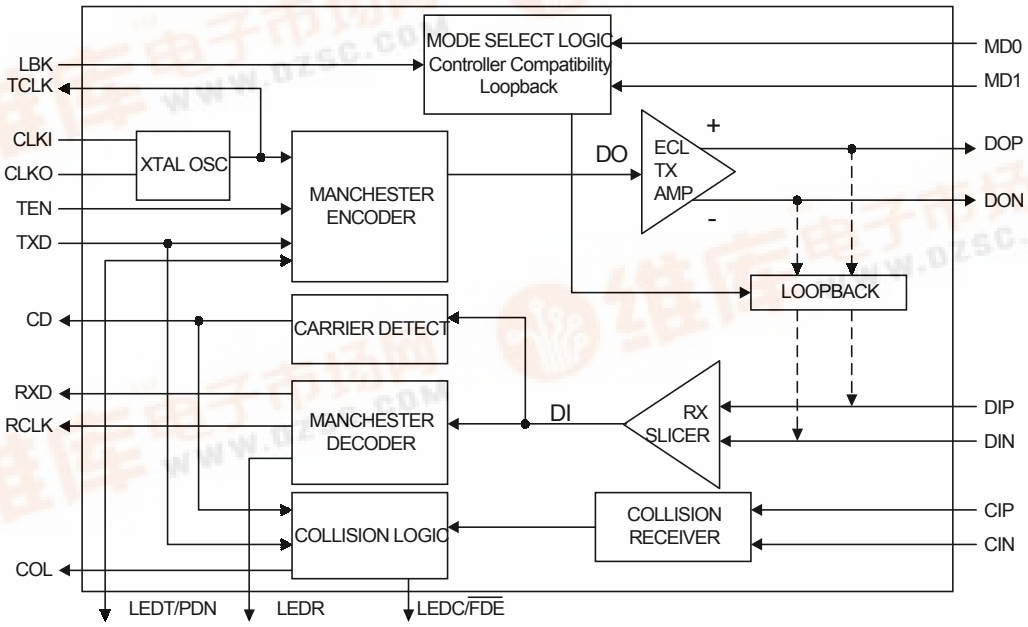
Features

- Integrated Manchester Encoder/Decoder
- AUI Transceiver
- Supports Standard and Full-Duplex Ethernet
- Power Down Mode
- AUI Loopback mode for better testing
- Three LED Drivers
- Available in 44-pin PLCC package

Applications

- Bridges, routers and Ethernet-to-WAN access equipment
- Computer/workstation LAN adapter boards

LXT904 Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT904 Pin Assignments

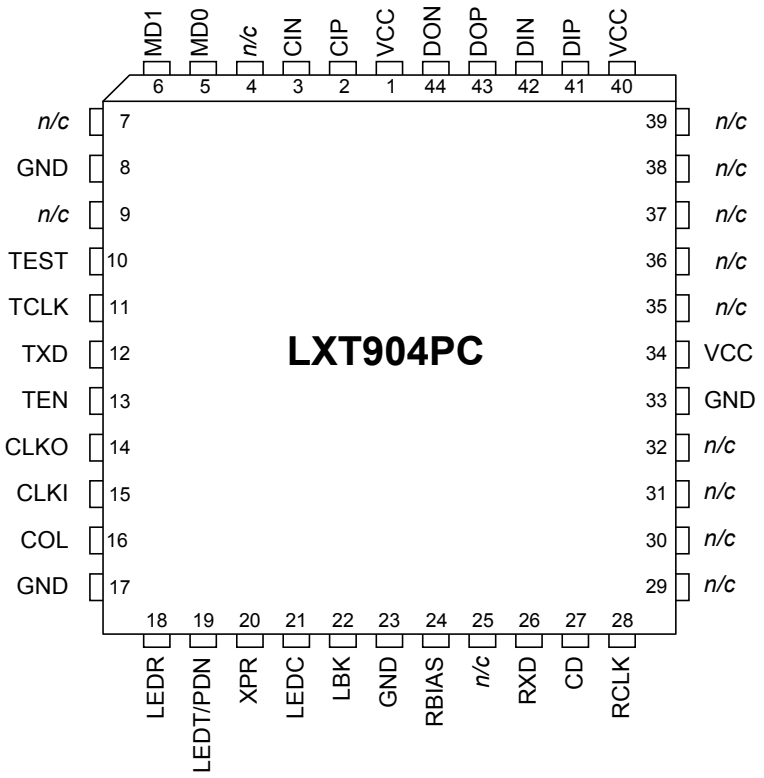


Table 1: LXT904 Pin Descriptions

Pin #	Sym	I/O	Description
1	VCC	I	**Power Input.** + 5 volt power supply input.
2	CIP	I	**AUI Collision Pair.** Differential input pair connected to the AUI transceiver CI circuit.
3	CIN	I	The input is collision signaling or SQE.
4	*n/c*	–	**No connection.** This pin must be left floating.
5	MD0	I	**Mode Select 0; Mode Select 1.** Mode select pins determine controller compatibility mode in accordance with Table 2.
6	MD1	I	
7	*n/c*	–	**No connection.** This pin must be left floating.
8	GND	–	**Ground.** Ground return.
9	*n/c*	–	**No connection.** This pin must be left floating.
10	TEST	I	**Test.** This pin must be tied High.
11	TCLK	O	**Transmit Clock.** A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.

Table 1: LXT904 Pin Descriptions – continued

Pin #	Sym	I/O	Description
12	TXD	I	**Transmit Data.** Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
13	TEN	I	**Transmit Enable.** Enables data transmission and starts the watchdog timer. Synchronous to TCLK (see Figures 5, 11, 17 and 23 for details).
14 15	CLKO CLKI	O I	**Crystal Oscillator.** A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.
16	COL	O	**Collision Detect.** Output which drives the collision detect input of the controller.
17	GND	–	**Ground.** Ground return.
18	LEDR	O	**Receive LED.** Open drain driver for the receive indicator LED. Output is pulled Low during receive.
19	LEDT/ PDN	O I	**Transmit LED/Power Down.** Open drain driver for the transmit indicator. Output is pulled Low during transmit. If externally tied Low, the LXT904 goes to power down state.
20	XPR	–	**External Pull Up.** Requires an external pull-up resister.
21	LEDC	O	**Collision LED.** Open drain driver for the collision indicator pulls Low during collision.
22	LBK	I	**Loopback.** Enables internal loopback mode. See Figure 8 (Mode 1), Figure 14 (Mode 2), Figure 20 (Mode 3) and Figure 26 (Mode 4) for details.
23	GND	–	**Ground.** Ground Return.
24	RBIAS	I	**Bias Control.** A 12.4 kΩ 1% resistor to ground at this pin controls operating circuit bias.
25	*n/c*	–	**No connection.** This pin must be left floating.
26	RXD	O	**Receive Data.** Output signal connected directly to the receive data input of the controller.
27	CD	O	**Carrier Detect.** An output to notify the controller of activity on the network.
28	RCLK	O	**Receive Clock.** A recovered 10 MHz clock which is synchronous to the received data and connected to the controller receive clock input.
29 30 31 32	*n/c* *n/c* *n/c* *n/c*	– – – –	**No connection.** These pins must be left floating.
33	GND	–	**Ground.** Ground Return.
34	VCC	I	**Power Input .** + 5 volt power supply input.
35 36 37 38 39	*n/c* *n/c* *n/c* *n/c* *n/c*	– – – – –	**No connection.** These pins must be left floating.
40	VCC	I	**Power Input.** + 5 volt power supply input.
41 42	DIP DIN	I I	**AUI Receive Pair.** Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
43 44	DOP DON	O O	**AUI Transmit Pair.** A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.

FUNCTIONAL DESCRIPTION

The LXT904 Ethernet Interface Transceiver performs the physical layer signaling (PLS) functions as defined by the IEEE 802.3 specification. It functions as a PLS-Only device for use with 10BASE-5 or 10BASE-2 coaxial cable networks. In addition to standard 10 Mbps operation, the LXT904 also supports full-duplex 20 Mbps operation.

Refer to the block diagram on the first page of this data sheet. The LXT904 interfaces a back end controller to an AUI drop cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision (CI). In addition to these basic interfaces, the LXT904 contains an internal crystal oscillator and three LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The LXT904 Transmit function refers to data transmitted by the back end to the AUI cable. The LXT904 receive function refers to data received by the back end from the AUI cable. The LXT904 receives incoming signals from the AUI DI circuit with ±18 ns of jitter and drives the AUI DO circuit. The CI pins are monitored for collision status.

Transmit Function

The LXT904 receives NRZ data from the controller at the TXD input, and passes it through a Manchester encoder. The encoded data is then transferred to the AUI cable (the DO circuit).

Receive Function

The LXT904 receive function acquires timing and data from the AUI (the DI circuit). Valid received signals are passed through the on-chip decoder and then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

The receive function is activated only by valid data streams above the squelch level with proper timing. If the differential signal at the DI circuit inputs falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT904 receive function enters the idle state.

Loopback Function

Loopback is controlled by the LBK pin. When LBK is High, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK is Low, no AUI loopback occurs.

Controller Compatibility Modes

The LXT904 is compatible with most industry standard controllers including devices produced by Motorola, Advanced Micro Devices (AMD), Intel, Fujitsu, National Semiconductor, Seeq and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins (MD0 and MD1) determine the controller compatibility mode as listed in Table 2.

A complete set of timing diagrams and specifications for each mode is provided in the Test Specifications section.

Table 2: Controller Compatibility Modes

Controller Mode	Settings	
	MD1	MD0
Mode 1–For Motorola 68EN360, Advanced Micro Devices AM7990 or compatible controllers	Low	Low
Mode 2–For Intel 82596 or compatible controllers	Low	High
Mode 3–For Fujitsu MB86950 or MB86960, Seeq 8005 or compatible controllers[1]	High	Low
Mode 4–For National Semiconductor 8390, Texas Instruments TMS380C26 or compatible controllers	High	High

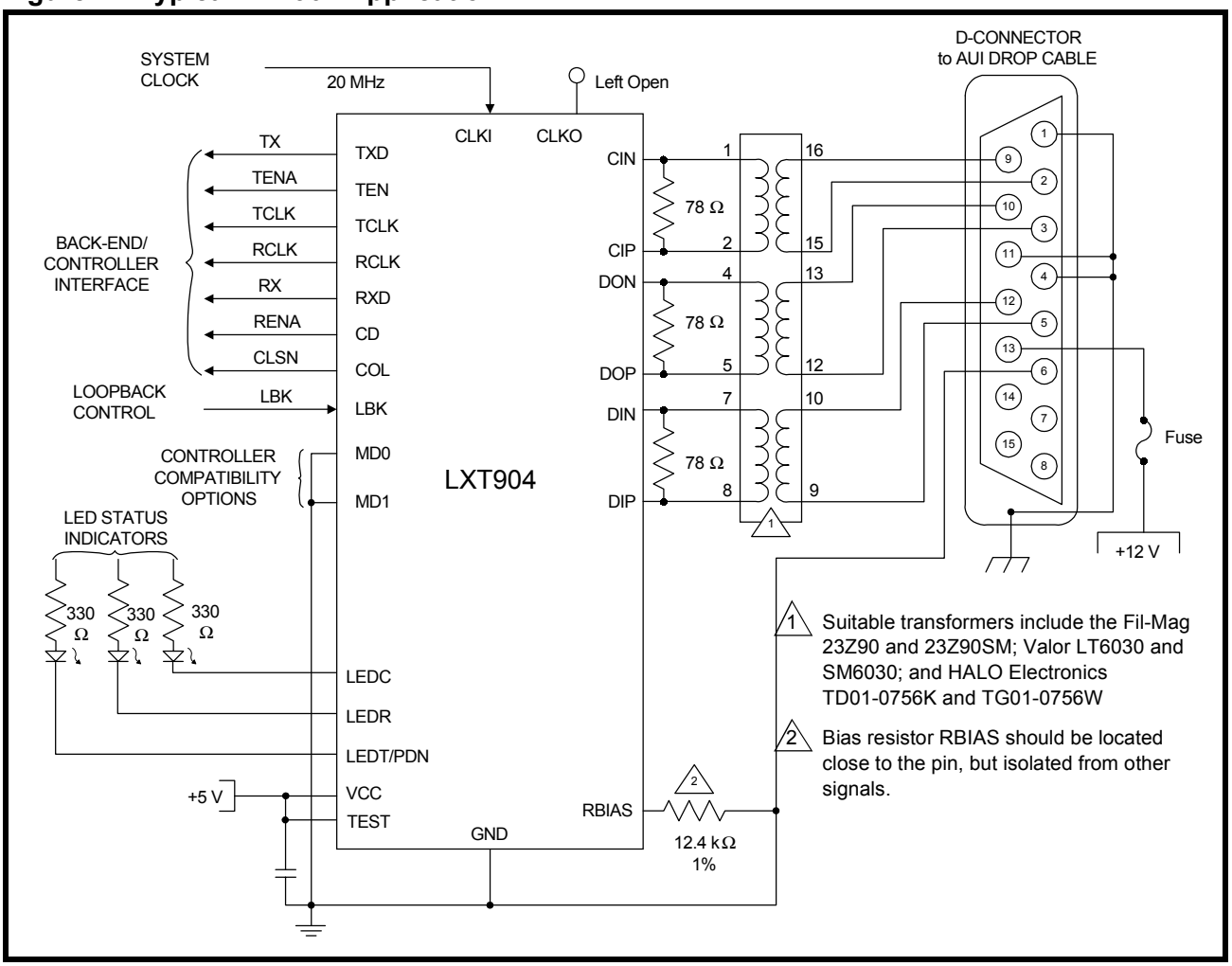
1. Seeq Controllers require inverters on CLKI, LBK, RCLK, and COL.

APPLICATION INFORMATION

Figure 2 is a typical LXT904 application. The diagram is arranged to group similar pins together; it does not represent the actual LXT904 pinout. The controller interface pins (transmit data, clock and enable; receive data and clock; and the collision detect, carrier detect and loopback control pins) are shown at the top left.

With MD1 and MD0 both Low, the LXT904 logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LBK input controls loopback. A 20 MHz system clock is supplied at CLKI with CLKO left open.

Figure 2: Typical LXT904 Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 11 and Figures 3 through 26 represent the performance specifications of the LXT904 and are guaranteed by test, except where noted by design.

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	VCC	-0.3	-	6	V
Operating Temperature	TOP	0	-	70	°C
Storage Temperature	TST	-65	-	150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4: Operating Conditions (Voltage with respect to ground unless otherwise specified.)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Recommended supply voltage	VCC	4.75	5.0	5.25	V	
Recommended operating temperature	TOP	0	-	70	°C	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 5: Electrical Characteristics (Over Recommended Range)

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Voltage [2]		VIL	-	-	0.8	V	
Input High Voltage [2]		VIH	2.0	-	-	V	
Output Low Voltage		VOL	-	-	0.4	V	IOL= 1.6 mA
		VOL	-	-	10	$\%V_{CC}$	IOL< 10µA
Output Low Voltage (Open drain LED Driver)		VOLL	-	-	0.7	V	IOLL= 10mA
Output High Voltage		VOH	2.4	-	-	V	IOH= 40µA
		VOH	90	-	-	$\%V_{CC}$	IOL < 10µA
Supply current	Normal mode	ICC	-	65	85	mA	Idle mode
		ICC	-	70	90	mA	Transmitting on AUI
	Power Down mode	ICC	-	0.75	2	mA	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels of 0 V and 3 V.

Table 6: Clock Timing (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Output Rise Time TCLK & RCLK	CMOS	-	-	3	12	ns	CLOAD = 20 pF
	TTL	-	-	2	8	ns	
Output Fall Time TCLK & RCLK	CMOS	-	-	3	12	ns	CLOAD= 20 pF
	TTL	-	-	2	8	ns	
CLKI rise time (externally driven)		-	-	-	10	ns	
CLKI duty cycle (externally driven)		-	-	50/50	40/60	%	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 7: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low Current	I_{IL}	-	-	-700	mA	
Input High Current	I_{IH}	-	-	500	mA	
Differential Output Voltage	V_{OD}	±150	-	±1200	mV	
Differential Squelch Threshold	V_{DS}	150	220	350	mV	5 MHz square wave input

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 8: RCLK/Start-of-Frame Timing

Parameter		Symbol	Minimum	Typical[1]	Maximum	Units
Decoder acquisition time		t_{DATA}	-	900	1100	ns
CD turn-on delay		t_{CD}	-	50	200	ns
Receive data setup from RCLK	Mode 1	t_{RDS}	60	70	-	ns
	Modes 2, 3 and 4	t_{RDS}	30	45	-	ns
Receive data hold from RCLK	Mode 1	t_{RDH}	10	20	-	ns
	Modes 2, 3 and 4	t_{RDH}	30	45	-	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 9: RCLK/End-of-Frame Timing

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Minimum	t_{RC}	5	1	27	5	bit times
Rx data throughput delay	Maximum	t_{RD}	400	375	375	375	ns
CD turn off delay [2]	Maximum	t_{CDOFF}	500	475	475	475	ns
Receive block out after TEN off	Typical[1]	t_{IFG}	5	50	-	-	bit times

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. CD turn-off delay is measured from the middle of the last bit; timing specification is unaffected by value of the last bit.

Table 10: Transmit Timing

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
TEN Setup from TCLK	tEHCH	22	-	-	ns
TXD Setup from TCLK	tDSCH	22	-	-	ns
TEN Hold after TCLK	tCHEL	5	-	-	ns
TXD Hold after TCLK	tCHDU	5	-	-	ns
Transmit Start-up Delay - AUI	tSTUD	-	200	450	ns
Transmit Through-put Delay - AUI	tTPD	-	-	300	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

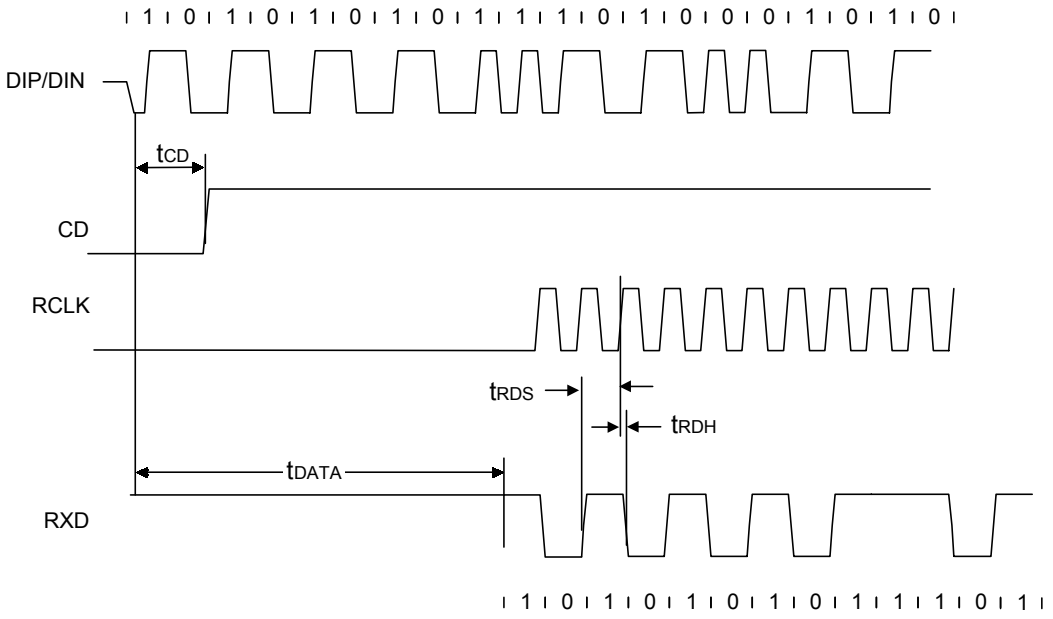
Table 11: Collision and Loopback Timing

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
COL turn on delay	tCOLD	-	-	500	ns
COL turn off delay	tCOLOFF	-	-	500	ns
COL (SQE) Delay after TEN off	tSQED	0.65	-	1.6	µs
COL (SQE) Pulse Duration	tSQEP	500	-	1500	ns
LBK setup from TEN	tKHEH	10	25	-	ns
LBK hold after TEN	tKHEL	10	0	-	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

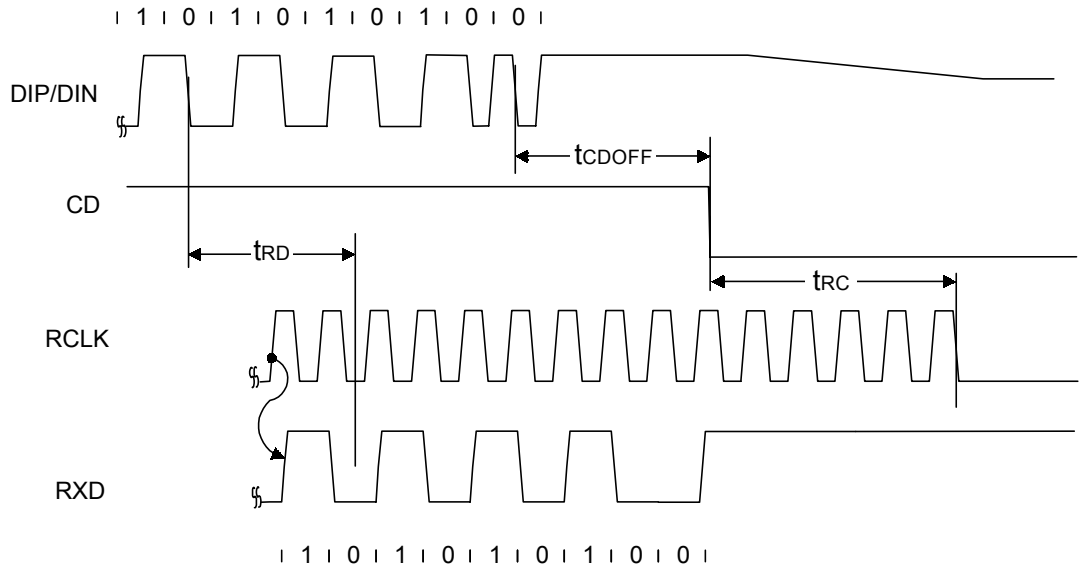
Timing Diagrams for Mode 1 (MD1 = Low, MD0 = Low)

Figure 3: Mode 1 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 4: Mode 1 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes 25 ns after the rising edge of RCLK.

Figure 5: Mode 1 Transmit Timing

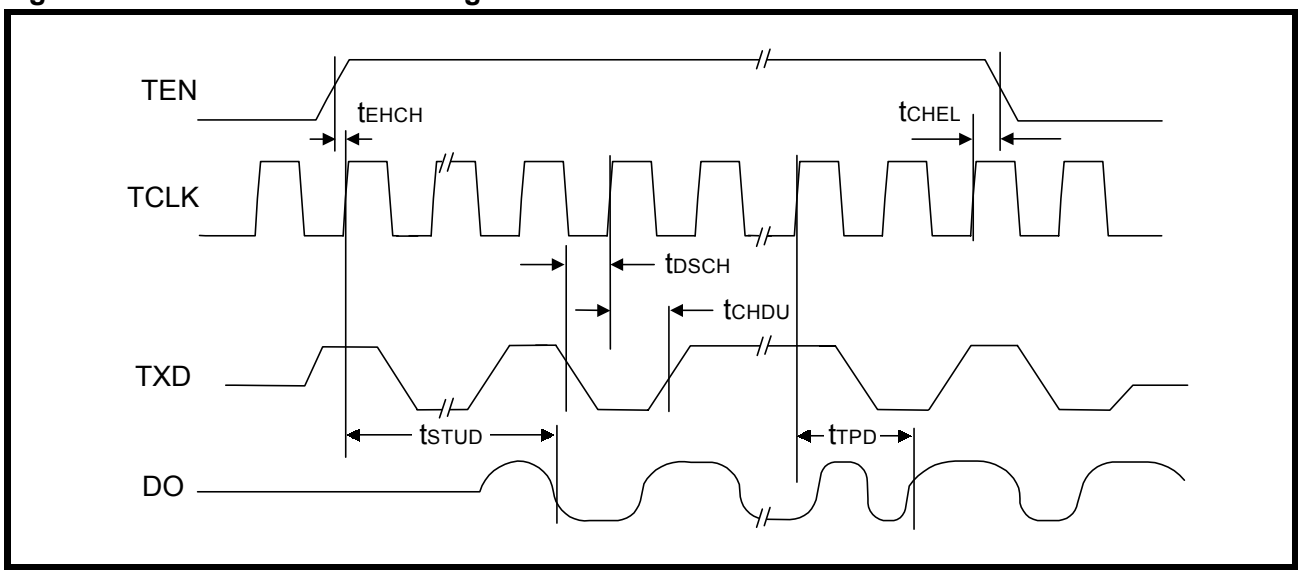


Figure 6: Mode 1 Collision Detect Timing

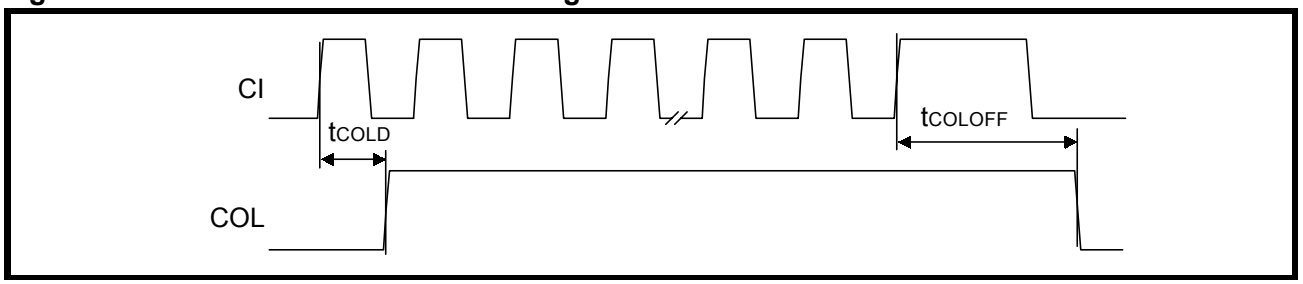


Figure 7: Mode 1 COL/CI Output Timing

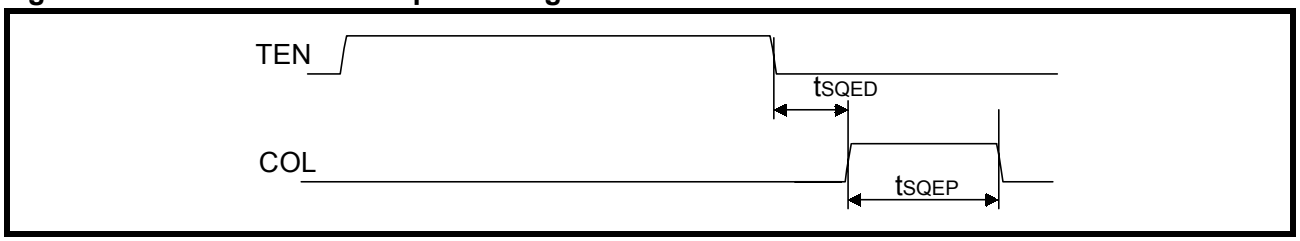
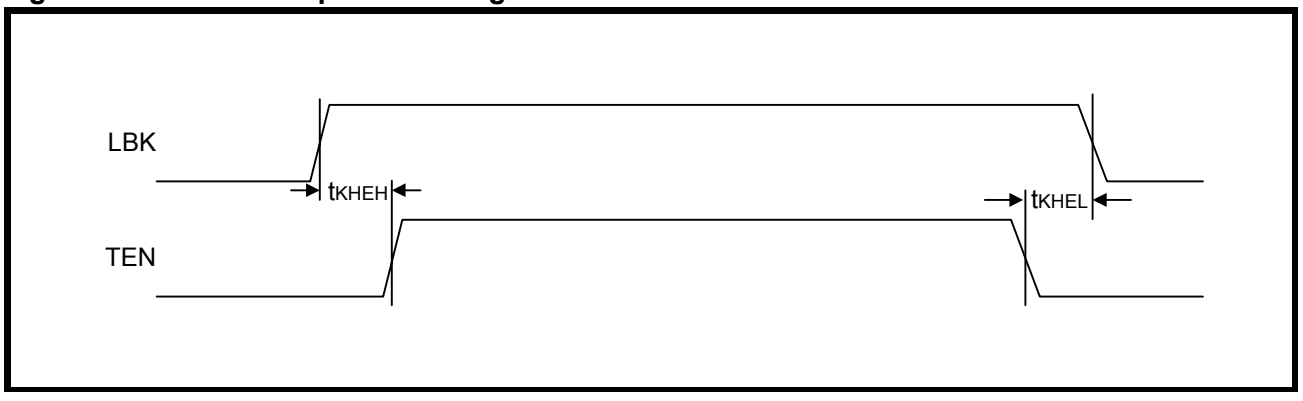
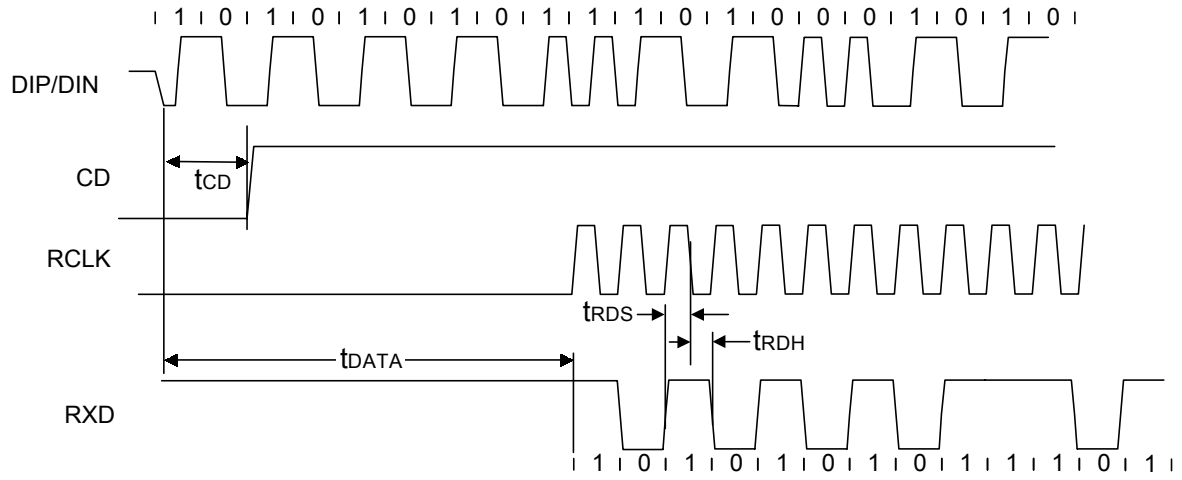


Figure 8: Mode 1 Loopback Timing



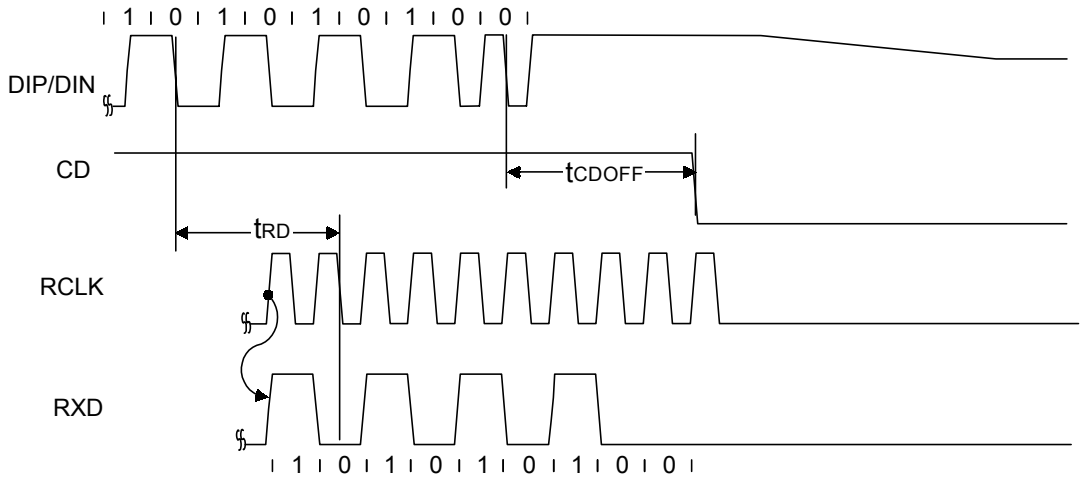
Timing Diagrams for Mode 2 (MD1 = Low, MD0 = High)

Figure 9: Mode 2 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 10: Mode 2 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 11: Mode 2 Transmit Timing

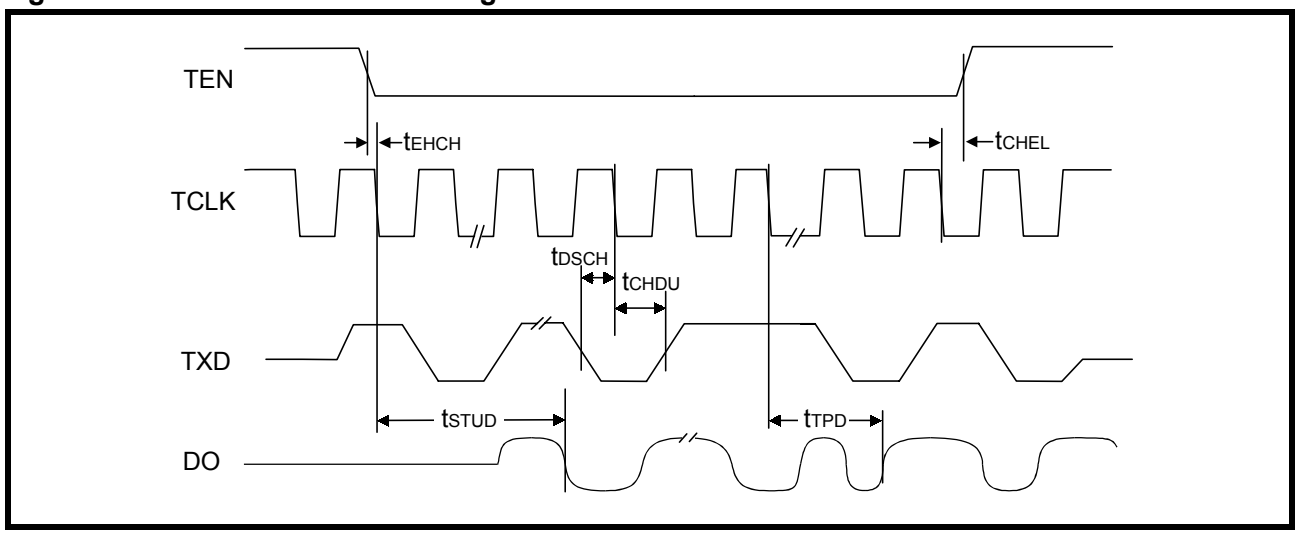


Figure 12: Mode 2 Collision Detect Timing

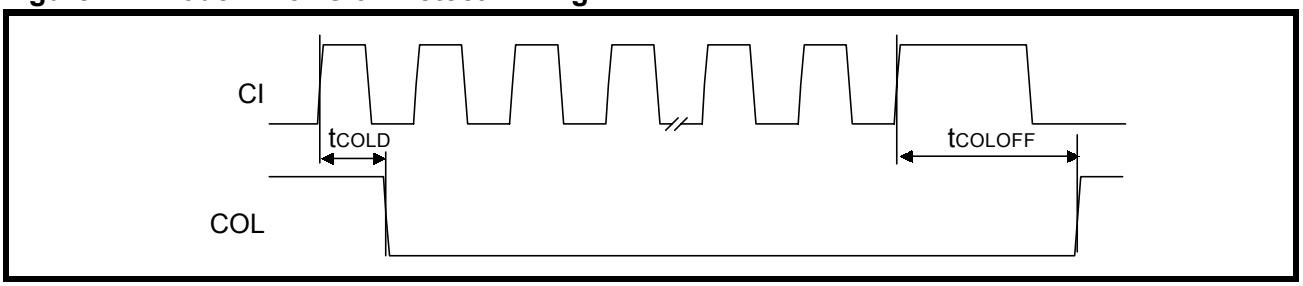
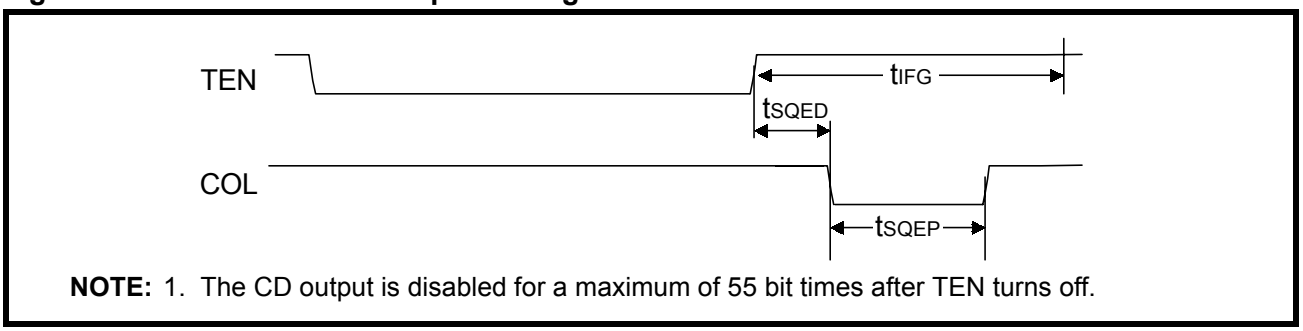
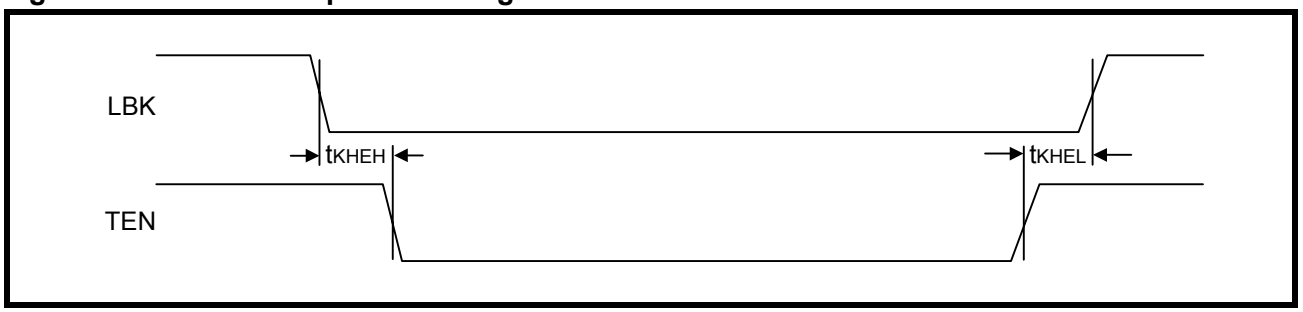


Figure 13: Mode 2 COL/CI Output Timing



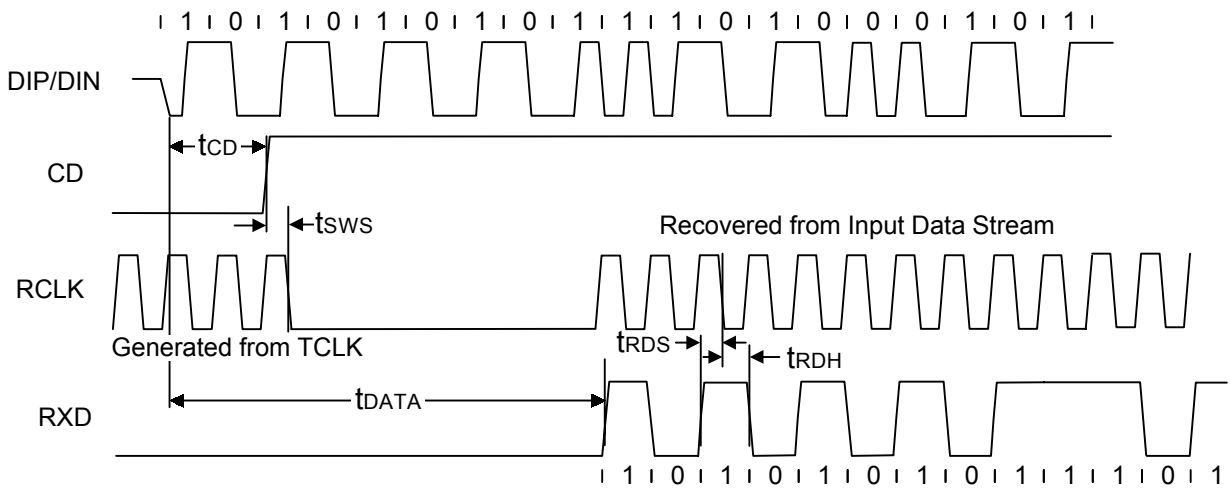
NOTE: 1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 14: Mode 2 Loopback Timing



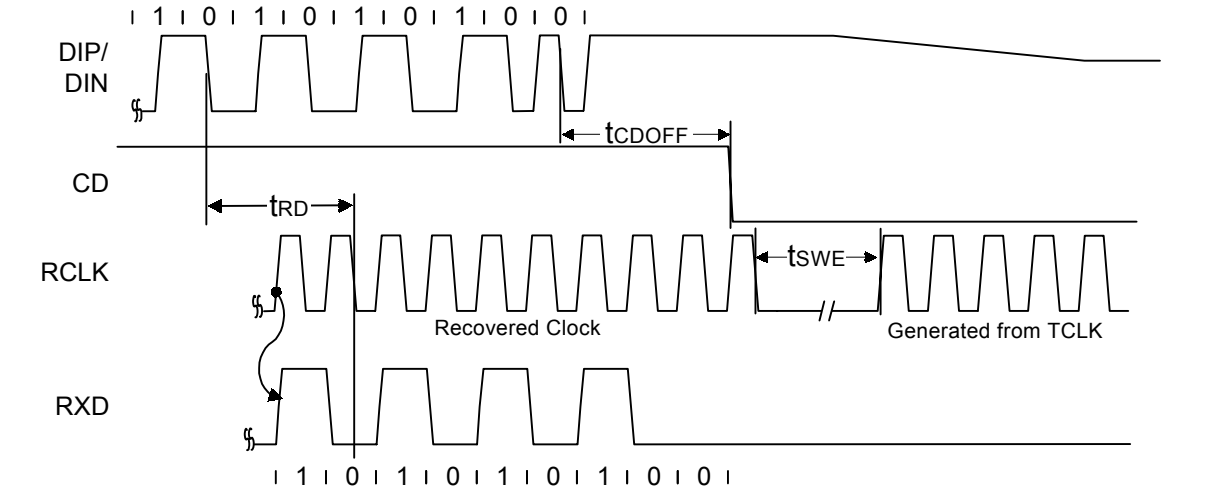
Timing Diagrams for Mode 3 (MD1 = High, MDO = Low)

Figure 15: Mode 3 RCLK/Start-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 16: Mode 3 RCLK/End-of-Frame Timing



NOTE: 1. RXD changes at the rising edge of RCLK. The controller is sampled at the falling edge.

Figure 17: Mode 3 Transmit Timing

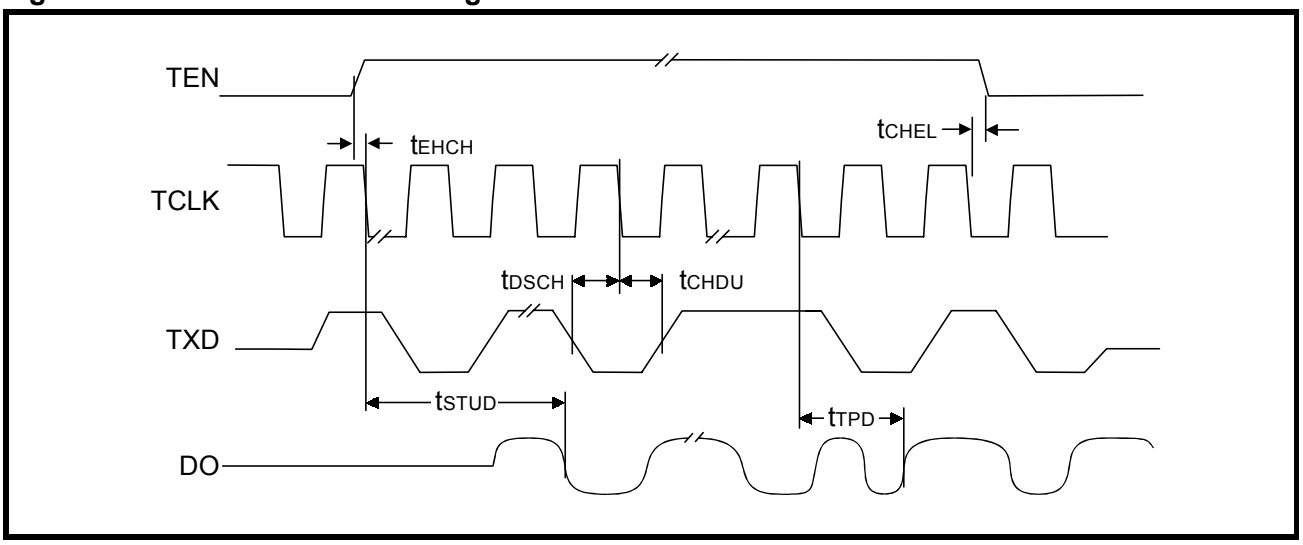


Figure 18: Mode 3 Collision Detect Timing

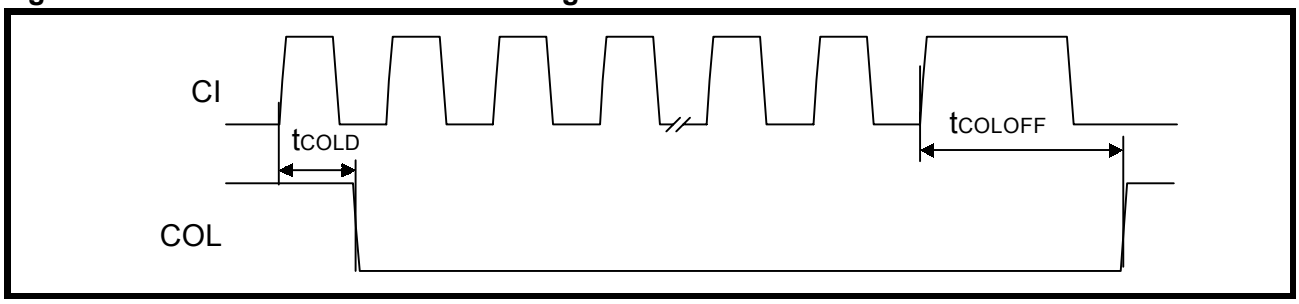
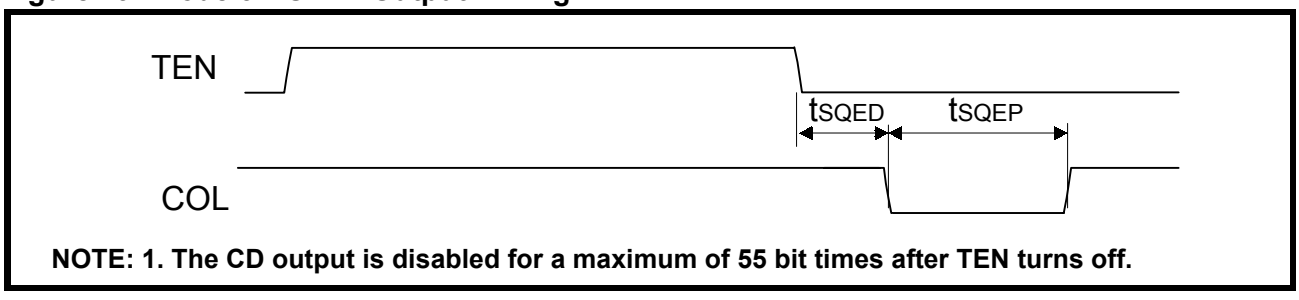
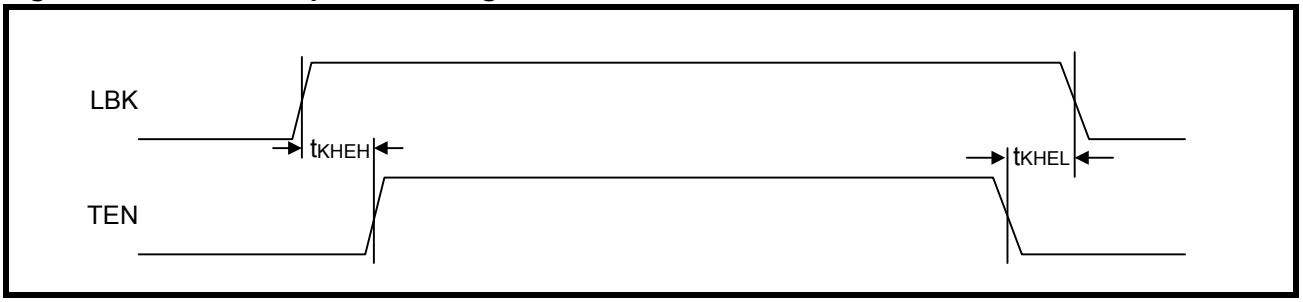


Figure 19: Mode 3 COL/CI Output Timing



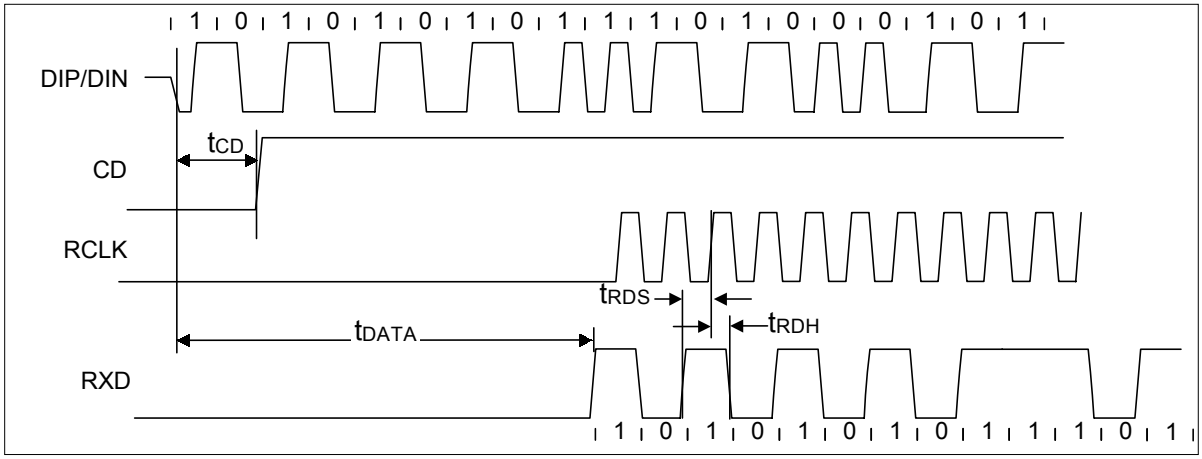
NOTE: 1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

Figure 20: Mode 3 Loopback Timing



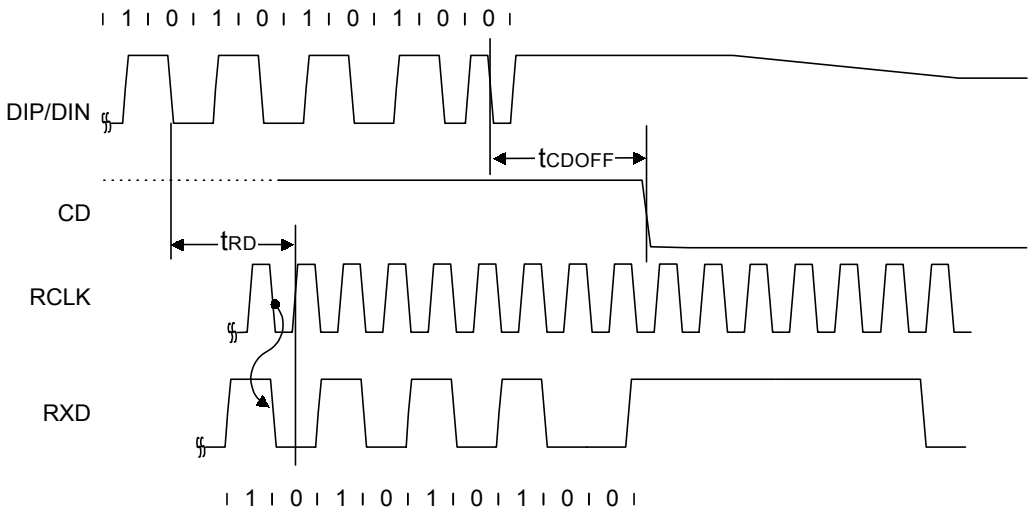
Timing Diagrams for Mode 4 (MD1 = High, MDO = High)

Figure 21: Mode 4 RCLK/Start of Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 22: Mode 4 RCLK/End of Frame Timing



NOTE: 1. RXD changes at the falling edge of RCLK. The controller is sampled at the rising edge.

Figure 23: Mode 4 Transmit Timing

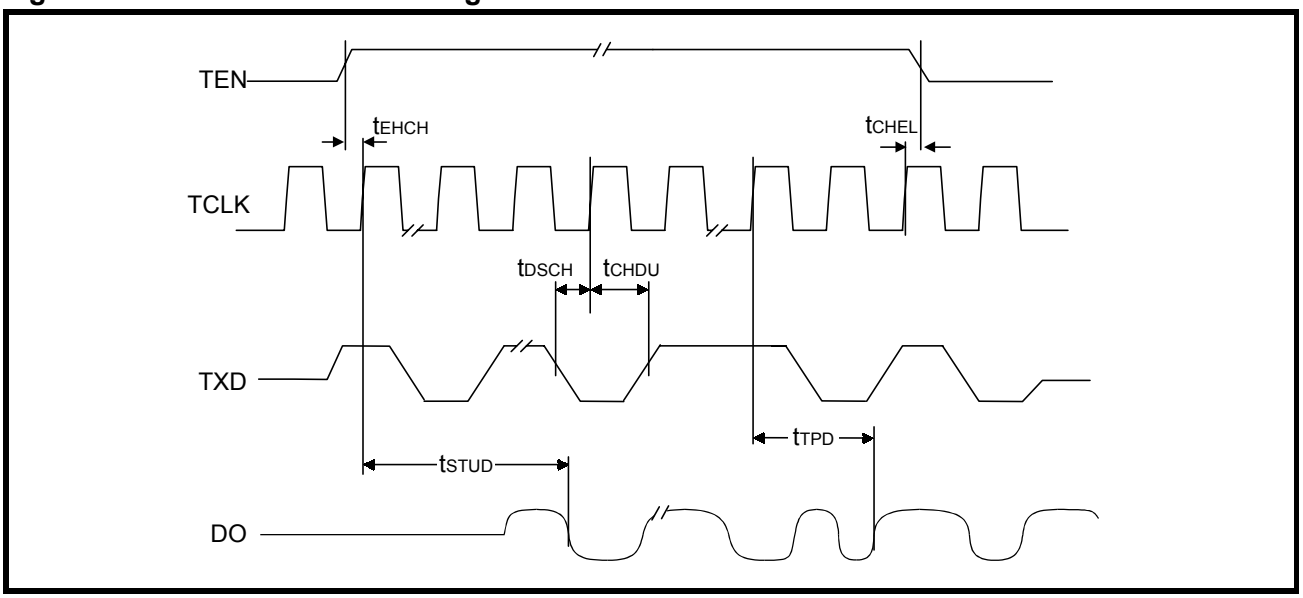


Figure 24: Mode 4 Collision Detect Timing

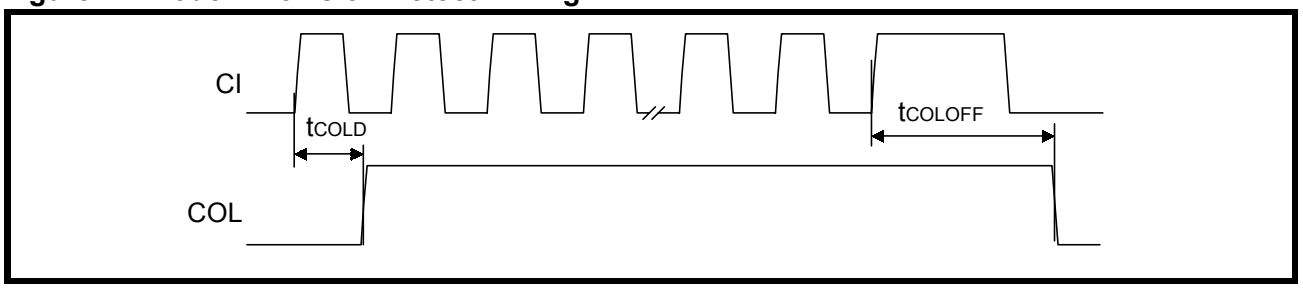


Figure 25: Mode 4 COL/CI Output Timing

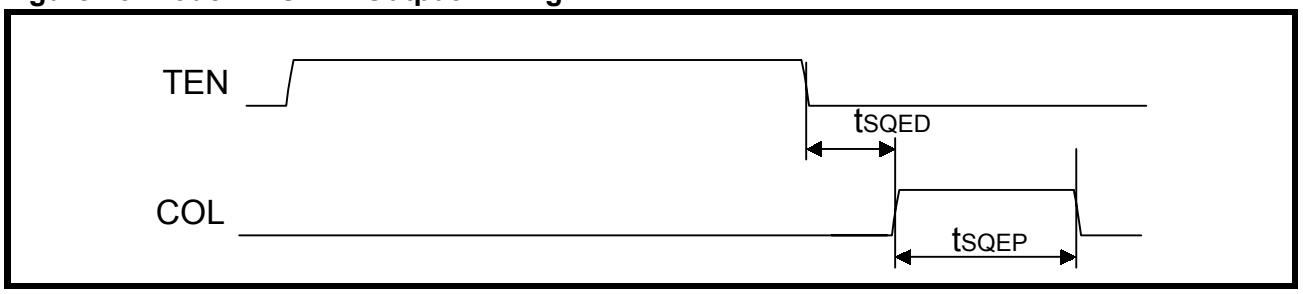
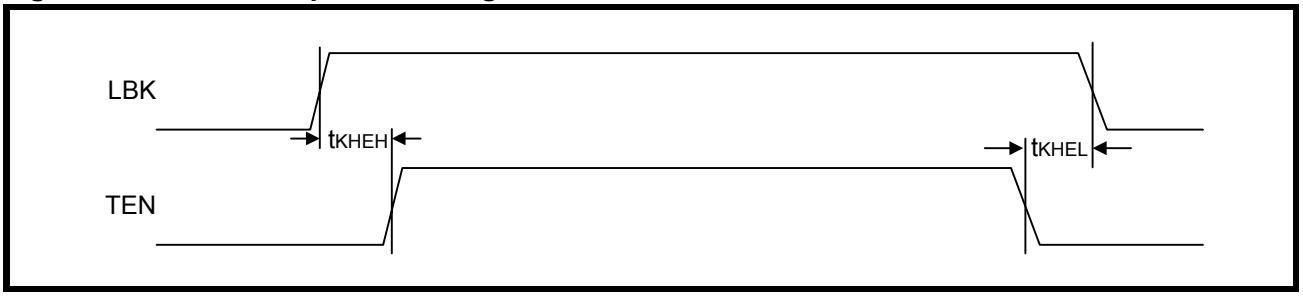


Figure 26: Mode 4 Loopback Timing



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