LZ93B53

Synchronous Signal Generator for CCD

DESCRIPTION

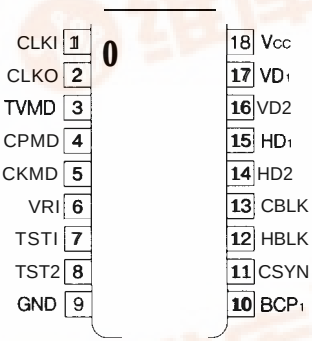
The LZ93B53 is a CMOS synchronous signal generator LSI which provides B/W TV synchronous pulses and video signal processing pulses, in combination with the timing signal generator LSI (LZ93N61, LZ95F50, or LZ93F33).

FEATURES

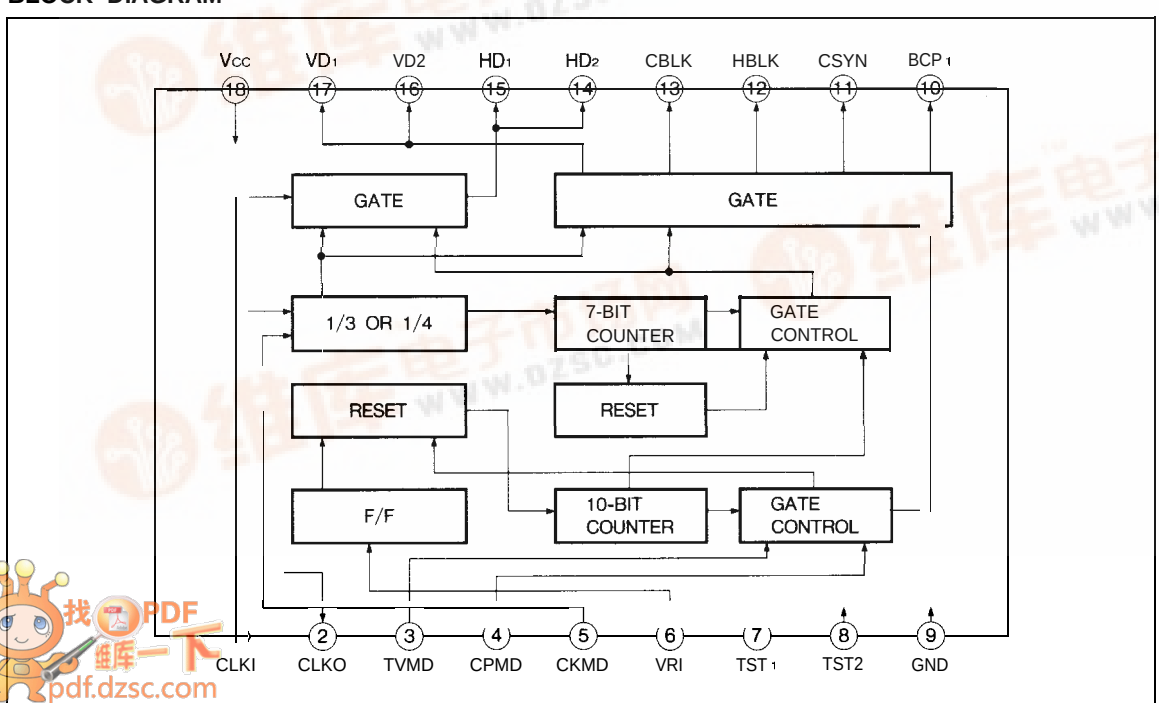
- Switchable between 270000 pixels B/W CCD and 320000 pixels B/W CCD
- Switchable between EIA and CCIR systems
- Single + 5 V power supply
- External synchronization is possible
- Package : 1 8-pin MFP(MFPOI 8-P)

PIN CONNECTIONS

18-PIN MFP TOP VIEW



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power voltage	V_{CC}	– 0.3 to 7.0	V
Input voltage	VI	-0.3 to V_{CC} + 0.3	V
Output voltage	Vo	– 0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	–20 to +70	°C
Storage temperature	Tstg	–55 to +150	°C

DC CHARACTERISTICS

(V_{CC} = +5 V ± 10%, Ta = –20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Low level input voltage	V_{IL}				1.5	V	1
High level input voltage	V_{IH}		3.5			V	
High level threshold voltage	V_{T+}	Schmitt buffer			3.7	V	2
Low level threshold voltage	V_{T-}	Schmitt buffer	1.0			V	
Hysteresis voltage	$V_{T+} - V_{T-}$	Schmitt buffer	0.4			V	
Low level output voltage	V_{OL}	I_{OL} = 4 mA			0.4	V	3
High level output voltage	V_{OH}	I_{OH} = –2 mA	4.0			V	
Low level input current	$\lvert I_{IL1} \rvert$	V_I = 0 V			1.0	μA	4
Low level input current	$\lvert I_{IL2} \rvert$	V_I = 0 V	8.0		60	μA	5
High level input current	$\lvert I_{IH1} \rvert$	V_I = V_{CC}			1.0	μA	6
High level input current	$\lvert I_{IH2} \rvert$	V_I = V_{CC}	8.0		60	μA	7

NOTES :

1. Applied to inputs (IC, ICU, ICD).
2. Applied to input (ICSU).
3. Applied to all outputs (0).
4. Applied to inputs (IC, ICU, ICSU).
5. Applied to input (ICD).
6. Applied to inputs (IC, ICD).
7. Applied to inputs (ICU, ICSU).

PIN FUNCTION

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I/O</th><th>POLARITY</th><th>PIN NAME</th><th>FUNCTION</th></tr>
<tr><td>1</td><td>CLKI</td><td>I C</td><td>⊓⊔</td><td>Main clock</td><td>This is a pin to input the clock which is used as the reference of the horizontal and vertical pulses. This pin should be connected to DO on the timing LSI. The frequency varies depending on CKMD (pin 5) as follows.
● EIA system
270000 pixels fck : 9.534964 MHz(606 fH)
360000 pixels fck : 12.713285 MHz(808 fH)
. CCIR system
320000 pixels fck : 9,656250 MHz(6I 8 fH)
420 000 pixels fck : 12.875000 MHz(824 fH)</td></tr>
<tr><td>2</td><td>CLKO</td><td>0</td><td>⊓⊓</td><td>Clock out</td><td>This is an inverted output pin for CLKI (pin 1).</td></tr>
<tr><td>3</td><td>TVMD</td><td>ICD</td><td>–</td><td>TV mode select</td><td>This is a pin to select TV systems.
● Low level : EIA system
● High level : CCIR system</td></tr>
<tr><td>4</td><td>CPMD</td><td>ICU</td><td>–</td><td>Clamp pulse mode select</td><td>This is a pin to control stop and continuance of BCPI (pin 10) within the vertical blanking period.
● High level : BCPI outputs continuous pulses.
● Low level : BCP ı stops outputting composite pulses while there is no effective pixel within the V blanking period.</td></tr>
<tr><td>5</td><td>CKMD</td><td>ICU</td><td>–</td><td>Clock mode select</td><td>This is an input pin to switch the frequency devision in accordance with the area sensor as follows.
<table>
<tr><th>Frequency division output</th><th>1/3</th><th>1/4</th></tr>
<tr><td>CKMD</td><td>High</td><td>Low</td></tr>
<tr><td>Number of pixels</td><td>270000</td><td>360000</td></tr>
</table></td></tr>
<tr><td>6</td><td>VRI</td><td>ICSU</td><td>u</td><td>Vertical reset</td><td>This is an input pin for the external V reset pulse which is used to apply vertical synchronization to the counter (2 fck counter) on the synchronization. This resetting takes priority over the internal reset-ting. Since the rise of input at VRI is taken at the horizontal synchronous frequency (2 fH) which is two times as high as the internal frequency, when the vertical pulses which were separated in terms of frequency from the composite synchronous signal from other equipment are used, the fall must have a phase difference of less than 1/2 fH compared with the start timing of the vertical synchronous signal. When the interal synchronization is obtained, the High level should be selected. The input is de-signed as a schmitt trigger buffer.</td></tr>
<tr><td>7</td><td>TST1</td><td>ICD</td><td>–</td><td>Test tarminal 1</td><td>This is an input pin for tests, Typically, this pin should be open or at the Low level.</td></tr>
</table>

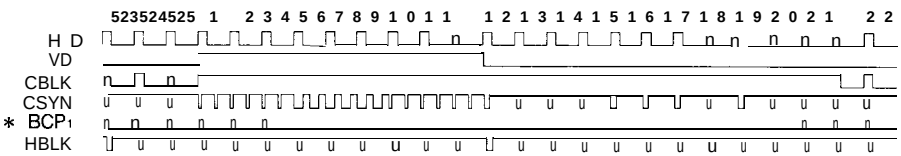
PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
8	TST2	ICD		Test tarminal 2	This is an input pin for tests. Typically, this pin should be open or at the Low level.
9	GND	–		Ground	This is a grounding pin.
10	BCP1	0		Optical block clamp pulse	This pin output pulse which is used to clamp optical black on each line of the sensor output, Typically, these are horizontal synchronization continuous pulses. However, setting CPMD (pin 4) to the Low level allows the composite output which becomes the Low level while there is no effective pixel within the vertical blanking period.
11	CSYN	0		Composite synchronous signal	This pin outputs EIA and CCIR standard composite synchronous signals. ● EIA system : Compatible with RS-170 . CCIR system : Compatible with CCIR
12	HBLK	0		Horizontal blanking pulse	This pin outputs a pulse to stop the horizontal transfer pulses which drive the horizontal register in the area sensor.
13	CBLK	0		Composite blanking pulse	This pin outputs pulses which are used for video blanking in the encoder. . EIA system : 11.01 μs, V20 H is cleared. . CCIR system : 12.12 μs, V25 H is cleared.
14	HD2	0		Horizontal drive pulse 2	This pin outputs pulses which are synchronous with the start of each line and used as the H reference of the timing LSI.
15	HDI	0		Horizontal drive pulse 1	This pin outputs pulses which are synchronous with the start of each line and used as the H reference of external equipment.
16	VD2	0		Vertical drive pulse 2	This pin outputs pulses which are obtained at the start of each field and used as the V reference of the timing LSI.
17	VDI	0		Vertical drive pulse 1	This pin outputs pulses which are obtained at the start of each field and used as the V reference of external equipment.
18	Vcc	–	–	Power supply	supply +5 V power

IC : Input Din (CMOS level).
ICU : Input pin (CMOS level with pull-up resistor).
ICD : Input pin (CMOS level with pull-down resistor).
ICSU : Schmitt-trigger input pin (CMOS level with pull-up resistor)
0 : Output pin

TIMING DIAGRAM

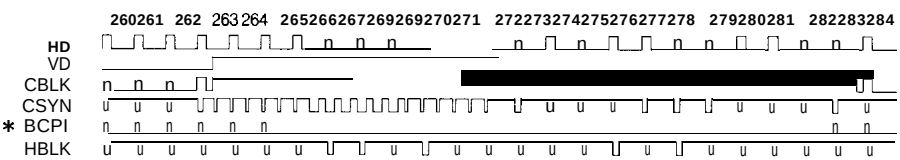
VERTICAL TIMING < EIA >

(ODD FIELD)



* CPMD = L

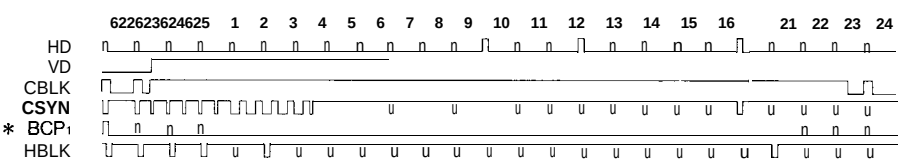
(EVEN FIELD)



* CPMD=L

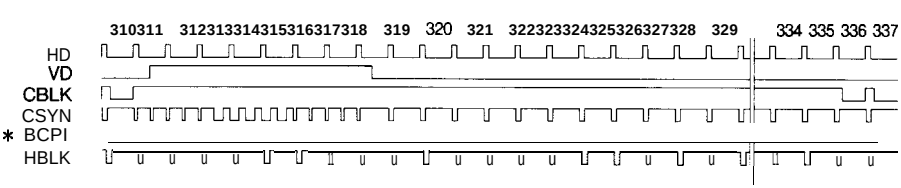
VERTICAL TIMING < CCIR >

(1st, 3rd FIELD)



* CPMD=L

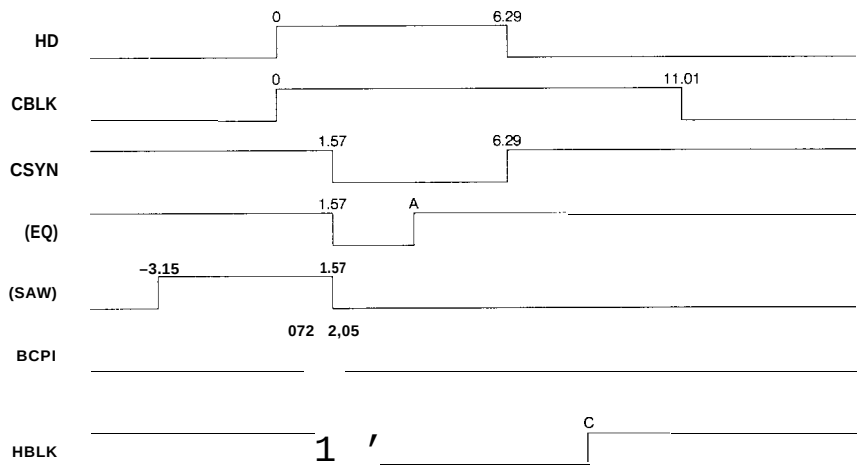
(2nd, 4th FIELD)



* CPMD = L

HORIZONTAL TIMING < EIA >

Unit : μS

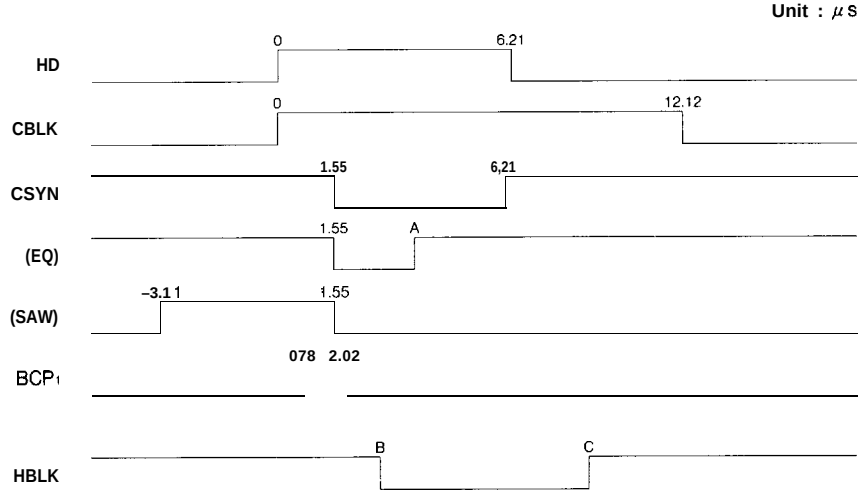


NOTES :

- Applied to the CCD of 542 horizontal pixels (CKMD = H) : A= 3.88, B =2.94, C =8.60
- Applied to the CCD of 726 horizontal pixels (CKMD = L) : A=3.93, B =2.91, C =8.57

HORIZONTAL TIMING < CCIR>

Unit : μS



NOTES :

- Applied to the CCD of 542 horizontal pixels (CKMD = H) : A =3.83, B =2.90, C= 9.73
- Applied to the CCD of 726 horizontal pixels (CKMD = L) : A =3.88, B =2.87, C=9.70