BURR - BROWN®

HDCD®

PCM1732

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SoundPLUS™ 24-Bit, 96kHz, Stereo Audio DIGITAL-TO-ANALOG CONVERTER With HDCD® Decoder

FEATURES

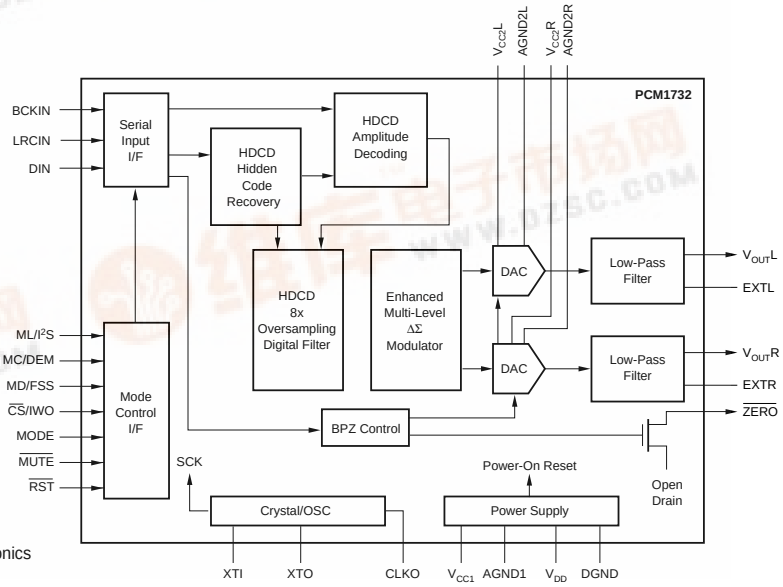
- ENHANCED MULTI-LEVEL ΔΣ DAC
- INPUT AUDIO DATA WORD: 16-, 20-, 24-Bit
- SAMPLING FREQUENCY (f_S): 16kHz - 96kHz
- SYSTEM CLOCK: 256, 384, 512, 768f_S
- HIGH PERFORMANCE:
  THD+N: –96dB
  Dynamic Range: 104dB
  SNR: 104dB
- AUDIO OUTPUT LEVEL: 0.57 x V_{CC} (Vp-p)
- 8x OVERSAMPLING DIGITAL FILTER WITH HDCD DECODER:
  Stopband Attenuation: –120dB
  Passband Ripple: ±0.00001dB
  HDCD Filter Optimized for 44.1kHz to 48kHz and 88.2kHz to 96kHz
- MULTI-FUNCTIONS:
  Digital De-emphasis
  Soft Mute
  Digital Attenuation
  Zero Detect
  Digital Gain Scaling
  Reversible Output Phase
- +5V SINGLE-SUPPLY OPERATION
- SMALL SO-28 PACKAGE

DESCRIPTION

The PCM1732 is designed for mid- to high-grade digital audio applications which achieve 96kHz sampling rates with 24-bit audio data, such as High Definition Compatible Digital (HDCD) CD players, DVD players, mini-disc players and AV receivers.

PCM1732 uses a newly-developed “enhanced, multi-level delta-sigma modulator” architecture that improves audio dynamic performance and reduces jitter sensitivity.

The internal digital filter operates at 8x oversampling at a 96kHz sampling rate, with –120dB stopband attenuation.



NOTE: An HDCD license from Pacific Microsonics, Inc. is required to purchase the PCM1732.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

24-Bit Data Performance

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and SYSCLK = 384f_S, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1732 MIN	PCM1732 TYP	PCM1732 MAX	UNITS
RESOLUTION		24		Bits	
DATA FORMAT					
Audio Data Interface Format			Standard/I²S		
Data Bit Length			16/20/24 Selectable		
Audio Data Format			MSB-First, Binary Two's Complement		
Sampling Frequency (f_S)		16		96	kHz
System Clock Frequency[1]			256/384/512/768f_S		
System Clock Duty Cycle		40		60	%
DIGITAL INPUT/OUTPUT LOGIC LEVEL					
Input Logic Level (except XTI): V_{IH}		2.0			V
V_{IL}				0.8	V
Output Logic Level (CLKO): V_{OH}	I_{OH} = 2mA	4.5			V
V_{OL}	I_{OL} = 4mA			0.5	V
CLKO PERFORMANCE[2]					
Output Rise Time	20 ~ 80% V_{DD}, 10pF		5.5		ns
Output Fall Time	80 ~ 20% V_{DD}, 10pF		4		ns
Output Duty Cycle	10pF Load		30		%
DYNAMIC PERFORMANCE[3, 4]					
THD+N V_O = 0dB	f_S = 44.1kHz		–96	–90	dB
	f_S = 96kHz		–94		dB
V_O = –60dB	f_S = 44.1kHz		–42		dB
Dynamic Range	f_S = 44.1kHz, EIAJ A-weighted	98	104		dB
	f_S = 96kHz, A-weighted		103		dB
Signal-to-Noise Ratio[5]	f_S = 44.1kHz, EIAJ A-weighted	98	104		dB
	f_S = 96kHz, A-weighted		103		dB
Channel Separation	f_S = 44.1kHz	96	104		dB
	f_S = 96kHz		101		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch Channel-to-Channel			±1.0	±3.0	% of FSR
Bipolar Zero Error	V_O = 0.5V_{CC} at Bipolar Zero		±30	±60	mV
ANALOG OUTPUT					
Output Voltage[6]	Full Scale (0dB)		0.57 V_{CC}		Vp-p
Center Voltage			0.5 V_{CC}		V
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Filter Characteristics 1					
(f_S = 44.1kHz/48kHz optimal)					
Passband	±0.002dB			0.471f_S	
	–3dB			0.487f_S	
Stopband		0.515f_S			
Passband Ripple	< 0.453f_S			±0.0001	dB
Stopband Attenuation	Stopband = 0.515f_S	–109			dB
	Stopband = 0.520f_S	–123			dB
Delay Time			81/f_S		sec
Filter Characteristics 2					
(f_S = 88.2kHz/96kHz optimal)					
Passband	±0.005dB			0.395f_S	
	–3dB			0.441f_S	
Stopband		0.538f_S			
Passband Ripple	< 0.341f_S			±0.0001	dB
Stopband Attenuation	Stopband = 0.538f_S	–132			dB
Delay Time			31/f_S		sec
De-Emphasis Error				±0.1	dB
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{CC}	4.5	5	5.5	VDC
Supply Current: I_{CC} + I_{DD}	f_S = 44.1kHz		85	105	mA
	f_S = 96kHz		93		mA
Power Dissipation	f_S = 44.1kHz		425	525	mW
	f_S = 96kHz		465		mW
TEMPERATURE RANGE					
Operating		–25		+70	°C
Storage		–55		+100	°C
Thermal Resistance, θ_{JA}			67		°C/W

NOTES: (1) Refer to the System Clock section of this data sheet. (2) An external buffer is recommended. (3) Dynamic performance specifications are tested with 20kHz low-pass filter and THD+N specifications are tested with 30kHz LPF, 400Hz HPF, Average Mode. (4) Dynamic performance specifications are tested with HDCD gain scaling set to analog gain scaling. (5) SNR is tested with infinite zero detection off. (6) Output level is for sine wave. DAC outputs 0.64 V_{CC} (peak-to-peak) due to filter response as transient.

SPECIFICATIONS

16-Bit Data Performance

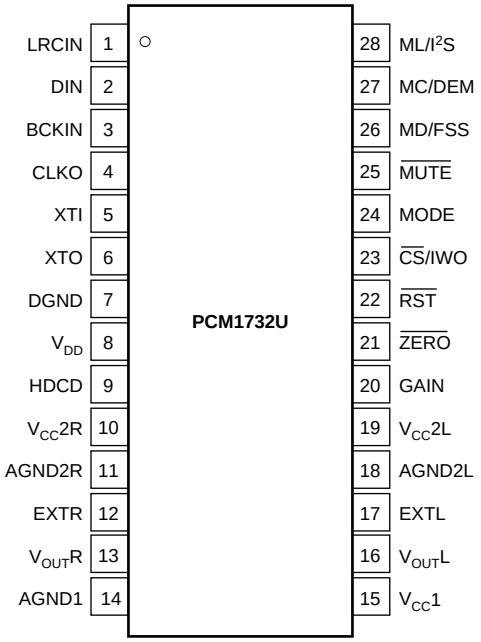
All specifications at +25°C, $+V_{DD}$ = $+V_{CC}$ = +5V, f_S = 44.1kHz, and SYSCLK = 384f_S, unless otherwise noted. For discussion of HDCD scaling options, see the Applications Considerations section of this data sheet.

PARAMETER	CONDITIONS	PCM1732U			UNITS
		MIN	TYP	MAX	
DYNAMIC ANALOG PERFORMANCE, STANDARD CD, ANALOG HDCD SCALING(1)					
Total Harmonic Distortion + Noise					
V_O = 0dB	0dBFS		–95		dB
V_O = –60dB			–37		dB
Dynamic Range	EIAJ A-Weighted		99		dB
Output Voltage, Sine Wave	0dBFS(2)		0.57V_{CC}		Vp-p
DYNAMIC ANALOG PERFORMANCE, HDCD CD, ANALOG HDCD SCALING(3)					
Total Harmonic Distortion + Noise					
V_O = 0dB	0dBFS		–94		dB
V_O = –60dB			–38		dB
Dynamic Range	EIAJ A-Weighted(4)		104		dB
Output Voltage, Sine Wave	0dBFS, Without Peak Extend(2)		0.57V_{CC}		Vp-p
	0dBFS, With Peak Extend(5)		0.285V_{CC}		Vp-p
	+6dBFS(5, 6)		0.57V_{CC}		Vp-p
DYNAMIC ANALOG PERFORMANCE, Standard CD, Digital HDCD SCALING(1)					
Total Harmonic Distortion + Noise					
V_O = 0dB	0dBFS		–92		dB
V_O = –60dB			–33		dB
Dynamic Range	EIAJ A-Weighted		96		dB
Output Voltage, Sine Wave	0dBFS		0.285V_{CC}		Vp-p
DYNAMIC ANALOG PERFORMANCE HDCD CD, Digital HDCD SCALING(2)					
Total Harmonic Distortion + Noise					
V_O = 0dB	0dBFS		–91		dB
V_O = –60dB			–34		dB
Dynamic Range	EIAJ A-Weighted(4)		104		dB
Output Voltage, Sine Wave	0dBFS		0.285V_{CC}		Vp-p
	+6dBFS(5)		0.57V_{CC}		Vp-p

NOTES: (1) Without dither. (2) Gain pin is LOW. (3) With the rectangular PDF dither. (4) Including Peak Extend to +6dBFS. (5) Gain pin is HIGH. (6) +6dBFS is the full Peak Extend, while dynamic range numbers are with Peak Extend.

PIN CONFIGURATION

Top View **SO-28**



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Input Current (except power supply)	±10mA
Power Dissipation	750mW
Operating Temperature Range	–25°C to +70°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
(reflow, 10s)	+235°C

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	LRCIN	IN	Left and Right Clock Input. This clock is equal to the sampling rate, f_S.(1)
2	DIN	IN	Serial Audio Data Input(1)
3	BCKIN	IN	Bit Clock Input for Serial Audio Data(1)
4	CLKO	OUT	Buffered System Clock Output.
5	XTI	IN	Oscillator Input/External Clock Input(2)
6	XTO	OUT	Oscillator Output
7	DGND	—	Digital Ground
8	V_{DD}	—	Digital Power +5V
9	HDCD	OUT	HDCD Encoded Data Detect
10	V_{CC}2R	—	Analog Power +5V, Rch
11	AGND2R	—	Analog Ground, Rch
12	EXTR	—	Common Mode Voltage for Analog Output Amp, Rch
13	V_{OUT}R	OUT	Analog Voltage Output, Rch
14	AGND1	—	Analog Ground
15	V_{CC}1	—	Analog Power +5V
16	V_{OUT}L	OUT	Analog Voltage Output, Lch
17	EXTL	—	Common Mode Voltage for Analog Output Amp, Lch
18	AGND2L	OUT	Analog Ground, Lch
19	V_{CC}2L	—	Analog Power +5V, Lch
20	GAIN	OUT	External (analog) Gain Scaling
21	$\overline{\text{ZERO}}$	OUT	Zero Data Flag
22	$\overline{\text{RST}}$	IN	Reset. When this pin is LOW, the digital filter and modulators are held in reset.(3)
23	$\overline{\text{CS}}$/IW0	IN	Chip Select/Input Format Selection. When this pin is LOW, the Mode Control interface is enabled.(4)
24	MODE	IN	Mode Control Select: H = Software; L = Hardware(3)
25	$\overline{\text{MUTE}}$	IN	Mute Control(3)
26	MD/FSS	IN	Mode Data/Sampling Rate Range Select(3)
27	MC/DEM	IN	Mode Clock/De-Emphasis Select(3)
28	ML/I2S	IN	Mode Latch/Input Format Select(3)

NOTES: (1) Schmitt Trigger input. (2) CMOS logic level input. (3) Schmitt Trigger input with pull-up resister. (4) Schmitt Trigger input with pull-down resistor.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
PCM1732U	SO-28	217	–25°C to +70°C	PCM1732U	PCM1732U	Rails
"	"	"	"	"	PCM1732U/1K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "PCM1732U/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

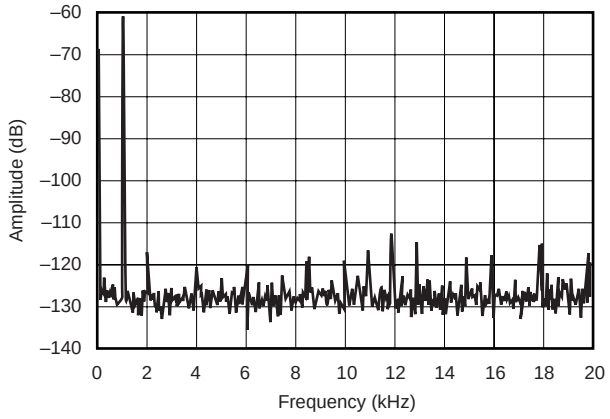
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

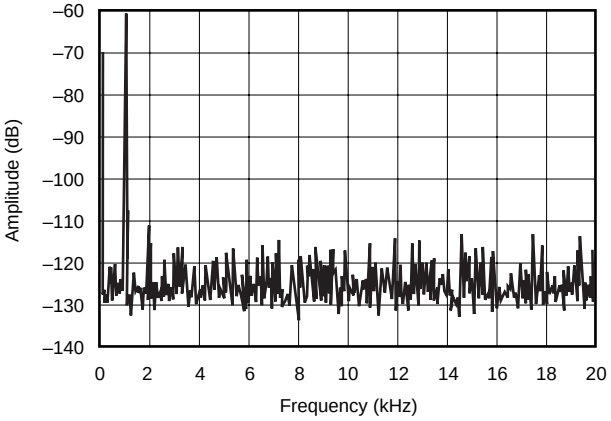
TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

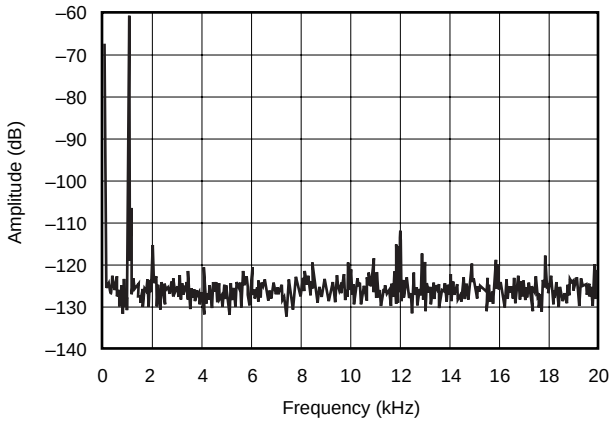
–60dB AMPLITUDE vs FREQUENCY
24-Bit Data



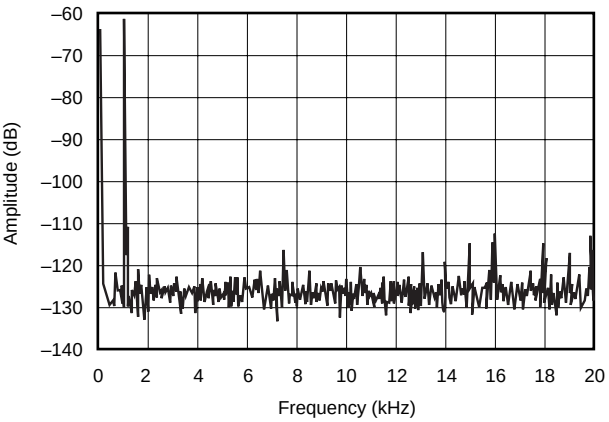
–60dB AMPLITUDE vs FREQUENCY
16-Bit Data



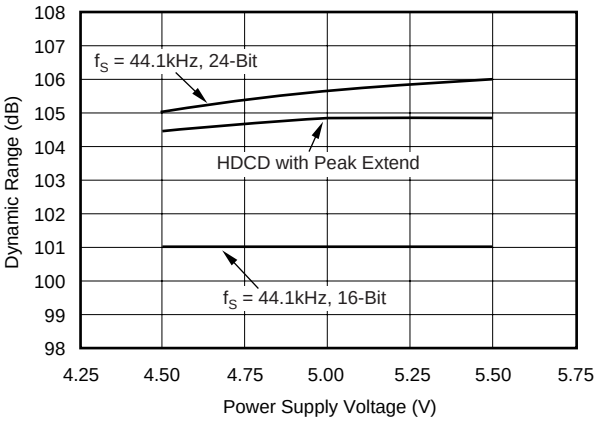
–60dB AMPLITUDE vs FREQUENCY
HDCD Without Peak Extend



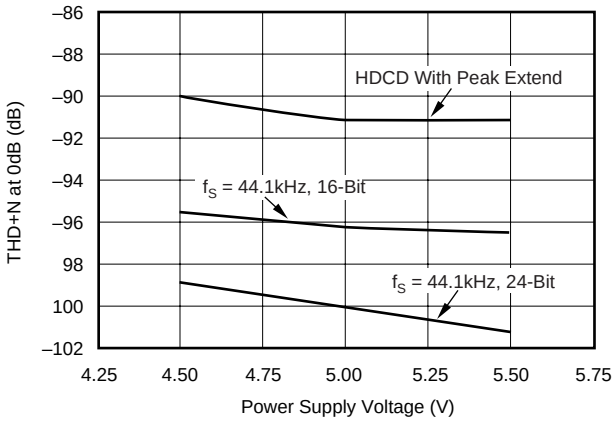
–60dB AMPLITUDE vs FREQUENCY
HDCD With Peak Extend



DYNAMIC RANGE vs SUPPLY VOLTAGE

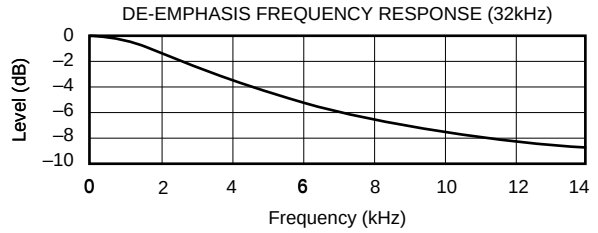


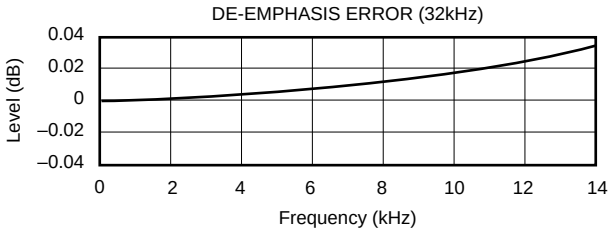
THD+N vs SUPPLY VOLTAGE

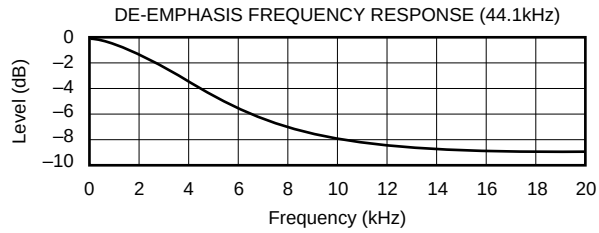


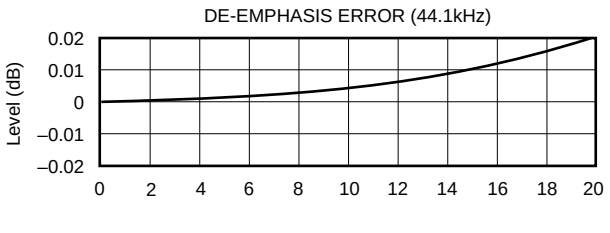
TYPICAL PERFORMANCE CURVES

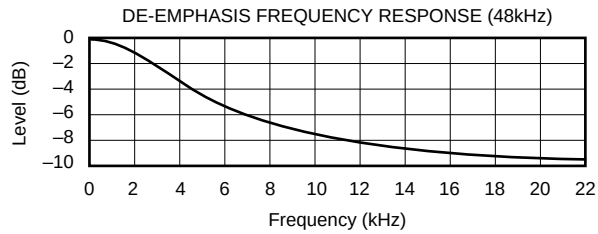
DIGITAL FILTER

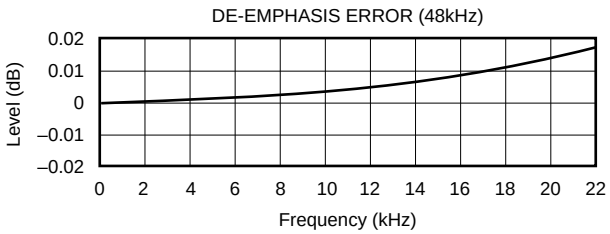


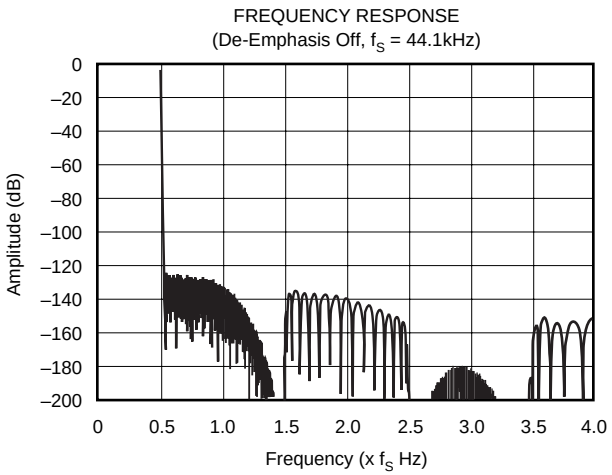


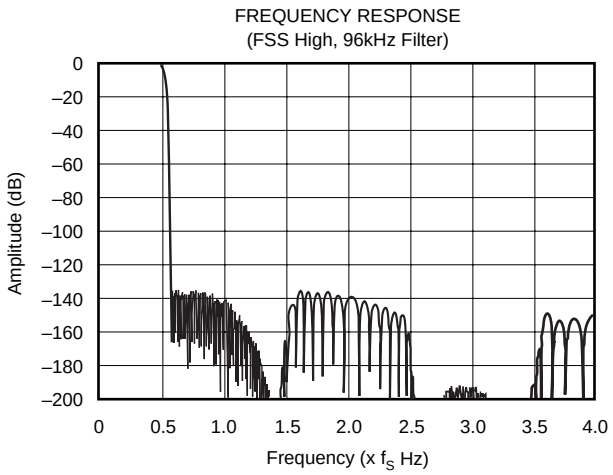


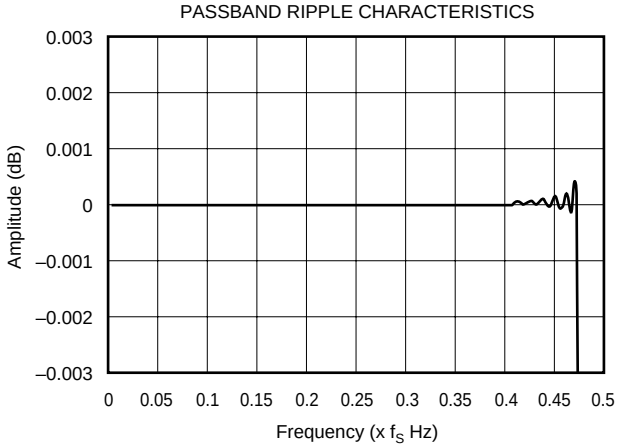












SYSTEM CLOCK

The system clock for PCM1732 must be either $256f_S$, $384f_S$, $512f_S$ or $768f_S$, where f_S is the audio sampling frequency (typically 32kHz, 44.1kHz, 48kHz, 88kHz, or 96kHz). A $768f_S$ system clock is not supported for 88.2kHz and 96kHz sampling frequencies.

The system clock can be either a crystal oscillator placed between XTI (pin 5) and XTO (pin 6), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1732 has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$ ~ $768f_S$. The system clock should be synchronized with the left/right clock (LRCIN, pin 1). LRCIN operates at the sampling frequency (f_S). In the event these clocks are not synchronized, the PCM1732 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6-bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

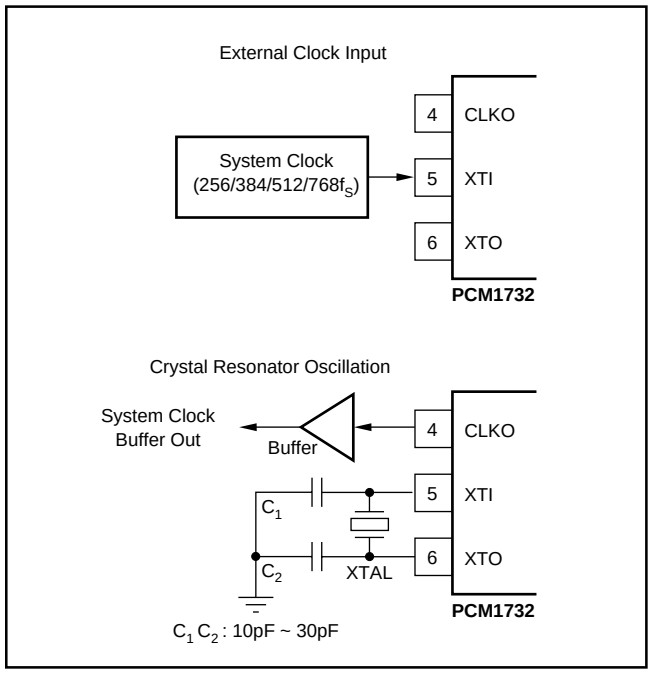


FIGURE 1. System Clock Connection.

Typical input system clock frequencies to the PCM1732 are shown in Table I and external input clock timing requirements are shown in Figure 2.

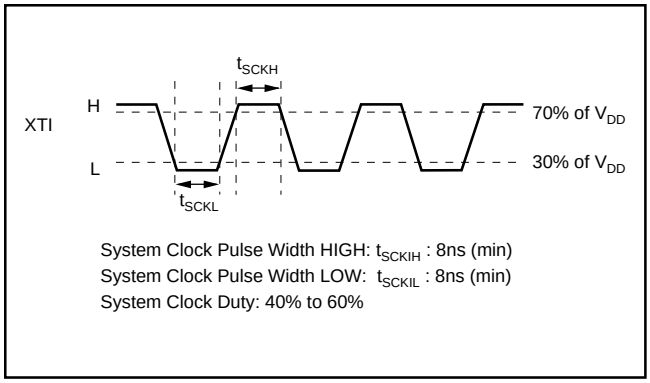


FIGURE 2. XTI Clock Timing.

DATA INTERFACE FORMATS

Digital audio data is interfaced to the PCM1732 on pin 1 (LRCIN), pin 2 (DIN), and pin 3 (BCKIN). The PCM1732 can accept standard, I^2S, and left-justified data formats.

Figure 3 illustrates acceptable input data formats. Figure 4 shows required timing specifications for digital audio data.

Reset

PCM1732 has both an internal power-on reset circuit and a $\overline{RST}$ pin (pin 22), which accepts an external reset when $\overline{RST}$ = LOW. For internal power-on reset, initialization (reset) is done automatically at power-on when V_{DD} > 2.2V (typical). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 5 illustrates the timing of the internal power-on reset.

PCM1732 accepts an external forced reset when $\overline{RST}$ = LOW. When $\overline{RST}$ = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialization (1024 system clocks count after $\overline{RST}$ = HIGH.) Figure 6 illustrates the timing of the $\overline{RST}$ pin.

Zero Out (pin 21)

Zero is an open drain output. If the input data is continuously zero for 65,536 cycles of BCKIN, an internal FET is switched to "ON" and the drain of the internal FET is switched to ground. The zero detect function is available in both software mode and hardware mode.

SAMPLING RATE FREQUENCY (f_S)	SYSTEM CLOCK FREQUENCY (MHz)			
	$256f_S$	$384f_S$	$512f_S$	$768f_S$
32kHz	8.1920	12.2880	16.3840	24.5760
44.1kHz	11.2896	16.9340	22.5792	33.8688(1)
48kHz	12.2880	18.4320	24.5760	36.8640(1)
88.2kHz	22.5792	33.8688(1)	45.1584(1)	—
96kHz	24.5760	36.8640(1)	49.1520(1)	—

NOTE: (1) The internal crystal oscillator frequency cannot be larger than 24.576MHz.

TABLE I. Typical System Clock Frequencies.

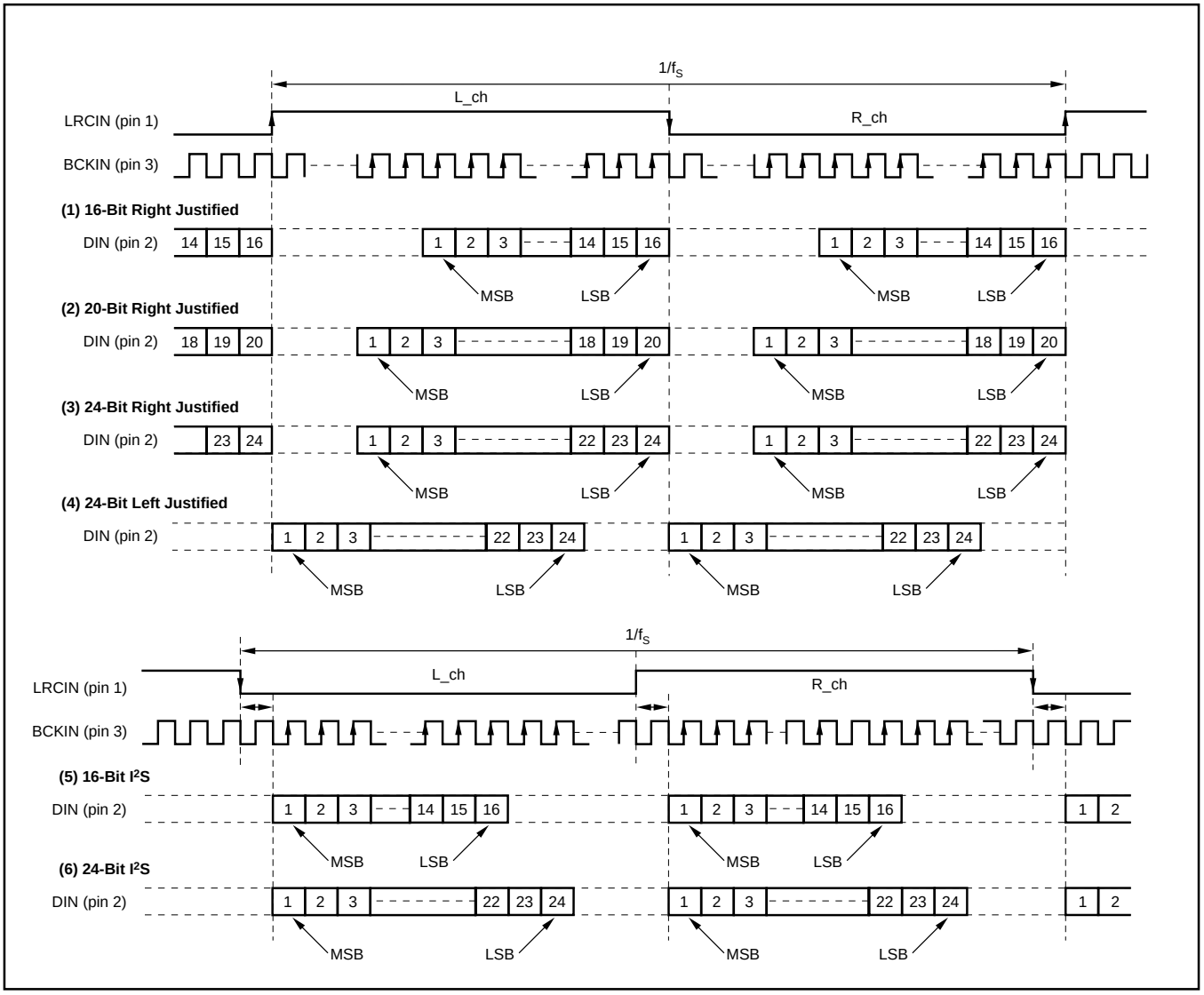
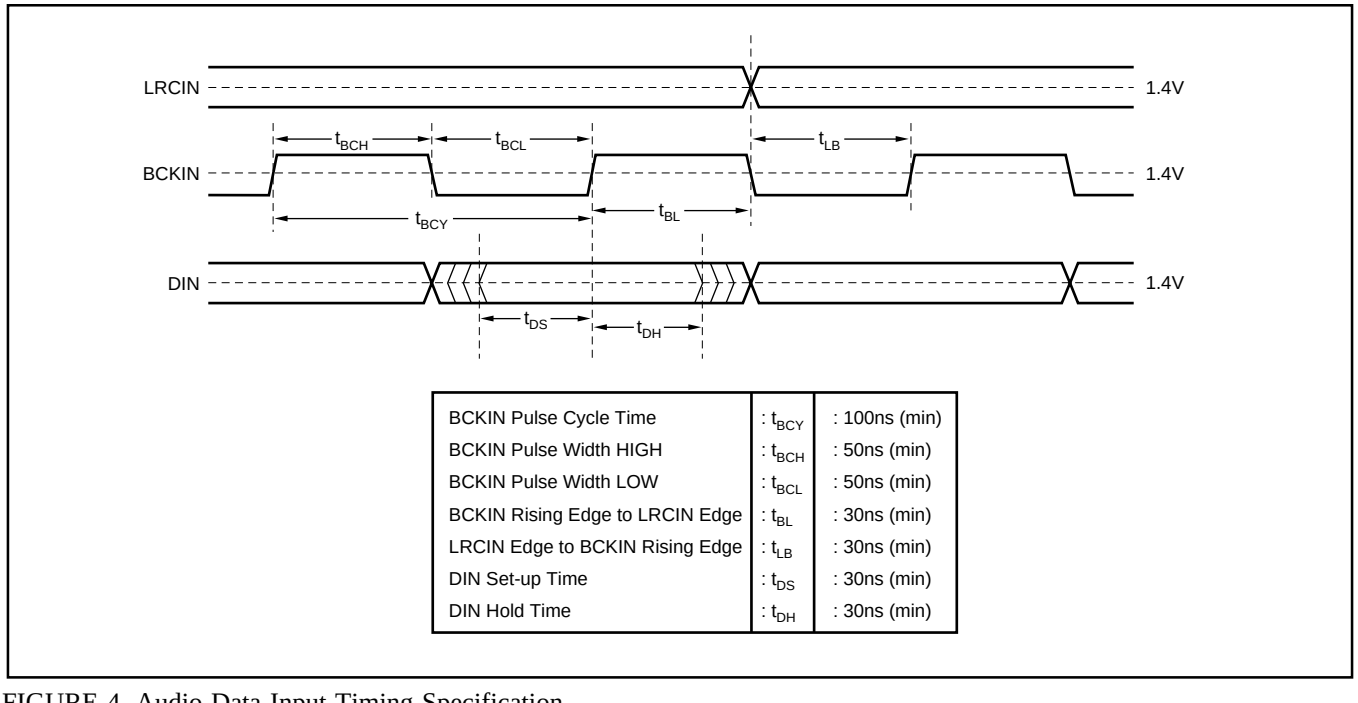


FIGURE 3. Audio Data Input Formats.



BCKIN Pulse Cycle Time	: t_{BCY}	: 100ns (min)
BCKIN Pulse Width HIGH	: t_{BCH}	: 50ns (min)
BCKIN Pulse Width LOW	: t_{BCL}	: 50ns (min)
BCKIN Rising Edge to LRCIN Edge	: t_{BL}	: 30ns (min)
LRCIN Edge to BCKIN Rising Edge	: t_{LB}	: 30ns (min)
DIN Set-up Time	: t_{DS}	: 30ns (min)
DIN Hold Time	: t_{DH}	: 30ns (min)

FIGURE 4. Audio Data Input Timing Specification.

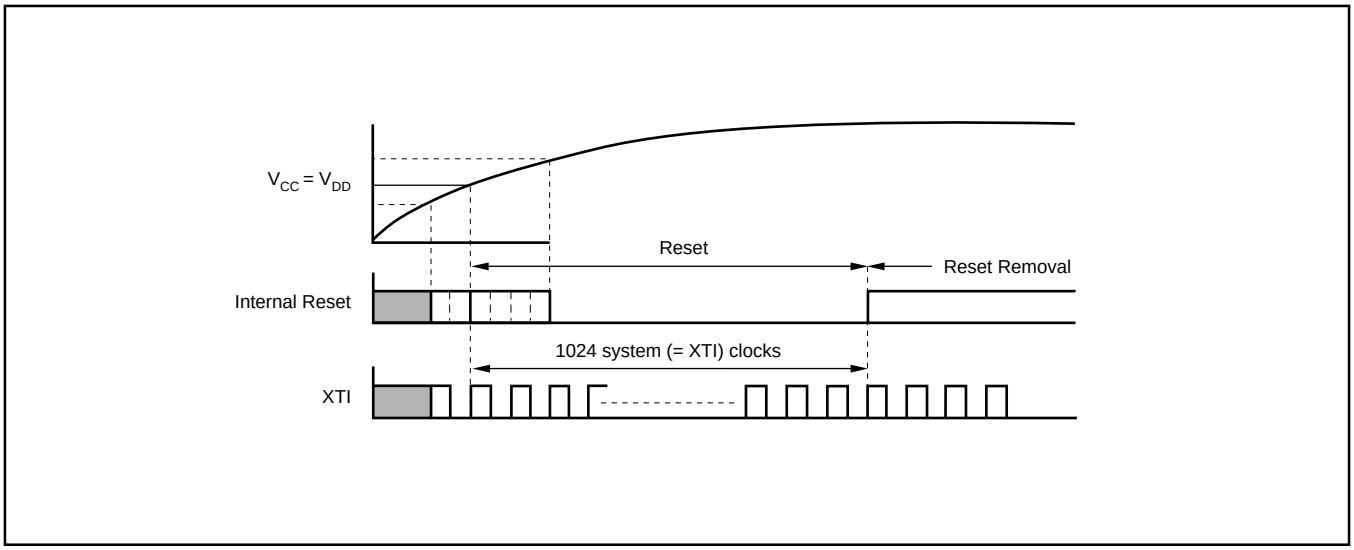


FIGURE 5. Internal Power-On Reset Timing.

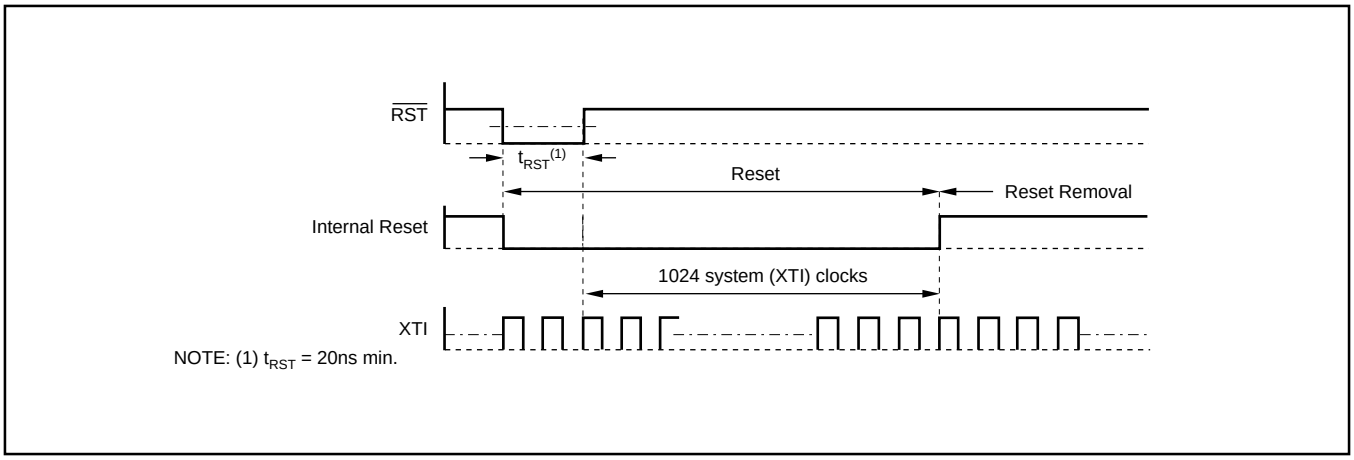


FIGURE 6. External Reset Timing.

FUNCTIONAL DESCRIPTION

The PCM1732 can be operated in two different modes: software or hardware mode. Software mode is a three-wire interface using pin 28 (ML), pin 27 (MC), and pin 26 (MD).

PCM1732 can also be operated in hardware mode, where static control signals are used on pin 28 (ML), pin 27 (DEM), pin 26 (FSS) and pin 23 (IWO).

The mode of operation (software or hardware) is selected by pin 24 (MODE), as shown in Table II.

CONTROL MODE (Pin 24)	SELECTION
H	Software
L	Hardware

TABLE II. Mode Control.

Table III indicates which functions are selectable within the chosen mode. All of the functions shown are selectable within the Software mode, but only de-emphasis control, soft mute and input data format may be selected when using PCM1732 in the Hardware mode.

FUNCTION	SOFTWARE (Mode = H)	HARDWARE (Mode = L)
Input Data Format Selection	O	P
Input Data Bit Selection	O	P
Input LRCIN Polarity Selection	O	X
Sampling Frequency Range	O	O
De-Emphasis Control	O	P
Mute	O	O
Attenuation	O	X
Infinity Zero Mute Control	O	X
DAC Operation Control	O	X
Output Phase Selection	O	X
CLKO Output Selection	O	X

NOTE: O = selectable, X = not selectable, P = partially selectable.

TABLE III. Mode Control, Selectable Functions.

HARDWARE MODE (MODE = L)

In Hardware mode, the following functions can be selected:

De-Emphasis Control

De-emphasis control can be selected by DEM (pin 26).

DEM (Pin 26)	DE-EMPHASIS
L	OFF
H	Mute OFF (Normal Operation)

TABLE IV. De-Emphasis Control.

Sampling Rate Range Selection

The sampling rate range must be selected by FSS (pin 26) as $f_S \leq 52kHz$ or $f_S > 52kHz$.

FSS (Pin 26)	SAMPLE RATE
L	$f_S \leq 52kHz$
H	$f_S > 52kHz$

TABLE V. Sampling Rate Range Select.

Input Audio Data Format

Input Data format can be selected by I²S (pin 28) and IW0 (pin 23).

I²S (Pin 28)	IWO (Pin 23)	DATA FORMAT
L	L	16-Bit Data Word, Normal, Right-Justified
L	H	20-Bit Data Word, Normal, Right-Justified
H	L	16-Bit Data Word, I²S Format
H	H	24-Bit Data Word, I²S Format

TABLE VI. Data Format Control.

SOFT MUTE

The Soft Mute function can be controlled by $\overline{\text{MUTE}}$ (pin 25).

$\overline{\text{MUTE}}$ (Pin 25)	SOFT MUTE
L	Mute ON
H	Mute OFF (normal operation)

TABLE VII. Soft Mute Control.

SOFTWARE MODE (MODE = H)

The PCM1732's special functions in the Software mode are shown in Table VIII. These functions are controlled using a ML, MC, MD serial control signal.

FUNCTION	DEFAULT MODE
Input Audio Data Format Selection Standard Format Left-Justified I²S Format	Standard Format
Input Audio Data Bit Selection 16-Bit 20-Bit 24-Bit	16-Bit
Sampling Rate Range $f_S \leq 52kHz$ $f_S > 52kHz$	$f_S \leq 52kHz$
Input LRCIN Polarity Selection Lch/Rch = HIGH/LOW Lch/Rch = LOW/HIGH	Lch/Rch = HIGH/LOW
De-Emphasis Control	OFF
Soft Mute Control	OFF
Attenuation Control Lch, Rch Individually Lch, Rch Common	0dB, Individual
Infinite Zero Mute Control	Not Operated
DAC Operation Control	Operated
Sampling Rate Selection for De-Emphasis Standard Frequency 44.1kHz 48kHz 32kHz	44.1kHz
HDCD Hidden Code Bit Location Bits 16, 20, 22, 24	Bit 16
Output Phase Selection	Not Inverted
CLKO Output Selection	Input Frequency

TABLE VIII. Selectable Functions and Default.

PROGRAM REGISTER BIT MAPPING

PCM1732's special functions are controlled using four program registers which are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Figure 7 shows the complete mapping of the four registers and Figure 8 illustrates the serial interface timing.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	res	res	A1	A0	CB1	CB0	SCA	FSS	IW1	IW0	OPE	DEM	MUT
MODE3	res	res	res	res	res	A1	A0	IZD	SF1	SF0	CK0	REV	res	ATC	LRP	I²S

FIGURE 7. Mode Register Mapping.

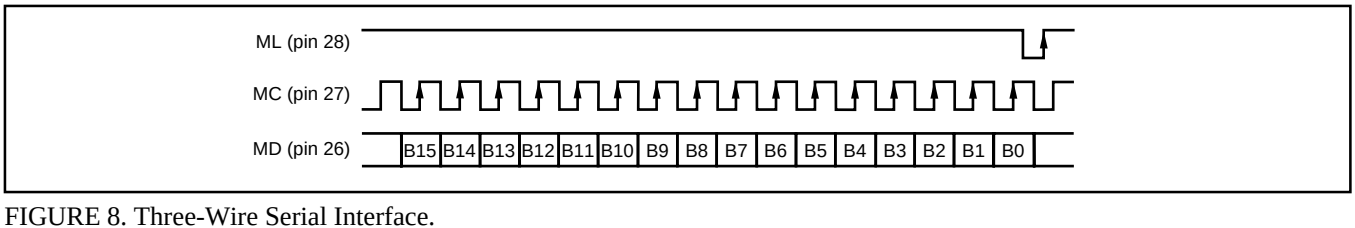
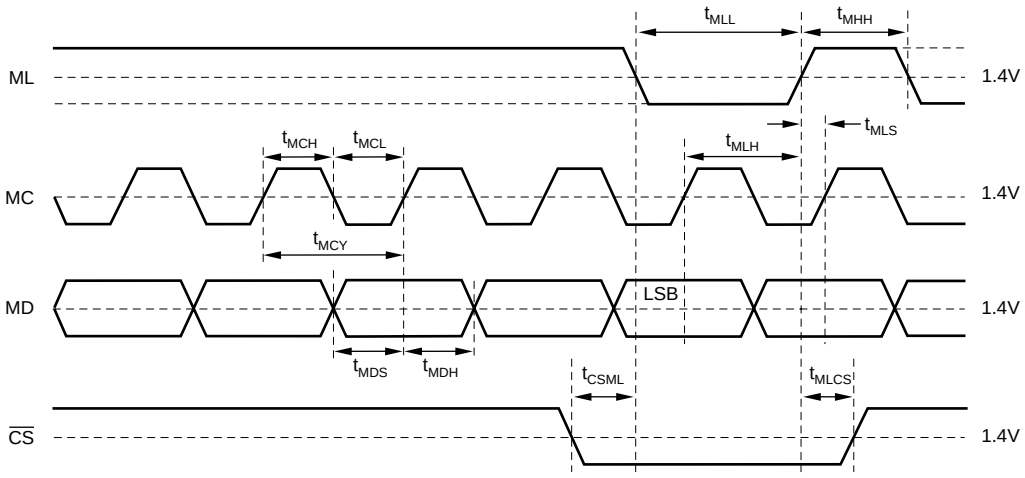


FIGURE 8. Three-Wire Serial Interface.



MC Pulse Cycle Time	: t_{MCY}	: 100ns (min)
MC Pulse Width LOW	: t_{MCL}	: 40ns (min)
MC Pulse Width HIGH	: t_{MCH}	: 40ns (min)
MD Hold Time	: t_{MDH}	: 40ns (min)
MD Set-up Time	: t_{MDS}	: 40ns (min)
ML Low Level Time	: t_{MLL}	: 40ns (min) + 1SYSCLK(1) (min)
ML High Level Time	: t_{MHH}	: 40ns (min) + 1SYSCLK(1) (min)
ML Hold Time	: t_{MLH}	: 40ns (min)
ML Set-up Time	: t_{MLS}	: 40ns (min)
$\overline{CS}$ LOW to ML LOW Time(2)	: t_{CSML}	: 10ns (min)
ML HIGH to $\overline{CS}$ HIGH Time(2)	: t_{MLCS}	: 10ns (min)

NOTES: (1) System Clock Cycle. (2) $\overline{CS}$ should be changed during ML = HIGH.

FIGURE 9. Program Register Input Timing.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	AL (7:0)	DAC Attenuation Data for Lch
	LDL	Attenuation Data Load Control for Lch
	A (1:0)	Register Address
	res	Reserved, set to LOW
Register 1	AR (7:0)	DAC Attenuation Data for Rch
	LDR	Attenuation Data Load Control for Rch
	A (1:0)	Register Address
	res	Reserved, set to LOW
Register 2	MUT	Left and Right DACs Soft Mute Control
	DEM	De-Emphasis Control
	OPE	Left and Right DACs Operation Control
	IW (1:0)	Input Audio Data Bit and Format Select
	FSS	Sampling Rate Range Select
	SCA	HDCD Grain Scaling Select
	C3 (1:0)	HDCD Hidden Code Location
	A (1:0)	Register Address
	res	Reserved, set to LOW
Register 3	I^2S	Audio Data Format Select
	LRP	Polarity of LRCIN Select
	ATC	Attenuator Control
	REV	Output Phase Select
	CKO	CLKO Output Select
	SF (1:0)	Sampling Rate Select
	IZD	Internal Zero Detection Circuit Control
	A (1:0)	Register Address
	res	Reserved, set to LOW

TABLE IX. Register Functions.

REGISTER 0 (A1 = 0, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to set the attenuation data for the left output channel.

When ATC = 1 (Bit B2 of Register MODE3 = 1), the left channel attenuation data AL[7:0] is used for both the left and right channel attenuators.

When ATC = 0, (Bit B2 of Register MODE3 = 0), left channel attenuation data is taken from AL[7:0] of register MODE0, and right channel attenuation data is taken from AR[7:0] of register MODE1.

AL[7:0] Left Channel Attenuator Data, where AL7 is the MSB and AL0 is the LSB.
Attenuation Level is given by:

ATTEN = 0.5 • (DATA – 255)dB

For DATA = FF_H, ATTEN = –0dB
For DATA = FE_H, ATTEN = –0.5dB
For DATA = 01_H, ATTEN = –127.5dB
For DATA = 00_H, ATTEN = infinity = Mute

LDL Left Channel Attenuation Data Load Control. This bit is used to simultaneously set attenuation levels of both the Left and Right channels.

When LDL = 1, the Left channel output level is set by the data in AL[7:0]. The Right channel output level is set by the data in AL[7:0], or the most recently programmed data in bits AR[7:0] of register MODE1.

When LDL = 0, the Left channel output data remains at its previously programmed level.

REGISTER 1 (A1 = 0, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to set the attenuation data for the Right output channel.

When ATC = 1 (Bit B2 of Register MODE3 = 1), the Left channel attenuation data AL[7:0] of register MODE0 is used for both the Left and Right channel attenuators.

When ATC = 0, (Bit B2 of Register MODE3 = 0), Left channel attenuation data is taken from AL[7:0] of register MODE0, and Right channel attenuation data is taken from AR[7:0] of register MODE1.

AR[7:0] Right Channel Attenuator Data, where AR7 is the MSB and AR0 is the LSB. Attenuation Level is given by:

ATTEN = 0.5 • (DATA – 255) dB

For DATA = FF_H, ATTEN = –0dB
For DATA = FE_H, ATTEN = –0.5dB
For DATA = 01_H, ATTEN = –127.5dB
For DATA = 00_H, ATTEN = infinity = Mute

LDR Right Channel Attenuation Data Load Control. This bit is used to simultaneously set attenuation levels of both the Left and Right channels.

When LDR = 1, the Right channel output level is set by the data in AR[7:0], or by the data in bits AL[7:0] of register MODE0. The Left channel output level is set to the most recently programmed data in bits AL[7:0] of register MODE0.

When LDR = 0, the Right channel output data remains at its previously programmed level.

REGISTER 2 (A1 = 1, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	CB1	CB0	SCA	FSS	IW1	IWO	OPE	DEM	MUTE

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and input audio data bit and format.

MUT (B0)	
MUT = L	Soft Mute OFF
MUT = H	Soft Mute ON

TABLE X. Soft Mute Control.

DEM (B1)	
DEM = L	De-Emphasis OFF
DEM = H	De-Emphasis ON

TABLE XI. De-Emphasis Control.

OPE (B2)	
OPE = L	Normal Operation
OPE = H	DAC Operation OFF

TABLE XII. DAC Operation Control.

When OPE (B2) is HIGH, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

IW0(B3), IW1 (B4) and I^2S (B0) of Register 3

Resisters IW0, IW1, and I^2S determine the input data word and input data format as shown in Table XIII.

IW1	IW0	I^2S	AUDIO INTERFACE
L	L	L	16-Bit Standard (Right-Justified)
L	H	L	20-Bit Standard (Right-Justified)
H	L	L	24-Bit Standard (Right-Justified)
H	H	L	24-Bit Left-Justified (MSB First)
L	L	H	16-Bit I^2S
L	H	H	24-Bit I^2S
H	L	H	Reserved
H	H	H	Reserved

TABLE XIII. Data Format Control.

Sampling Rate Range is selected by the FSS (B5) register.

FSS (B5)	SAMPLING RATE RANGE
FSS = L	Sampling Rate, f_S ≤52kHz
FSS = H	Sampling Rate, f_S >52kHz

TABLE XIV. Sampling Rate Range Select.

HDCD gain scaling can be implemented internally with digital gain scaling (for normal CD and HDCD without peak extend), or externally with analog gain scaling (for HDCD with and without peak extend).

Digital gain scaling is implemented by 6dB attenuation for normal CD and HDCD without peak extend, and also operated as 0dB attenuation for HDCD with peak extend. Detection for normal CD, HDCD without peak extend, and HDCD with peak extend is done automatically.

SCA (B6)	GAIN SCALING
SCA = L	Digital Gain Scaling
SCA = H	Analog Gain Scaling

TABLE XV. Gain Scaling Select.

These bits define the location of the bit in which the PCM1732 looks for HDCD hidden code, which is inserted into the Least Significant Bit (LSB) of the audio data.

In the case of HDCD encoded data, the HDCD hidden code is located in the Least Significant Bit (LSB) of 16-bit audio data. It is not necessary to change the location of this hidden code as default.

In the case of 20-bit or 24-bit data word with HDCD encoded input signal, this HDCD hidden code bit location must be changed to LSB of the 20- or 24-bit word to detect HDCD encoded signal. The word length is selected by the CB0 and CB1 bits.

CB1 (B8)	CB0 (B7)	HDCD HIDDEN CODE BIT LOCATION
L	L	16th Data (default for CD)
L	H	20th Data
H	L	Reserved
H	H	24th Data

TABLE XVI. Word Length Selection for Hidden Code Bit.

REGISTER 3 (A1 = 1, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	IZD	SF1	SF0	CKO	REV	res	ATC	LRP	I^2S

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency, infinite zero detection, output phase, CLKO output, and slow roll-off.

Bit 8 is used to control the Infinite Zero Detection (IZD) function.

When IZD is LOW, the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is HIGH, the zero detect feature is enabled. If the input data is continuously zero for 65,536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1732 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

IZD (B8)	ZERO MUTE
IZD = L	Zero Detect Mute OFF
IZD = H	Zero Detect Mute ON

TABLE XVII. Zero Mute Control.

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency for de-emphasis.

SF1	SF0	DE-EMPHASIS SAMPLING RATE
L	L	Reserved
L	H	48kHz
H	L	44.1kHz
H	H	32kHz

TABLE XVIII. De-Emphasis Sampling Rate Selection.

CKO (B5) is output frequency control at CLKO pin, can be selected as buffer (1/1) or half rate of input frequency (1/2).

CKO (B5)	CLOCK OUTPUT RATE
CKO = L	Buffer Out of XTI Clock
CKO = H	Half (1/2) Frequency Out of XTI Clock

TABLE XIX. Clock Output Rate Selection.

REV (B4) is output analog signal phase control.

REV (B4)	DAC OUTPUT PHASE
REV = L	Normal Output
REV = H	Inverted Output

TABLE XX. Output Phase Inversion Control.

ATC (B2) is used as an attenuation control. When bit 3 is set HIGH, the attenuation data on Register 0 is used for both channels, and the data in Register 1 is ignored. When bit 3 is LOW, each channel has separate attenuation data.

ATC (B2)	ATTENUATION CONTROL
ATC = L	Individual Channel ATT Control
ATC = H	Common ATT Control

TABLE XXI. Attenuation Control Bit.

Bit 0 (I^2S)is used to control the input data format. A LOW on bit 0 sets the format to MSB-first, right-justified standard format) and a HIGH sets the format to I^2S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (left/right clock). When bit 1 is LOW, left channel data is assumed when LRCIN is in a HIGH phase, and right channel data is assumed when LRCIN is in a LOW phase. When bit 1 is HIGH, the polarity assumption is reversed. LRP applies only to standard and left-justified data formats.

LRP (B1)	LRCIN POLARITY	
LRP = L	L R	H/Lch
LRP = H	L R	L/Lch

TABLE XXII. LRCIN Polarity.

THEORY OF OPERATION

The delta-sigma DAC portion of the PCM1732 is based on an 8-level amplitude quantizer and a 4th-order noise shaper, which converts the oversampled input data to an 8-level delta-sigma format.

This newly developed "enhanced multi-level delta-sigma" architecture achieves high-grade audio dynamic performance and sound quality.

A block diagram of the 8-level delta-sigma modulator is shown in Figure 10. This 8-level delta-sigma modulator has several advantages over the typical one-bit (2 level) delta-sigma modulator. These advantages include improved quantization noise performance, low out-of-band noise, low idle channel tones, and improved jitter performance.

The theoretical quantization noise performance of an 8-level delta-sigma modulator is shown in Figure 11 and a simulated clock jitter sensitivity plot is shown in Figure 12.

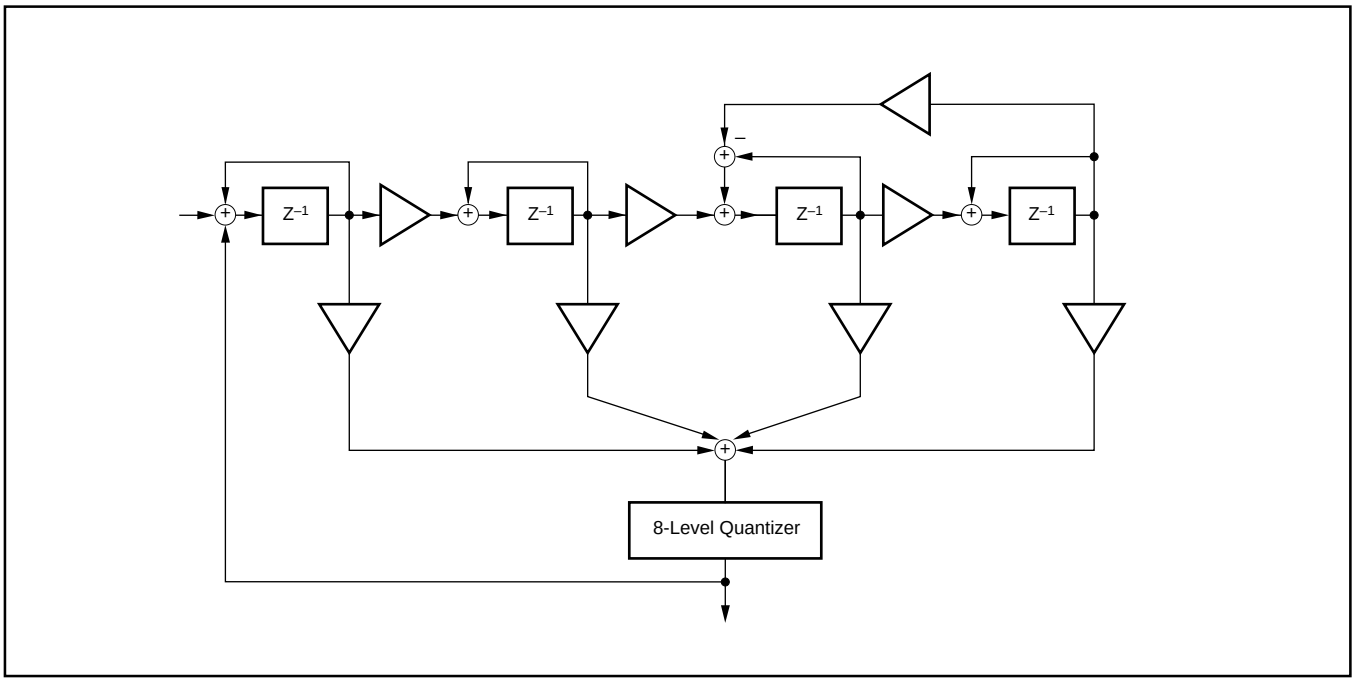


FIGURE 10. 8-Level Delta-Sigma Modulator.

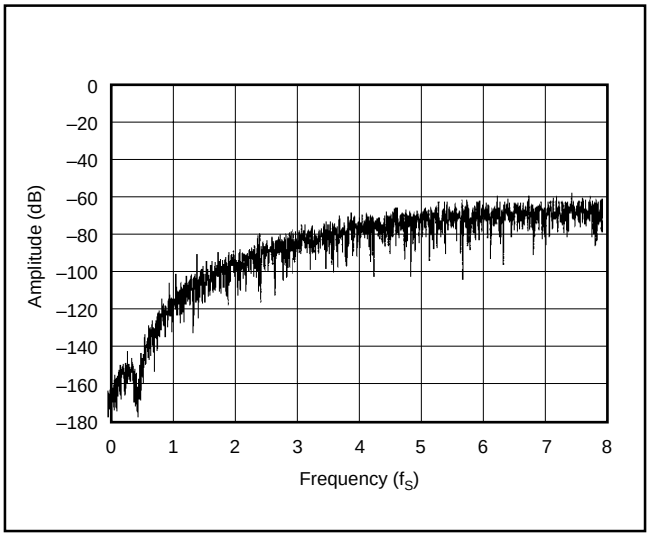


FIGURE 11. Quantization Noise Spectrum.

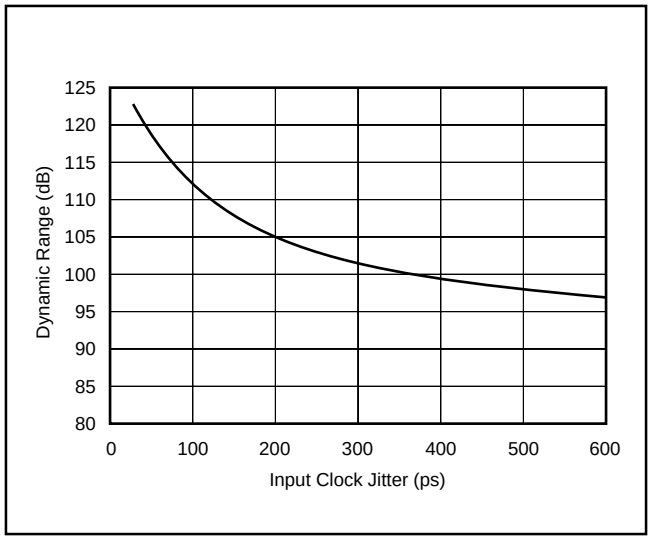


FIGURE 12. Jitter Sensitivity.

APPLICATION CONSIDERATIONS

TYPES OF CD SOURCE MATERIAL

There are two types of HDCD recordings: HDCD encoded data “with peak extend” and “without peak extend.” Most HDCD recordings are encoded using peak extension which gives them more “headroom” than standard CD and HDCD disks without peak extend.

PCM1732 automatically detects these various types of source materials, indicates HDCD encoded source material by the HDCD encoded data detect (pin 9), and indicates a peak extended source by the GAIN (pin 20). Table XXII shows the relationship between various types of CD source material and their corresponding reference levels.

CD SOURCE MATERIAL	HDCD PIN	GAIN PIN	REFERENCE LEVEL
Standard CD	L	L	0dB
HDCD Without Peak Extend	H	L	0dB
HDCD With Peak Extend	H	H	–6dB

TABLE XXIII. CD Source Material and Reference Levels.

In order to ensure that the average system output level of HDCD recordings (with peak extend) match that of standard CD and HDCD (without peak extend), analog or digital gain scaling is implemented.

DIGITAL GAIN SCALING

Digital gain scaling is automatically performed in the digital attenuation section by detecting HDCD material encoded with peak extend and reducing the gain of standard CD and HDCD encoded without peak extend by 6dB.

Digital gain scaling produces a 6dB reduciton in dynamic range, but does not require additional analog gain scaling circutry.

Gain scaling is controlled by the SCA bit in Register 2. Setting SCA = 0 enables digital gain scaling. Setting SCA = 1 enables analog gain scaling. The reset default is SCA = 0, digital gain scaling.

ANALOG GAIN SCALING

Analog gain scaling (SCA = 1) is implemented by an external switched analog gain circuit which is controlled by the GAIN pin (pin 20). This switched analog gain circuit provides +6dB of gain for HDCD disks with peak extend 0dB of gain for standard CD and HDCD disks without peak extend. Since HDCD recording with peak extend may have peaks similiar to standard CD recordings, the analog gain circuits must provide enough headroom for these higher signal levels when operating with +6dB of gain.

OUTPUT FILTERING

For testing purposes, all dynamic tests are performed on the PCM1732 using a 20kHz low-pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and dynamic range readings than listed in the Specifications Table. The low-pass filter removes out-of-band noise. Although it is not audible, it may affect dynamic performance specifications.

The performance of the internal low pass filter from DC to 40kHz is shown in Figure 13. The higher frequency roll-off of the filter is shown in Figure 14. If the user’s application has the PCM1732 driving a wideband amplifier, it is recommended to use an external low-pass filter.

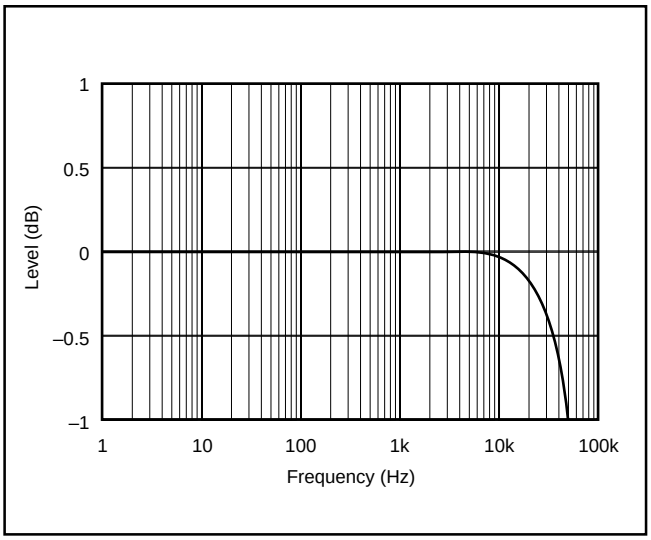


FIGURE 13. Low-Pass Filter Response.

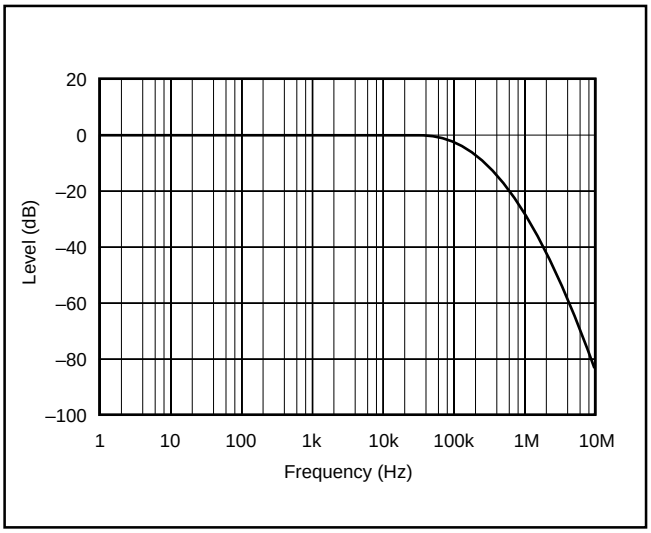


FIGURE 14. Low-Pass Filter Response.

POWER SUPPLY BYPASSING

The power supplies should be bypassed as close as possible to the device. Refer to Figure 15 for optimal values of bypass capacitors.

POWER SUPPLY CONNECTIONS

PCM1732 has four power supply pins for digital (V_{DD}), and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.1V.

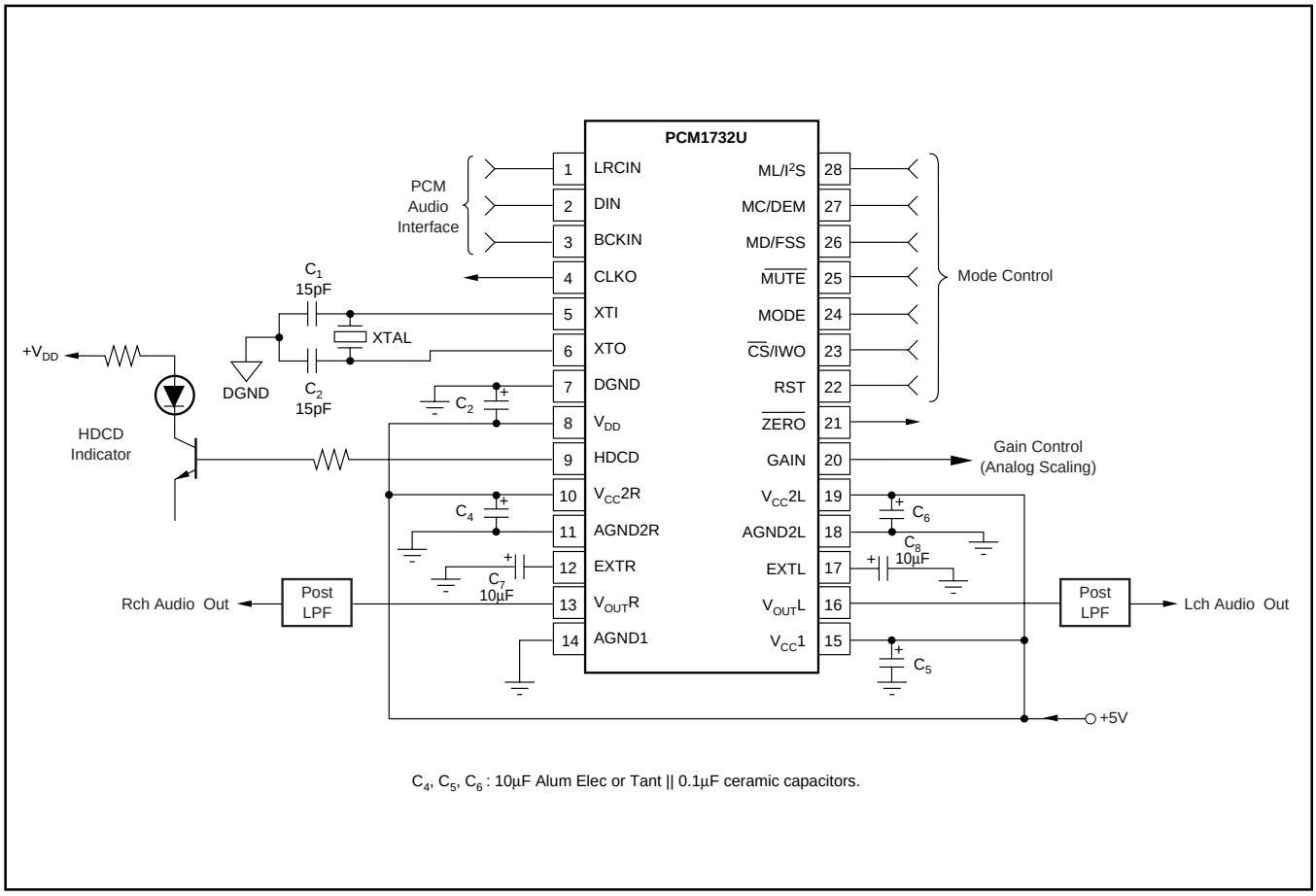


FIGURE 15. Typical Circuit Connection Diagram.

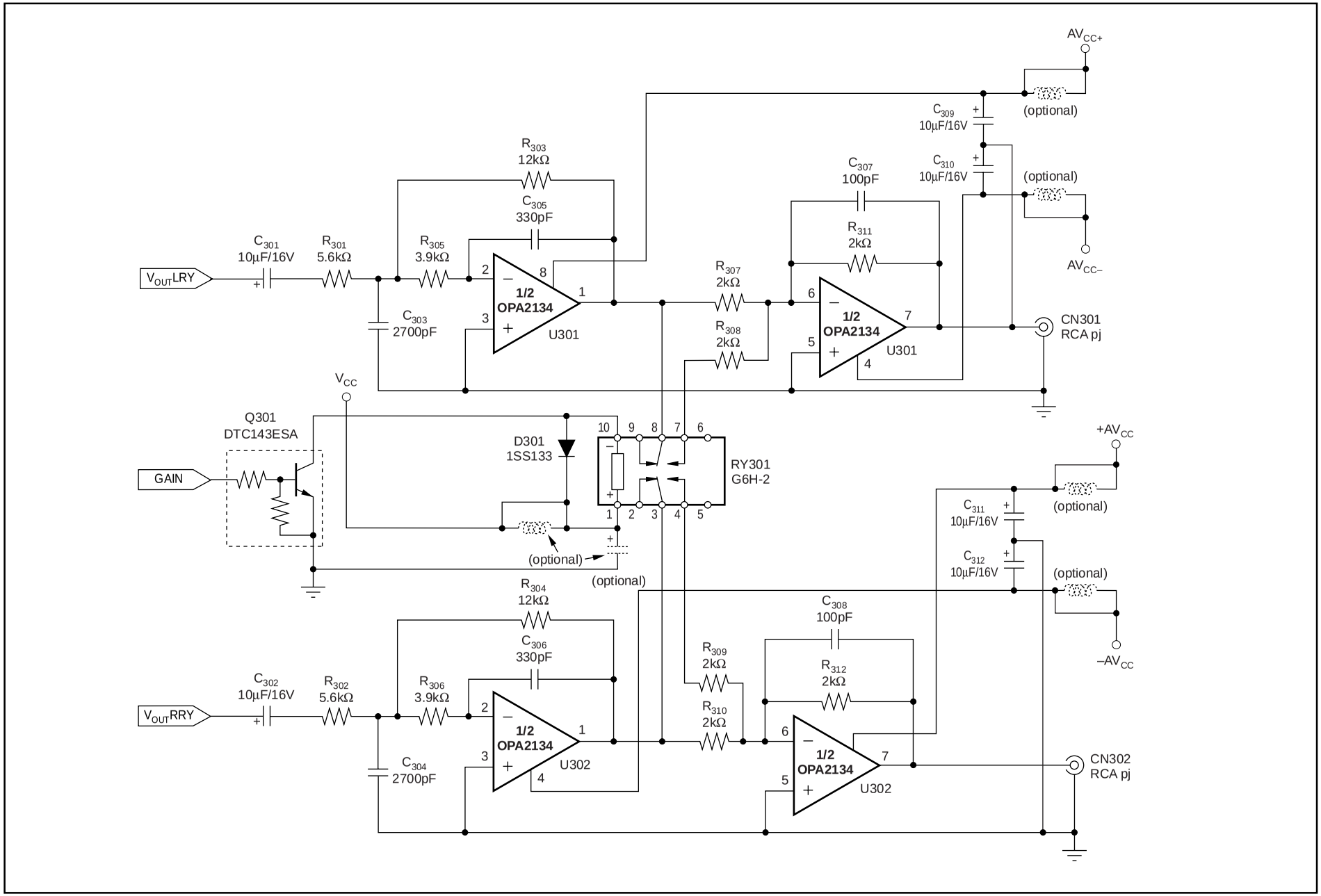


FIGURE 16. Low-Pass Filter and Amplifier (relay switched).

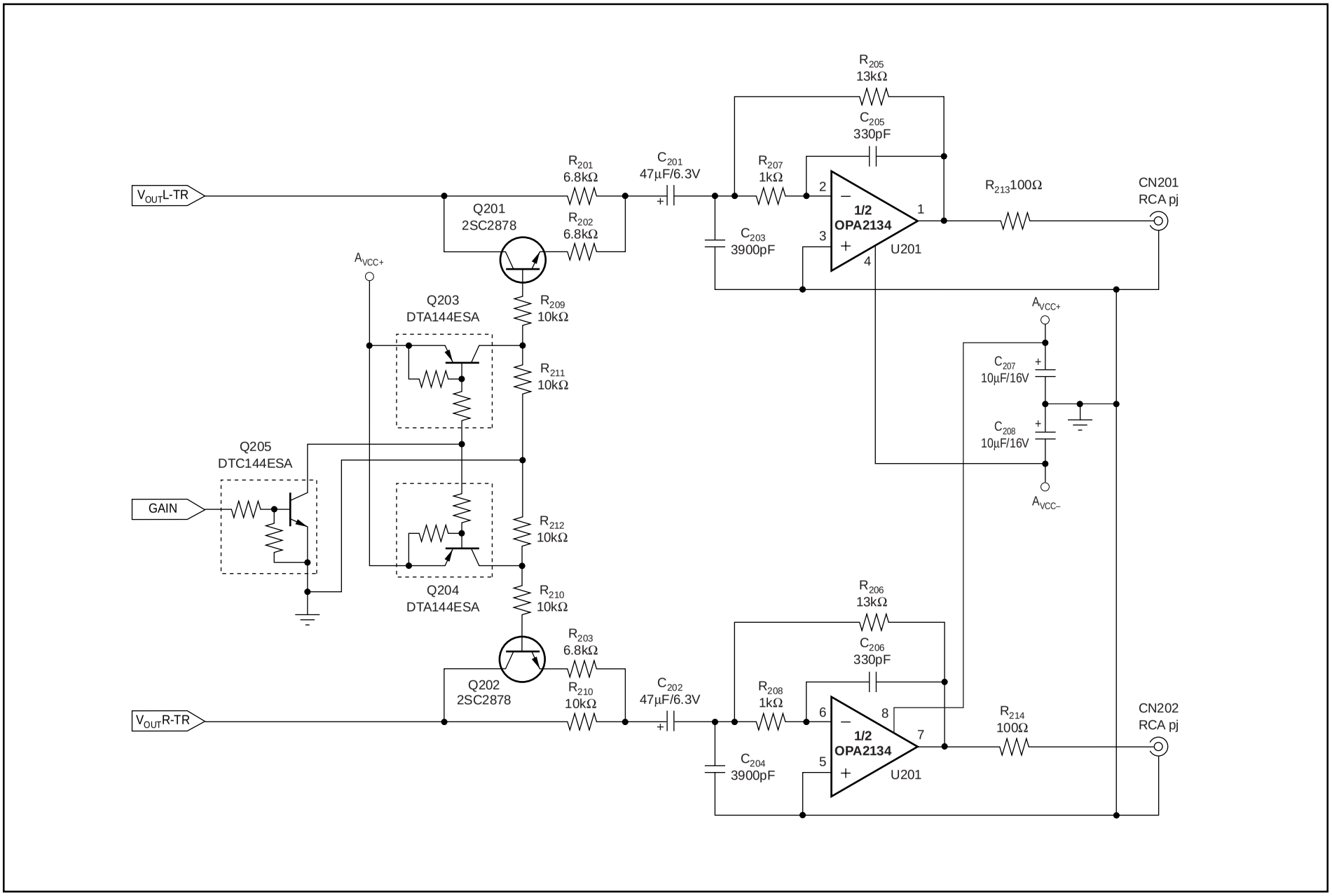


FIGURE 17. Low-Pass Filter and Amplifier (transistor swtiched).