M41T50

Serial Access Digital Input Real-Time Clock with Alarms

PRELIMINARY DATA

FEATURES SUMMARY

- TIMEKEEPING DOWN TO 1.3V
- 1.7V TO 3.6V I^2C BUS OPERATING VOLTAGE
- OPERATES FROM 50Hz OR 60Hz DIGITAL CLOCK SIGNAL
- COUNTERS FOR SECONDS, MINUTES, HOURS, DAY, DATE, MONTH, YEAR, AND CENTURY
- SERIAL INTERFACE SUPPORTS I^2C BUS (400kHz)
- PROGRAMMABLE ALARM AND INTERRUPT FUNCTION
- 1Hz SQUARE WAVE OUTPUT
- LOW OPERATING CURRENT OF 350µA
- AUTOMATIC LEAP YEAR COMPENSATION
- SOFTWARE PROGRAMMABLE OUTPUT (OUT)
- OPERATING TEMPERATURE OF –40 TO 85°C
- LEAD-FREE 16-PIN QFN PACKAGE

Figure 1. Package

QFN16 (Q)

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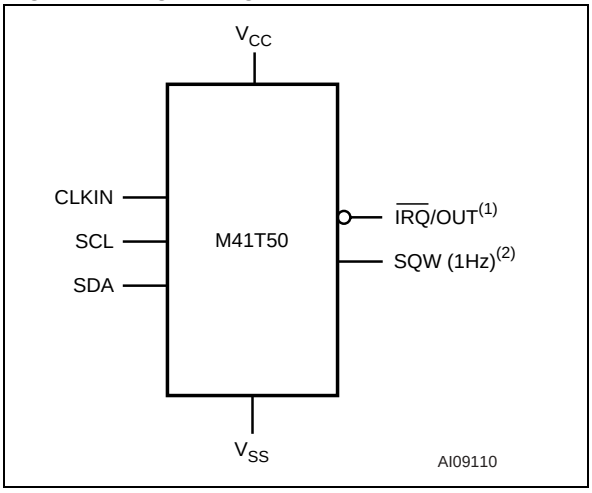
SUMMARY DESCRIPTION

The M41T50 Serial Access TIMEKEEPER® is a low power Serial RTC that does not require a crystal. The clock operates from a digital clock input pin at 50Hz or 60Hz. Eight registers (see Table 2., page 12) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 8 registers provide status/control of Alarm, Square Wave (1Hz), and 50Hz or 60Hz digital clock frequency selection functions. Addresses and data are transferred serially via a two line, bi-directional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

Functions available to the user include a time-of-day clock/calendar, Alarm interrupts, and Square Wave output. The eight clock address locations contain the century, year, month, date, day, hour, minute, and seconds in 24-hour BCD format. Corrections for 28-, 29- (leap year), 30- and 31-day months are made automatically.

The M41T50 is supplied in a 16-pin QFN.

Figure 2. Logic Diagram

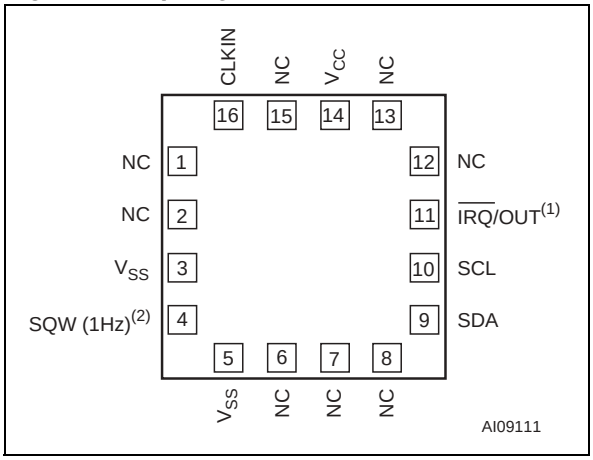


Note: 1. Open Drain only.
2. Defaults to push-pull (SQW disabled) on power-up. May also be programmed to be Open Drain.

Table 1. Signal Names

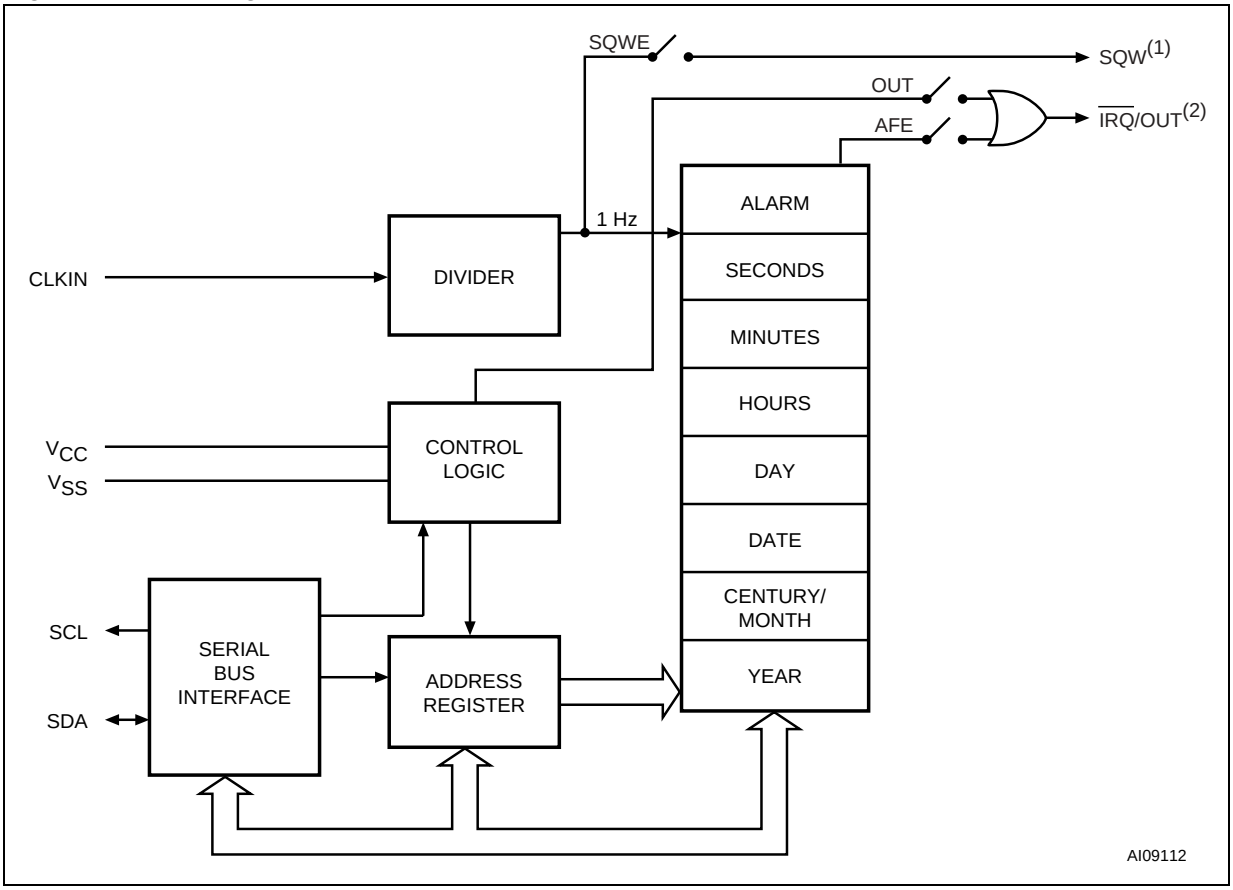
CLKIN	Digital Clock Input (50Hz or 60Hz)
SDA	Serial Data Input/Output
SCL	Serial Clock Input
$\overline{IRQ}$/OUT	Interrupt or OUT Output (Open Drain)
SQW (1Hz)	Square Wave Output (Open Drain or Push-pull)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 3. 16-pin QFN Connections



Note: 1. Open Drain only.
2. Defaults to push-pull (SQW disabled) on power-up. May also be programmed to be Open Drain.

Figure 4. Block Diagram



Note: 1. May be configured as either push-pull or open drain.
2. Open drain only.

OPERATION

The M41T50 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 16 bytes contained in the device can then be accessed sequentially in the following order:

1. Reserved0 Register
2. Seconds Register
3. Minutes Register
4. Hours Register
5. Day Register
6. Date Register
7. Century/Month Register
8. Year Register
9. Out Register
10. Reserved1 Register

11 - 15. Alarm Registers

16. Flags Register

2-Wire Bus Characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

– Data transfer may be initiated only when the bus is not busy.
– During data transfer, the data line must remain stable whenever the clock line is High.
– Changes in the data line, while the clock line is High, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy. Both data and clock lines remain High.

Start data transfer. A change in the state of the data line, from high to Low, while the clock is High, defines the START condition.

Stop data transfer. A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data Valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

Acknowledge. Each byte of eight bits is followed by one Acknowledge Bit. This Acknowledge Bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 5. Serial Bus Data Transfer Sequence

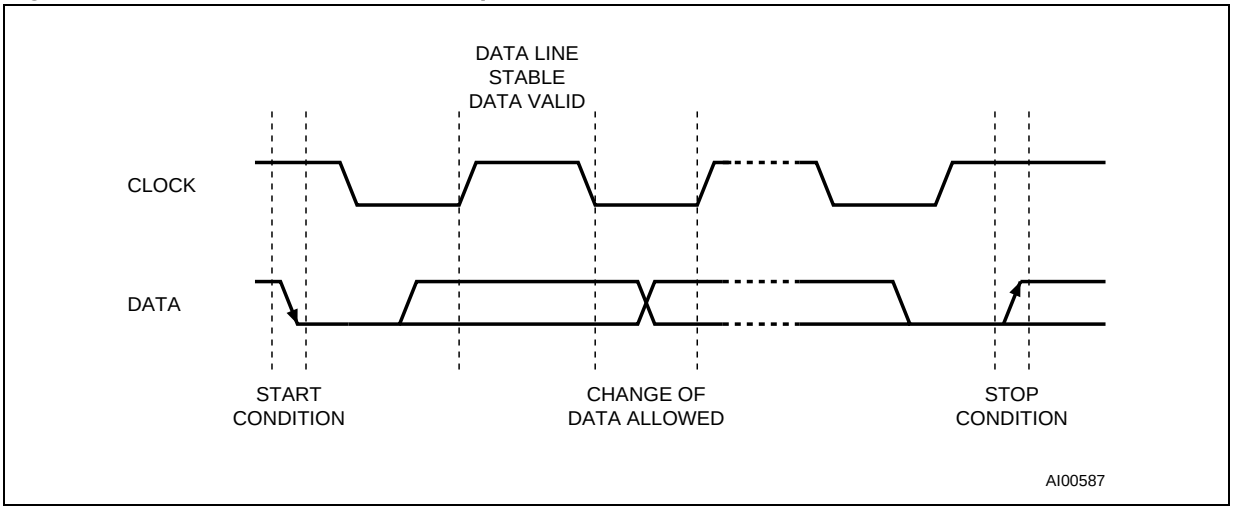
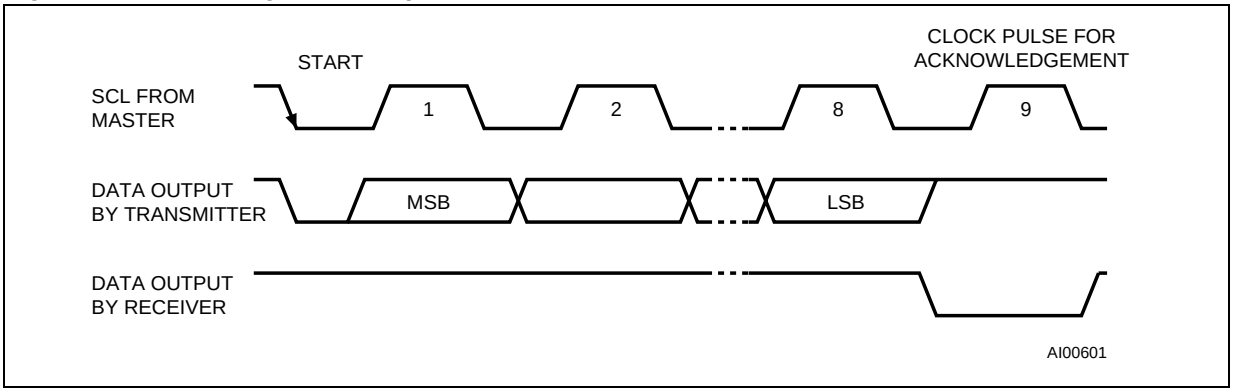


Figure 6. Acknowledgement Sequence



READ Mode

In this mode the master reads the M41T50 slave after setting the slave address (see Figure 8., page 9). Following the WRITE Mode Control Bit (R/$\overline{W}$=0) and the Acknowledge Bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ Mode Control Bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an Acknowledge Bit to the slave transmitter. The address pointer is only incremented on reception of an Acknowledge Clock. The M41T50 slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to “An+2.”

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume due to a Stop Condition or when the pointer increments to any non-clock address (08h-0Fh).

Note: This is true both in READ Mode and WRITE Mode.

An alternate READ Mode may also be implemented whereby the master reads the M41T50 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see Figure 9., page 9).

Figure 7. Slave Address Location

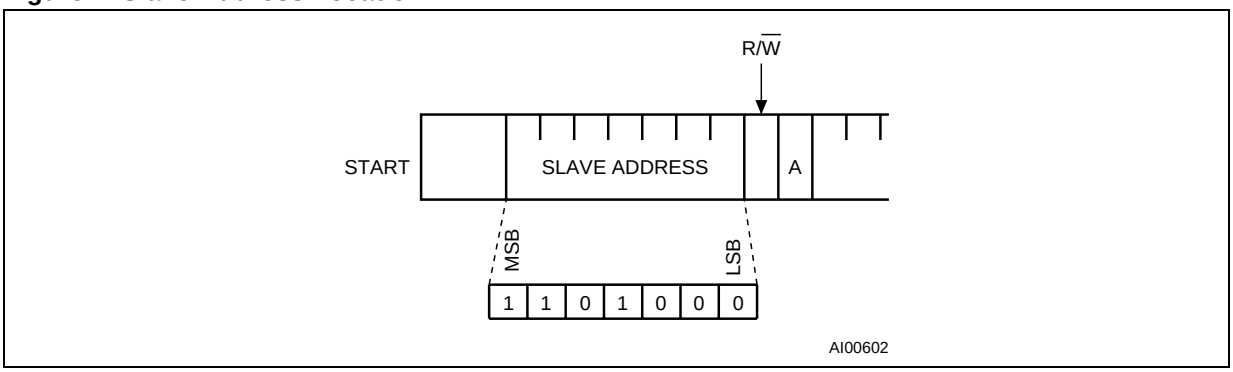


Figure 8. READ Mode Sequence

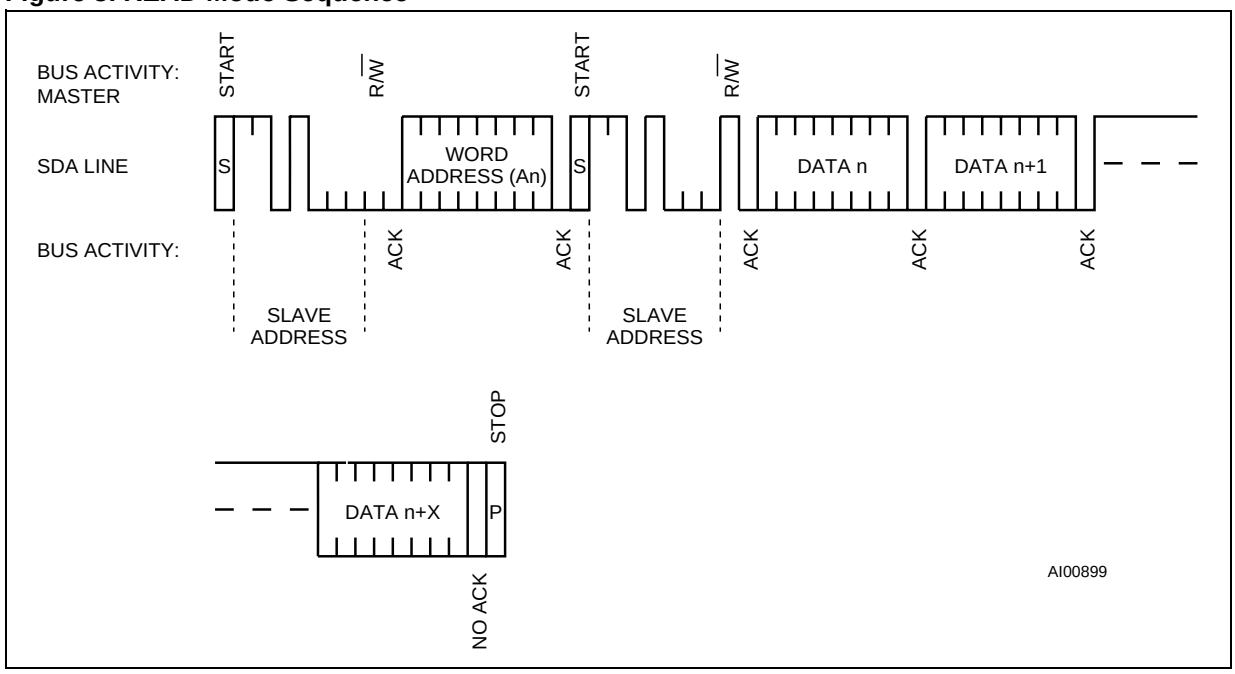
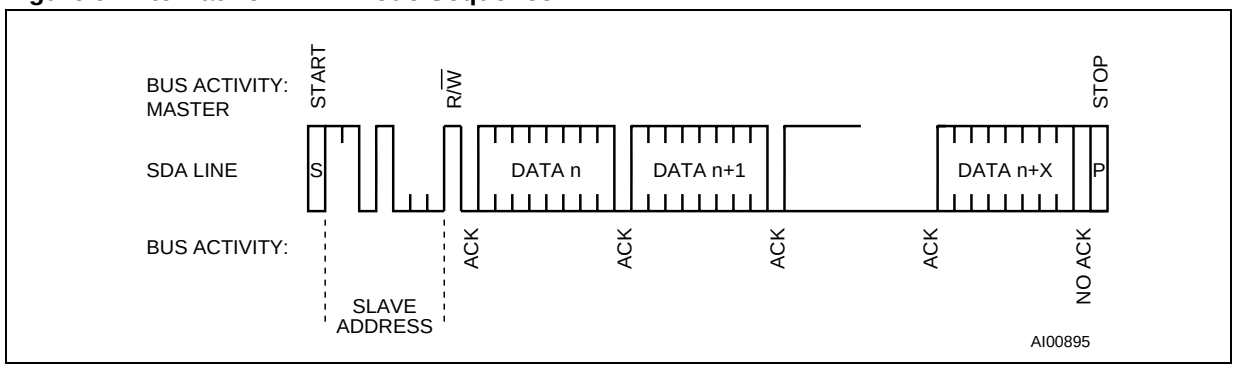


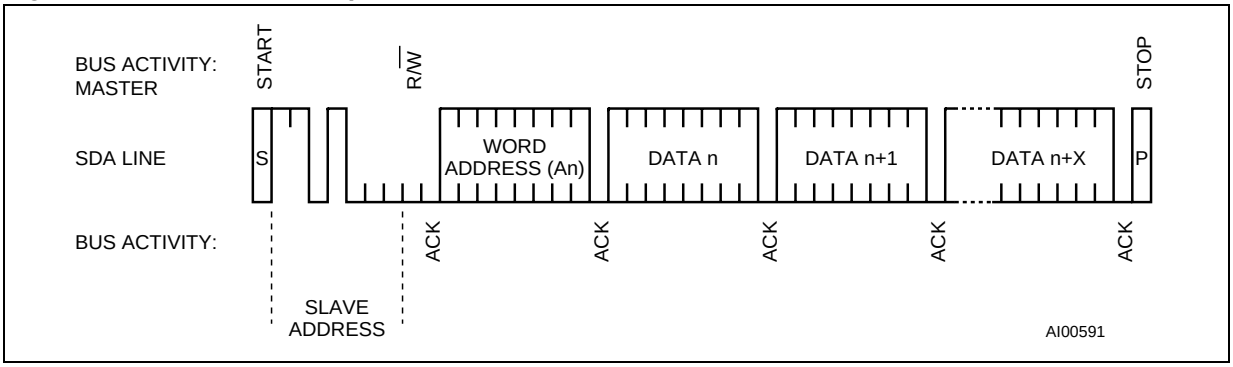
Figure 9. Alternative READ Mode Sequence



WRITE Mode

In this mode the master transmitter transmits to the M41T50 slave receiver. Bus protocol is shown in Figure 10., page 10. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T50 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address see Figure 7., page 8 and again after it has received the word address and each data byte.

Figure 10. WRITE Mode Sequence



CLOCK OPERATION

The eight byte clock register (see Table 2., page 12) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Reserved0, Seconds, Minutes, and Hours are contained within the first four registers.

Bits D0 through D2 of Register 04h contain the Day (day of week). Registers 05h, 06h, and 07h contain the Date (day of month), Month, and Years. Bit D7 of Register 01h contains the STOP Bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a '0' the oscillator restarts within one second (typical).

Bits D6 and D7 of Clock Register 06h (Century/ Month Register) contain the CENTURY Bit 0 (CB0) and CENTURY Bit 1 (CB1).

Bit D6 of Register 0Ch (Alarm Hour Register) contains the SQW Open Drain Bit (SQWOD). When this bit is set to '1,' the Square Wave output will become an open drain output and require a pull-up resistor.

Note: A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the 60Hz Bit and CB0-CB1 Bits will result in an update of the system clock and a reset of the divider chain. This could result in an inadvertent change of the current time. These non-clock related bits should be written prior to setting the clock, and remain unchanged until such time as a new clock time is also written.

The eight Clock Registers may be read one byte at a time, or in a sequential block. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

Digital Clock Input

The M41T50 requires an external square wave clock source of 50Hz or 60Hz (45% to 55% duty cycle) for the clock function. Bit D7 (60Hz bit) of Register 05h (Date Register) is used to select between a 50Hz (60Hz Bit = '0') or a 60Hz (60Hz Bit = '1') clock input frequency signal. The 60Hz Bit defaults to '1' on power-up.

TIMEKEEPER® Registers

The M41T50 offers 16 internal registers which contain Clock, Alarm, and Flag Registers. The Clock registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address (00h to 07h).

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a Stop Condition or when the pointer increments to a non-clock address.

TIMEKEEPER and Alarm Registers store data in BCD format.

Table 2. TIMEKEEPER® Register Map

Addr									Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0	0	0	0	0	0	0	0	Reserved0	
01h	ST	10 Seconds			Seconds				Seconds	00-59
02h	0	10 Minutes			Minutes				Minutes	00-59
03h	0	0	10 Hours		Hours (24 Hour Format)				Hours	00-23
04h	0	0	0	0	0	Day of Week			Day	01-7
05h	60Hz	0	10 Date		Date: Day of Month				Date	01-31
06h	CB1	CB0	0	10M	Month				Century/ Month	0-3/01-12
07h	10 Years				Year				Year	00-99
08h	OUT	0	0	0	0	0	0	0	Out	
09h	0	0	0	0	0	0	0	0	Reserved1	
0Ah	AFE	SQWE	0	Al 10M	Alarm Month				Al Month	01-12
0Bh	RPT4	RPT5	Al 10 Date		Alarm Date				Al Date	01-31
0Ch	RPT3	SQWOD	Al 10 Hour		Alarm Hour				Al Hour	00-23
0Dh	RPT2	Alarm 10 Minutes			Alarm Minutes				Al Min	00-59
0Eh	RPT1	Alarm 10 Seconds			Alarm Seconds				Al Sec	00-59
0Fh	0	AF	0	0	0	0	0	0	Flags	

Keys: 0 = Must be set to '0'
AF = Alarm Flag (Read only)
AFE = Alarm Flag Enable Flag
CB0-CB1 = Century Bits
OUT = Output level
SQWOD = Square Wave output Open Drain Bit
RPT1-RPT5 = Alarm Repeat Mode Bits
SQWE = Square Wave Enable Bit
ST = Stop Bit
60Hz = 50Hz or 60Hz Select Bit

Setting Alarm Clock Registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. Bits RPT5–RPT1 put the alarm in the repeat mode of operation. Table 3., page 13 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5–RPT1, the AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$/OUT pin. To disable the alarm, write '0' to the Alarm Date Register and to RPT5–RPT1.

Note: If the address pointer is allowed to increment to the Flag Register address, an alarm condition will not cause the Interrupt/Flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the “Alarm Seconds,” the address pointer will increment to the Flag address, causing this situation to occur.

The $\overline{IRQ}$ output is cleared by a READ to the Flags Register as shown in Figure 11., page 13. A subsequent READ of the Flags Register is necessary to see that the value of the Alarm Flag has been reset to '0.'

Figure 11. Alarm Interrupt Reset Waveform

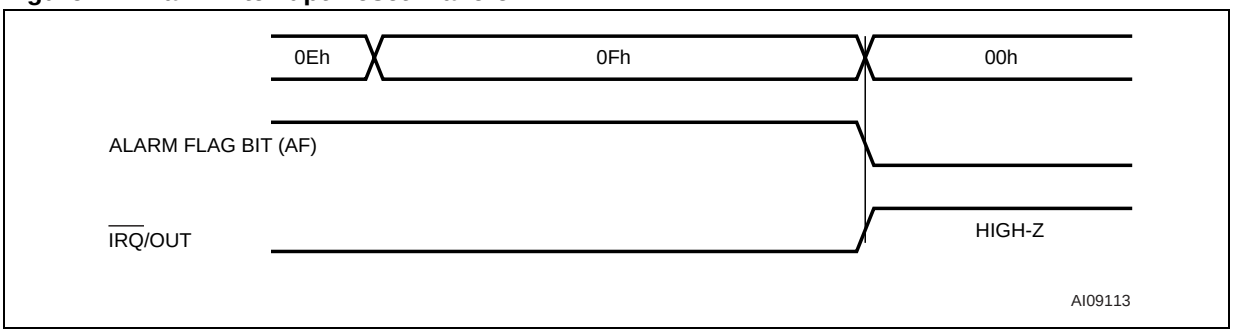


Table 3. Alarm Repeat Modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm Setting
1	1	1	1	1	Once per Second
1	1	1	1	0	Once per Minute
1	1	1	0	0	Once per Hour
1	1	0	0	0	Once per Day
1	0	0	0	0	Once per Month
0	0	0	0	0	Once per Year

Square Wave Output

The M41T50 offers the user a 1Hz square wave function which is output on the SQW pin. The SQW pin can be turned on and off under software control with the Square Wave Enable Bit (SQWE) located in Register 0Ah.

The SQW output is programmable as an N-channel, open drain output driver, or a full CMOS output driver. The initial power-up default for the SQW output is disabled, in the full-CMOS (or Push-pull mode). By setting the Square Wave Open Drain Bit (SQWOD in address 0Ch) to a '1,' the output will be configured as an open drain (with I_{OL} as specified in Table 9., page 17). When SQWOD is set to '0,' the output will be configured as full-CMOS (sink and source current as specified in Table 9., page 17).

Note: When configured as Open Drain (SQWOD = '1'), the SQW pin requires an external pull-up resistor.

Century Bits

These two bits will increment in a binary fashion at the turn of the century, and handle all leap years correctly. See Table 5., page 14 for additional explanation.

Output Driver Pin

When the AFE Bit is not set to generate an interrupt, the $\overline{IRQ}$/OUT pin becomes an output driver that reflects the contents of D7 of the Out Register. In other words, when D7 (OUT Bit) is a '0,' then the $\overline{IRQ}$/OUT pin will be driven low.

Note: The $\overline{IRQ}$/OUT pin is an open drain which requires an external pull-up resistor.

Initial Power-on Defaults

Upon application of power to the device, the register bits will initially power-on in the state indicated in Table 4.

Table 4. Initial Power-on Default Values

Condition	ST	SQWOD	OUT	AFE	SQWE	60Hz
Initial Power-up(1)	0	0	1	0	0	1

Note: 1. All other control bits power-up in an undetermined state.

Table 5. Century Bits Examples

CB0	CB1	Leap Year?	Example(1)
0	0	Yes	2000
0	1	No	2100
1	0	No	2200
1	1	No	2300

Note: 1. Leap year occurs every four years (for years evenly divisible by four), except for years evenly divisible by 100. The only exceptions are those years evenly divisible by 400 (the year 2000 was a leap year, year 2100 is not).

MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Sym	Parameter	Value	Unit
T_{STG}	Storage Temperature (V_{CC} Off)	–55 to 125	°C
V_{CC}	Supply Voltage	–0.3 to 4.6	V
T_{SLD}(1)	Lead Solder Temperature for 10 Seconds	260	°C
V_{IO}	Input or Output Voltages	–0.2 to Vcc+0.2	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: 1. Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. Operating and AC Measurement Conditions

Parameter	M41T50
Supply Voltage (V_{CC})	1.7V to 3.6V
Ambient Operating Temperature (T_A)	–40 to 85°C
Load Capacitance (C_L)	50pF
Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8\ V_{CC}$(1)
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7\ V_{CC}$

Note: 1. $0.2V_{CC}$ to $0.9V_{CC}$ for CLKIN input (pin 16)

Figure 12. AC Measurement I/O Waveform

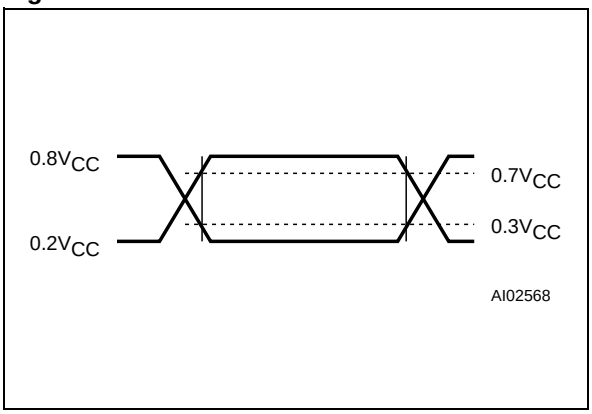


Table 8. Capacitance

Symbol	Parameter(1,2)	Min	Max	Unit
C_{IN}	Input Capacitance		7	pF
C_{OUT}(3)	Output Capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

Note: 1. Effective capacitance measured with power supply at 3.6V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 9. DC Characteristics

Symbol	Parameter	Test Condition(1)			Min	Typ	Max	Unit
V_{CC}	Operating Voltage	Clock			1.3		3.6	V
		I^2C bus (400kHz)			1.7		3.6	V
I_{CC1}	Supply Current	SCL = 400kHz (No load)		V_{CC} = 3.6V			400	µA
				V_{CC} = 3.0V		350		µA
				V_{CC} = 2.5V		300		µA
				V_{CC} = 2.0V		250		µA
I_{CC2}	Supply Current (standby)	SCL = 0Hz All inputs(2) ≥ V_{CC} – 0.2V ≤ V_{SS} + 0.2V	SQW On (Open Drain)	3.6V			1.3	µA
				3.0V		1.2		µA
				2.0V		0.9		µA
			SQW Off	3.6V			0.7	µA
				3.0V		0.65		µA
				2.0V		0.6		µA
V_{IL}	Input Low Voltage				–0.2		$0.3V_{CC}$	V
V_{IH}	Input High Voltage				$0.9V_{CC}$		V_{CC}+0.2	V
V_{OL}	Output Low Voltage	V_{CC} = 3.6V, I_{OL} = 3.0mA (SDA)					0.4	V
		V_{CC} = 3.6V, I_{OL} = 1.0mA ($\overline{IRQ}$/OUT, SQW)					0.4	V
V_{OH}	Output High Voltage	V_{CC} = 3.6V, I_{OH} = –1.0mA (Push-Pull only)			2.4			V
	Pull-up Supply Voltage (Open Drain)	$\overline{IRQ}$/OUT, SQW (1Hz)					3.6	V
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}(2)					±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}					±1	µA

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 1.7V to 3.6V (except where noted).
2. CLKIN pin = V_{SS} or V_{CC}.

Figure 13. Bus Timing Requirements Sequence

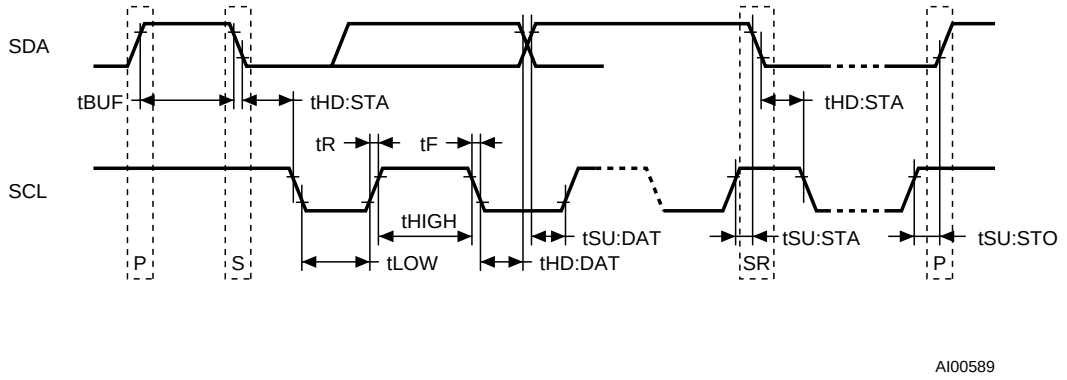


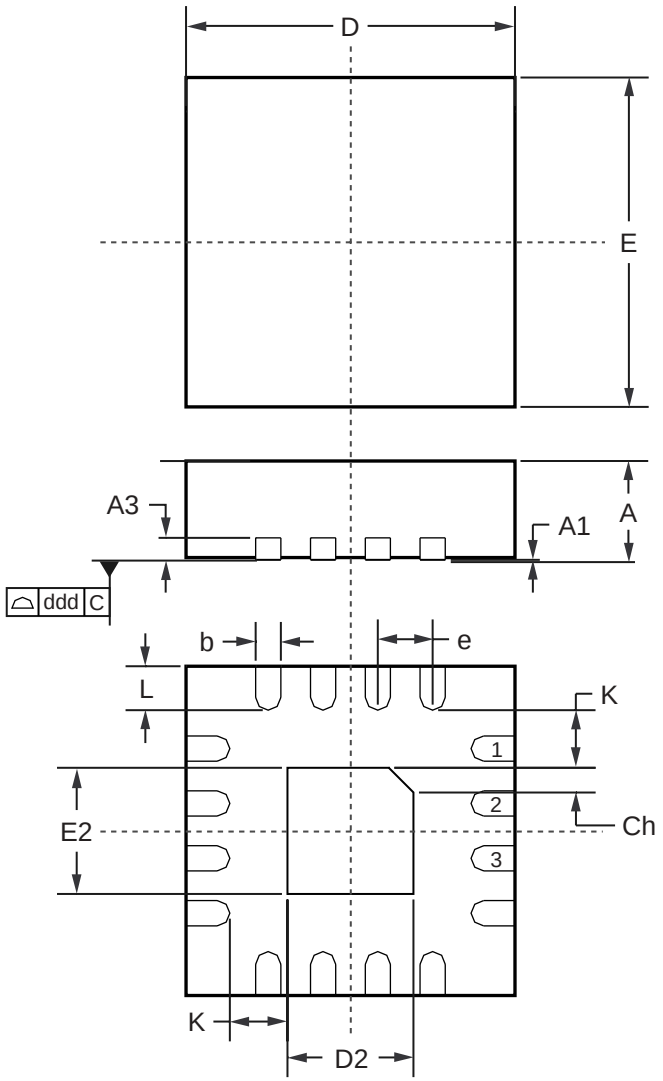
Table 10. AC Characteristics

Sym	Parameter[1]	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	0		400	kHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_R	SDA and SCL Rise Time			300	ns
t_F	SDA and SCL Fall Time			300	ns
$t_{HD:STA}$	START Condition Hold Time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START Condition Setup Time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$[2]	Data Setup Time	100			ns
$t_{HD:DAT}$	Data Hold Time	0			µs
$t_{SU:STO}$	STOP Condition Setup Time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = 1.7V to 3.6V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of SCL.

PACKAGE MECHANICAL INFORMATION

Figure 14. QFN16 – 16-lead, Quad, Flat Package, No Lead, 3x3mm body size, Outline

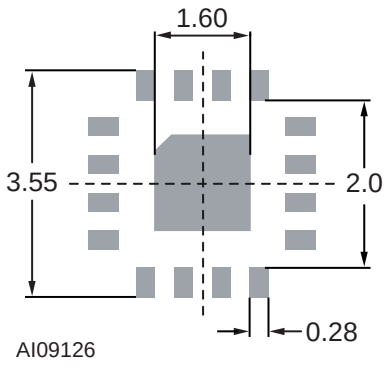


Note: Drawing is not to scale.

Table 11. QFN16 – 16-lead, Quad, Flat Package, No Lead, 3x3mm body size, Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.90	0.80	1.00	0.035	0.032	0.039
A1	0.02	0.00	0.05	0.001	0.000	0.002
A3	0.20	–	–	0.008	–	–
b	0.25	0.18	0.30	0.010	0.007	0.012
D	3.00	2.90	3.10	0.118	0.114	0.122
D2	1.70	1.55	1.80	0.067	0.061	0.071
E	3.00	2.90	3.10	0.118	0.114	0.122
E2	1.70	1.55	1.80	0.067	0.061	0.071
e	0.50	–	–	0.020	–	–
K	0.20	–	–	0.008	–	–
L	0.40	0.30	0.50	0.016	0.012	0.020
ddd	–	0.08	–	–	0.003	–
Ch	–	0.33	–	–	0.013	–
N	16			16		

Figure 15. QFN16 – 16-lead, Quad, Flat Package, No Lead, 3x3mm, Recommended Footprint



Note: Substrate pad should be tied to V_{SS}.

PART NUMBERING

Table 12. Ordering Information Scheme

Example: M41T 50 Q 6 F

Device Family

M41T

Device Type and Supply Voltage

50 = V_{CC} = 1.7V to 3.6V

Package

Q = QFN16

Temperature Range

6 = –40°C to 85°C

Shipping Method for SOIC

F = Lead-free Package (ECOPACK®), Tape & Reel

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

REVISION HISTORY

Table 13. Document Revision History

Date	Version	Revision Details
December 12, 2003	1.0	First Edition
25-Dec-03	1.1	Add crystal isolation, footprint (Figure 13)
15-Jan-04	1.2	Update characteristics (Figure 2, 3, 13; Table 2, 4, 9, 11, 12)
27-Feb-04	1.3	Update characteristics, mechanical information (Figure 4, 14, 15; Table 6, 9, 11)
02-Mar-04	1.4	Update characteristics (Table 7, 9, 10, 12)
26-Apr-04	2.0	Reformat and publish
13-May-04	3.0	Update characteristics (Table 6, 9, 10; Figure 2, 3, 15)
18-Jan-05	4.0	Update characteristics (Figure 4; Table 2, 7, 9)