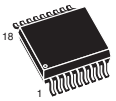
M41T82
M41T83

Serial I²C bus RTC with battery switchover

Features

- Ultra-low battery supply current of 365nA
- Factory calibrated accuracy ±5PPM guaranteed after 2 reflows (SOX18)
  - Much better accuracies achievable using built-in programmable analog and digital calibration circuits
- 2.0V to 5.5V clock operating voltage
- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- Automatic switchover and reset output circuitry (fixed reference)
  - M41T83S
    V_{CC} = 3.00V to 5.50V
    (2.85V ≤ V_{RST} ≤ 3.00V)
  - M41T83R
    V_{CC} = 2.70V to 5.50V
    (2.55V ≤ V_{RST} ≤ 2.70V)
  - M41T83Z
    V_{CC} = 2.38V to 5.50V
    (2.25V ≤ V_{RST} ≤ 2.38V)
- Serial interface supports I²C Bus (400kHz protocol)
- Programmable alarm with interrupt function (valid even during battery back-up mode)
- Optional 2nd programmable alarm available
- Square wave output defaults to 32KHz on power-up (M41T83 only)
- RESET ($\overline{RST}$) output
- Watchdog timer
- Programmable 8-bit counter/timer
- 7 bytes of battery-backed user SRAM
- Battery low flag
- Power-down time stamp (HT bit)
- Low operating current of 80µA

QFN16, 4mm x 4mm (QA)
(VFQFPN16)



SOX18 (MY, 18-pin, 300mil SOIC with embedded crystal)[1]

SO8 (M)

1. Contact local ST sales office for availability of SOX18 package.

- Oscillator stop detection
- Battery or Super-cap™ back-up
- Operating temperature of –40°C to 85°C
- Package options include:
  - a 16-lead QFN (M41T83),
  - an 18-lead embedded crystal SOIC (M41T83), or
  - an 8-lead SOIC (M41T82)
- RoHS compliance: lead-free components are compliant with the RoHS directive

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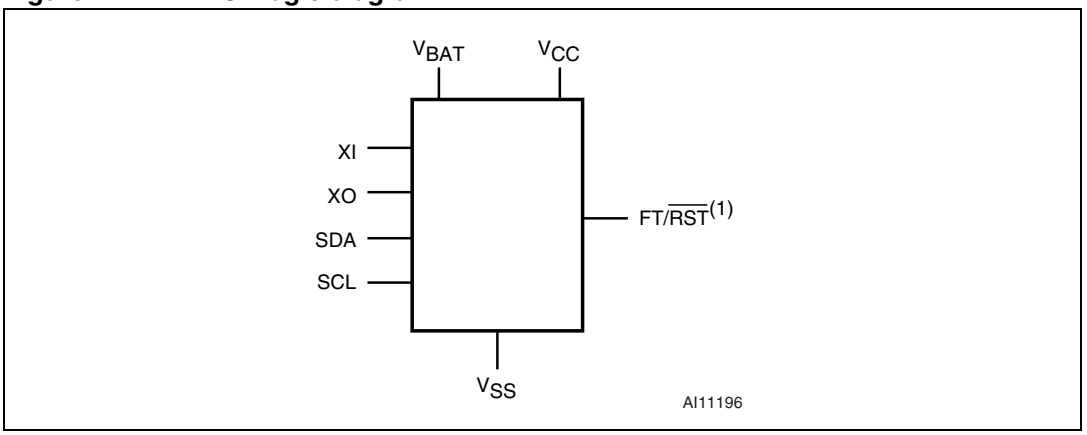
1 Description

The M41T8x are low power serial I^2C real-time clocks with a built-in 32.768kHz oscillator (external crystal-controlled for the QFN16 and SO8 packages, embedded crystal for the SOX18 package). Eight bytes of the Register Map (see *Table 2 on page 23*) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 17 bytes of the Register Map provide status/control of the two Alarms, Watchdog, 8-bit Counter, and Square Wave functions. An additional seven bytes are made available as user SRAM.

Addresses and data are transferred serially via a two line, bi-directional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41T8x has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the clock operations can be supplied by a small lithium button battery when a power failure occurs.

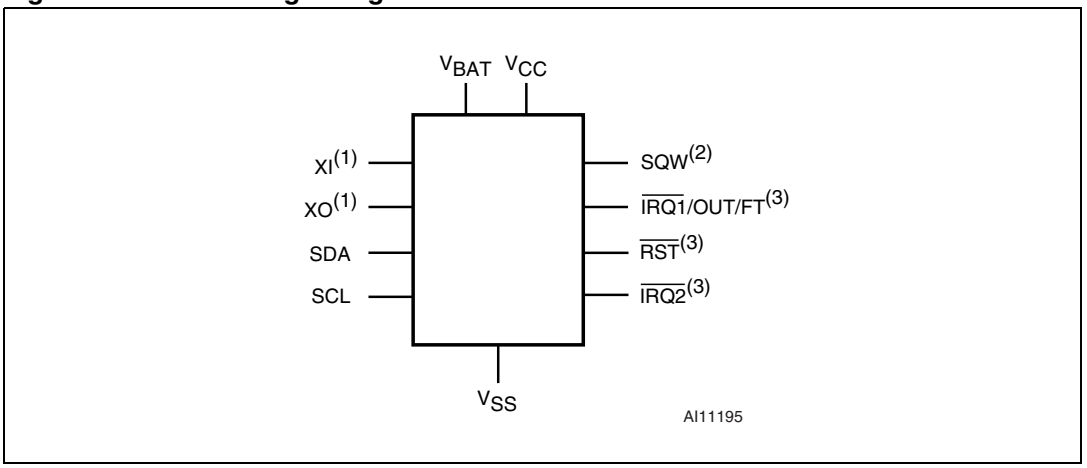
Functions available to the user include a non-volatile, time-of-day clock/calendar, two Alarm interrupts, Watchdog Timer, programmable 8-bit Counter, and Square Wave outputs. The eight clock address locations contain the century, year, month, date, day, hour, minute, second, and tenths/hundredths of a second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. The M41T83 is supplied in either a QFN16 (QA) or an SOX18 (MY), 300mil SOIC which includes an embedded 32KHz crystal. The SOX18 package requires only a user-supplied battery to provide non-volatile operation. The M41T82 is available only in an SO8 package.

Figure 1. M41T82 logic diagram



1. Open drain

Figure 2. M41T83 logic diagram



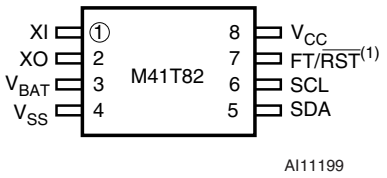
1. For QFN16 package only.
2. Defaults to 32KHz on power-up.
3. Open drain

Table 1. Signal names

Symbol	Description
XI(1)	32KHz oscillator input
XO(1)	32KHz oscillator output
$\overline{IRQ1}$/OUT/FT	Interrupt 1/output driver/frequency test output (open drain)
SQW(2)	32KHz programmable square wave output
$\overline{RST}$	Power-on reset output (open drain)
FT/$\overline{RST}$	Frequency test output/power-on reset (open drain - M41T82 only)
$\overline{IRQ2}$(3)	Interrupt for alarm 2 (open drain)
SDA	Serial data address input/output
SCL	Serial clock input
V_{BAT}	Battery supply voltage (tie V_{BAT} to V_{SS} if no battery is connected.)
DU(4)	Do not use
V_{CC}	Supply voltage
V_{SS}	Ground

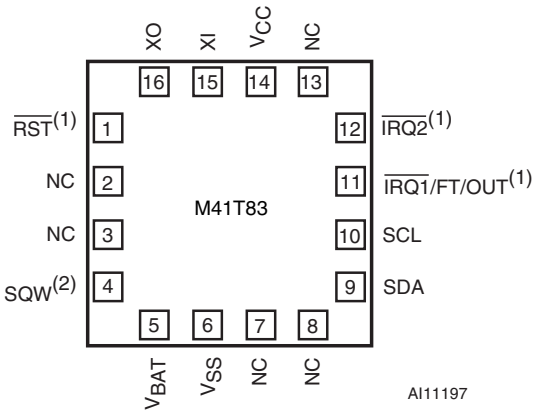
1. For SO8 and QFN16 packages only.
2. Defaults to 32KHz on power-up.
3. For SOX18 and QFN16 packages only.
4. DU pin must be tied to V_{CC}.

Figure 3. SO8 (M) connections (M41T82)



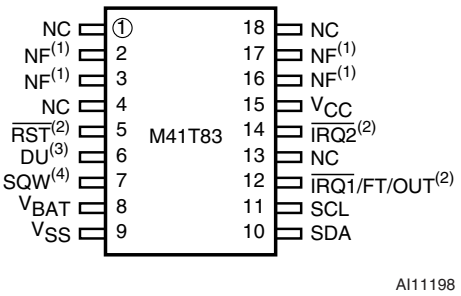
1. Open drain output

Figure 4. QFN16 (QA) connections (M41T83)



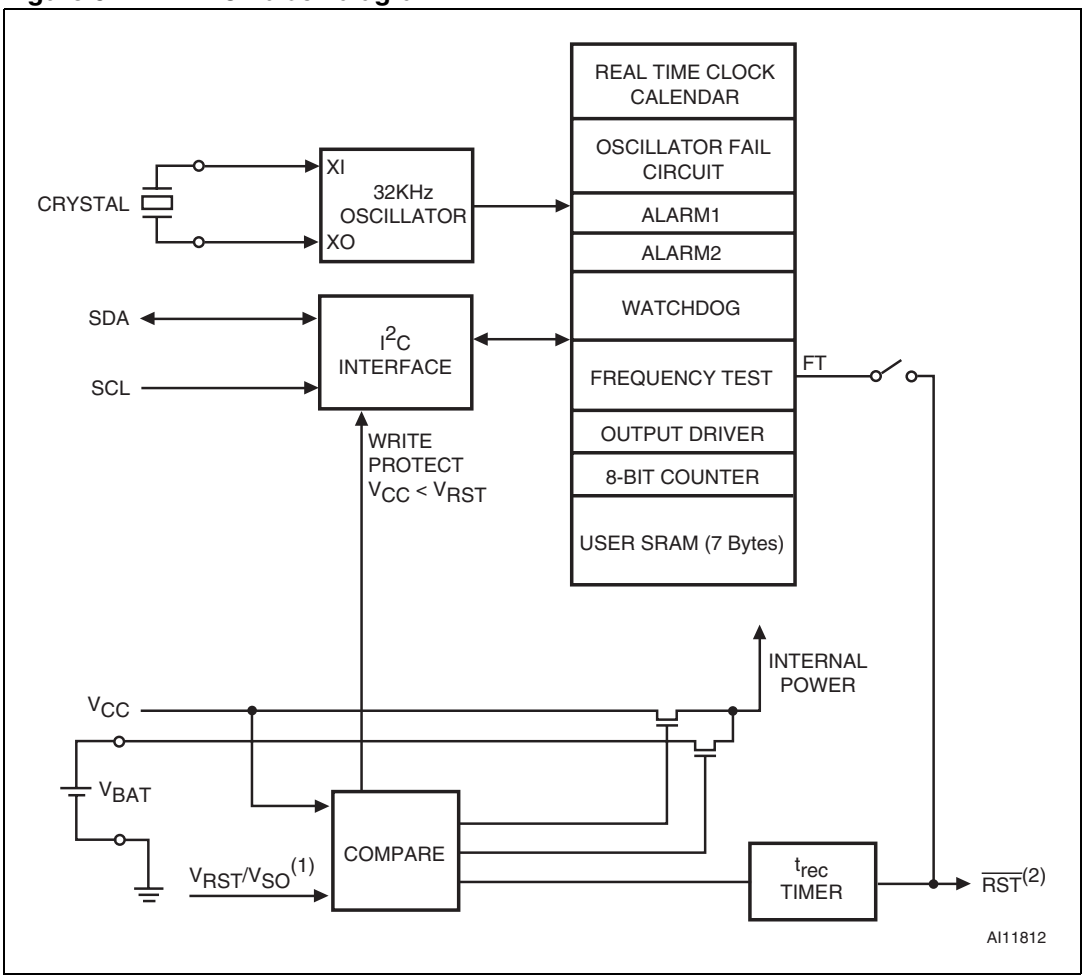
1. Open drain output
2. Defaults to 32Hz on Power-up.

Figure 5. SOX18 (MY) connections (M41T83)



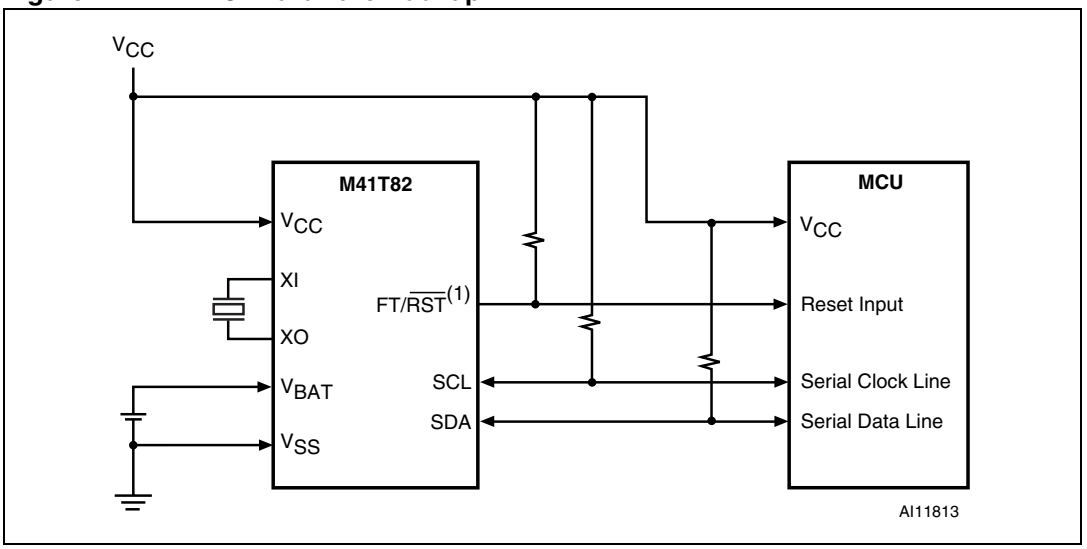
1. NF pins must be tied to V_{SS}. Pins 2 and 3, and 16 and 17 are internally shorted together.
2. Open drain output
3. Do not use (must be tied to V_{CC})
4. Defaults to 32KHz on power-up.

Figure 6. M41T82 block diagram



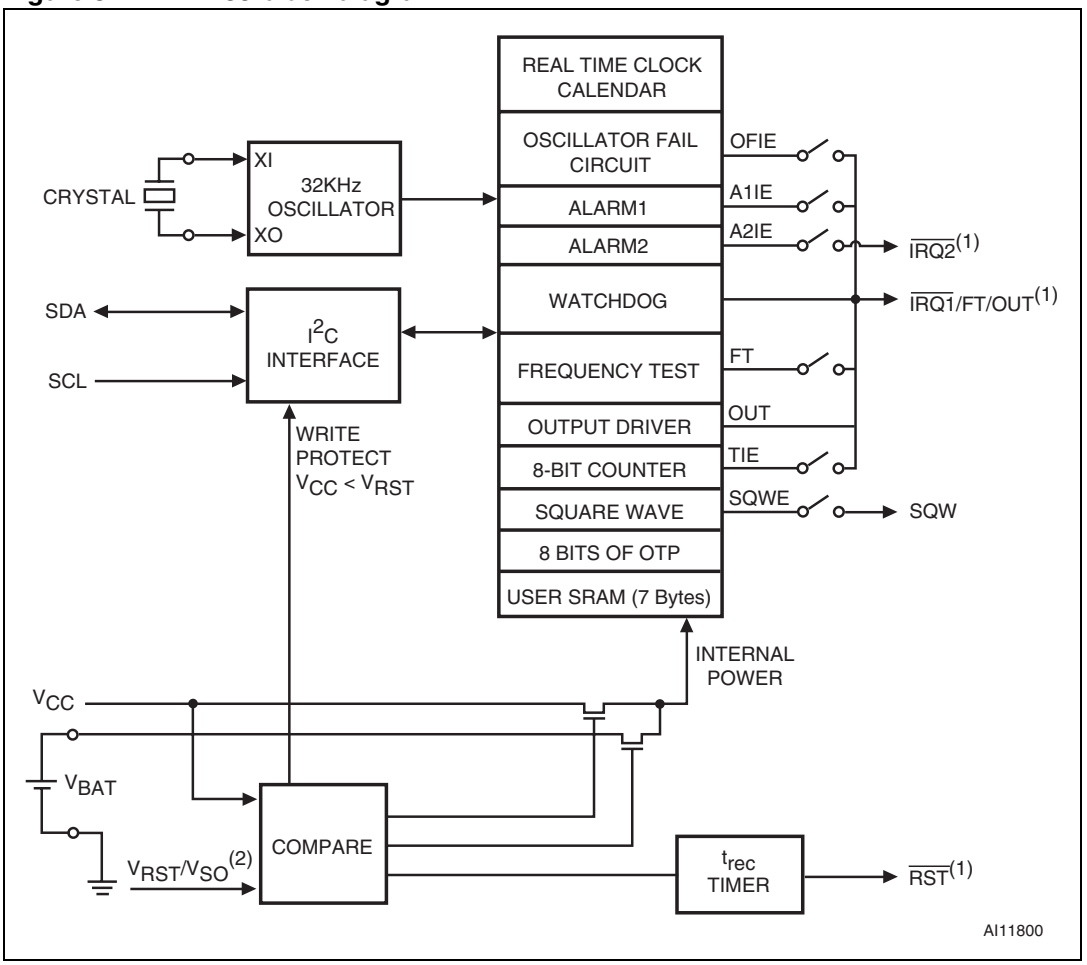
1. $V_{RST} = V_{SO}$ = 2.93V (S), 2.63V (R), and 2.32V (Z).
2. Open drain output

Figure 7. M41T82 hardware hookup



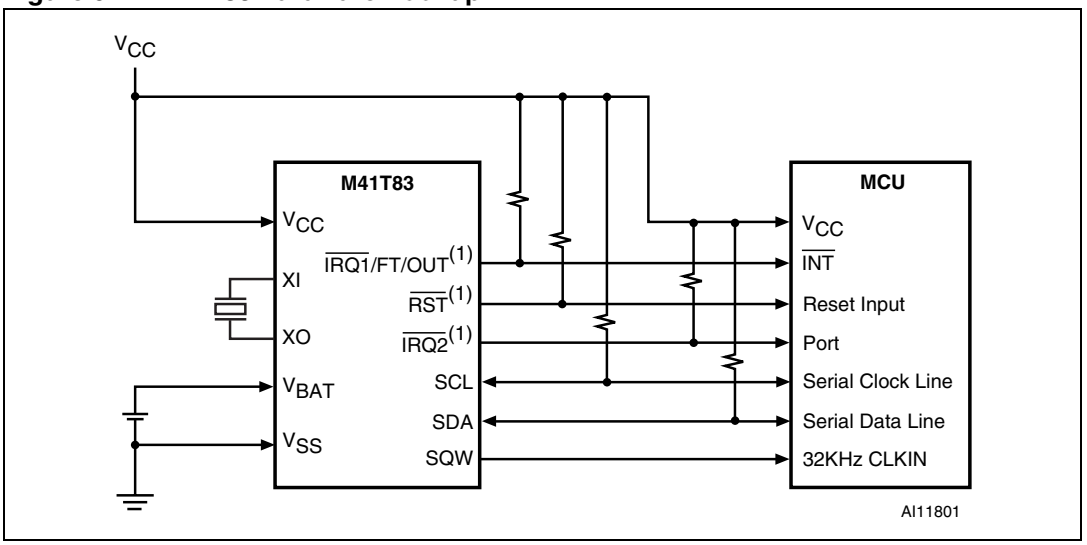
1. Open drain output

Figure 8. M41T83 block diagram



1. Open drain output
2. $V_{RST} = V_{SO}$ = 2.93V (S), 2.63V (R), and 2.32V (Z).

Figure 9. M41T83 hardware hookup



1. Open drain output

2 Operation

The M41T8x clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 32 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: tenths/hundredths of a second register
- 2nd byte: seconds register
- 3rd byte: minutes register
- 4th byte: century/hours register
- 5th byte: day register
- 6th byte: date register
- 7th byte: month register
- 8th byte: year register
- 9th byte: digital calibration register
- 10th byte: watchdog register
- 11th - 15th bytes: alarm 1 registers
- 16th byte: flags register
- 17th byte: timer value register
- 18th byte: timer control register
- 19th byte: analog calibration register
- 20th byte: square wave register
- 21st - 25th bytes: alarm 2 registers
- 26th - 32nd bytes: user RAM

The M41T8x clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{RST}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out-of-tolerance system. The power input will also be switched from the V_{CC} pin to the battery when V_{CC} falls below the battery back-up switchover voltage ($V_{SO} = V_{RST}$). At this time the clock registers will be maintained by the attached battery supply. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High.
- Changes in the data line, while the clock line is High, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain High.

2.1.2 Start data transfer

A change in the state of the data line, from high to Low, while the clock is High, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one Acknowledge bit. This Acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

Figure 10. Serial bus data transfer sequence

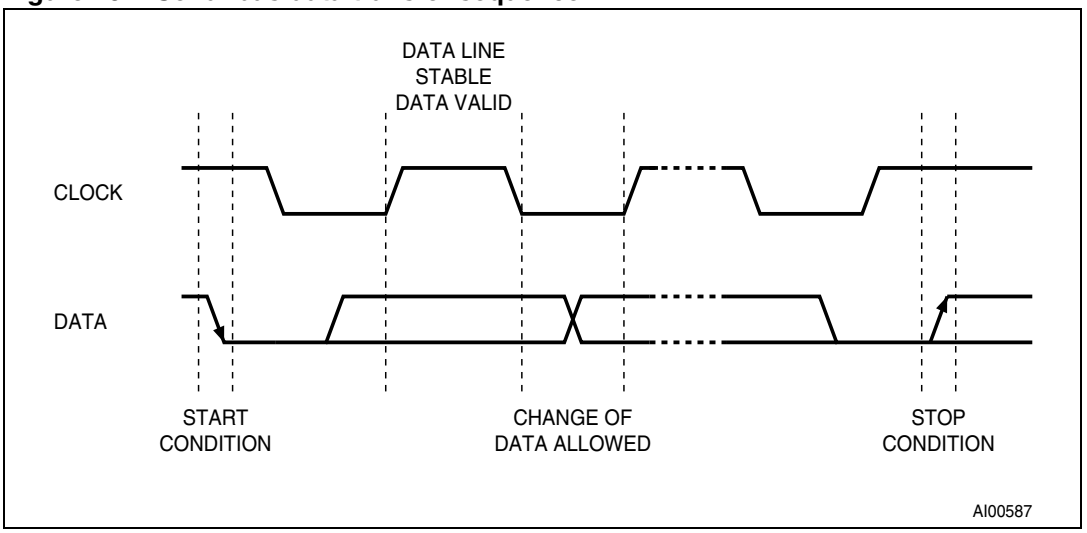
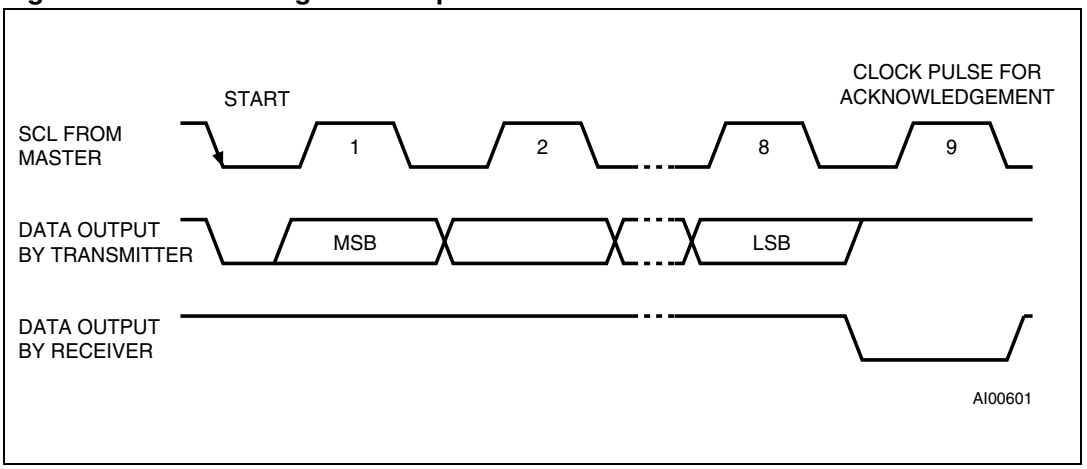


Figure 11. Acknowledgement sequence



2.2 Read mode

In this mode the master reads the M41T8x slave after setting the slave address (see *Figure 13 on page 18*). Following the WRITE Mode control bit (R/W = 0) and the Acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ Mode control bit (R/W = 1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an Acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an Acknowledge clock. The M41T8x slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to “An+2.”

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter. The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume due to a Stop Condition or when the pointer increments to any non-clock address (08h-1Fh).

Note: This is true both in READ Mode and WRITE Mode.

An alternate READ Mode may also be implemented whereby the master reads the M41T8x slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 14 on page 18*).

Figure 12. Slave address location

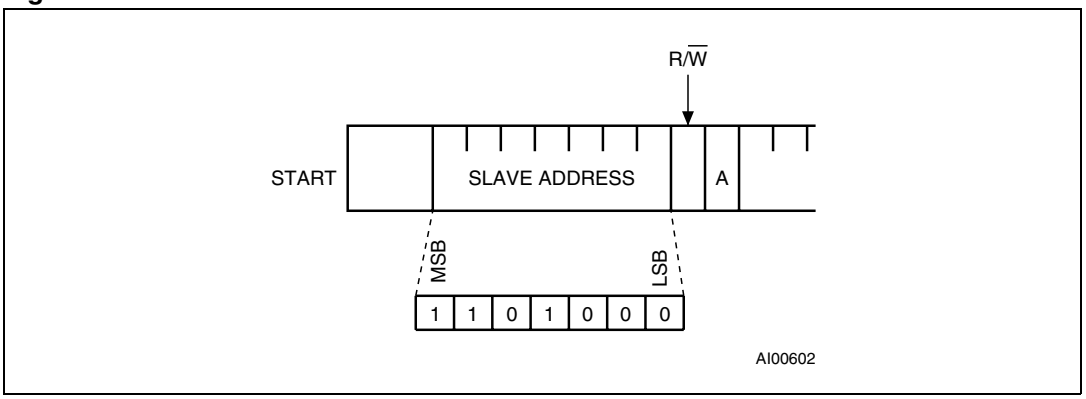


Figure 13. Read mode sequence

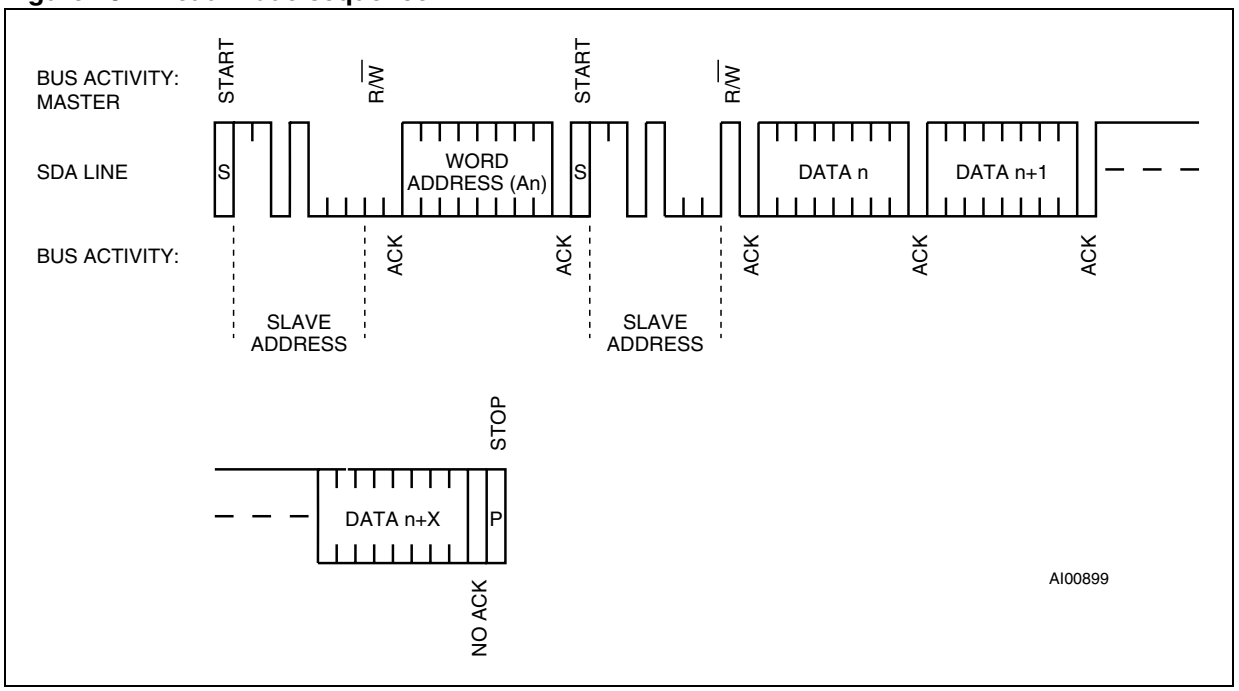
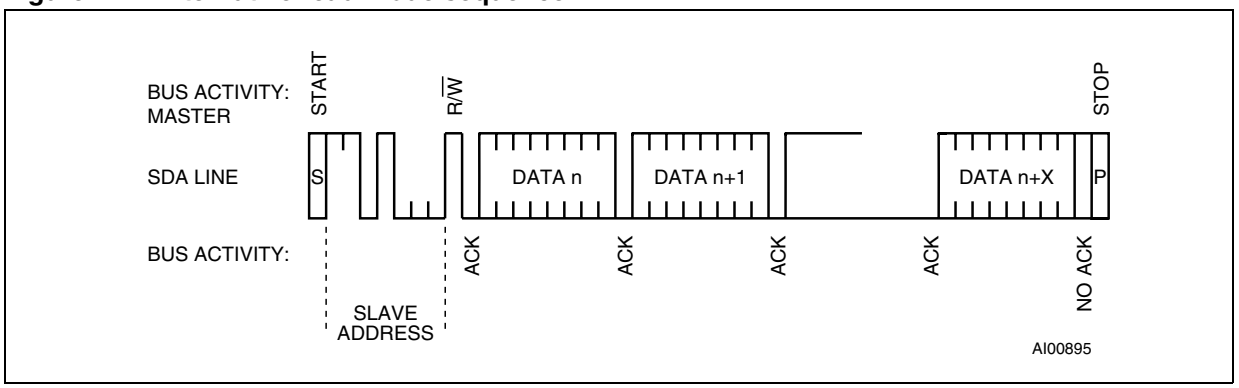


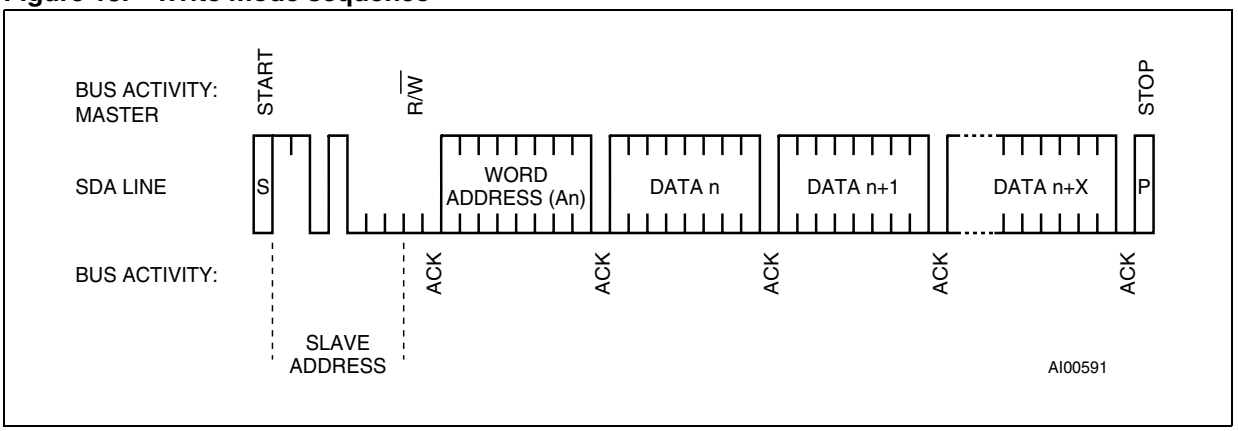
Figure 14. Alternative read mode sequence



2.3 Write mode

In this mode the master transmitter transmits to the M41T8x slave receiver. Bus protocol is shown in *Figure 15*. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T8x slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address see *Figure 12 on page 17* and again after it has received the word address and each data byte.

Figure 15. Write mode sequence



2.4 Data retention and battery switchover (V_{SO} = V_{RST})

Once V_{CC} falls below the switchover voltage (V_{SO} = V_{RST}), the device automatically switches over to the battery and powers down into an ultra low current mode of operation to preserve battery life. If V_{BAT} is less than, or greater than V_{RST}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{RST} (see *Figure 25 on page 48*). At this time the clock registers and user RAM will be maintained by the attached battery supply.

When it is powered back up, the device switches back from battery to V_{CC} at V_{SO} + hysteresis. When V_{CC} rises above V_{RST}, it will recognize the inputs. For more information on battery storage life refer to Application Note AN1012.

2.5 Power-on reset (t_{rec})

The M41T8x continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ output pulls low (open drain) and remains low after power-up for t_{rec} (210ms typical) after V_{CC} rises above V_{RST} (max).

Note: The t_{rec} period does not affect the RTC operation. Write protect only occurs when V_{CC} is below V_{RST}. When V_{CC} rises above V_{RST}, the RTC will be selectable immediately. Only the $\overline{RST}$ output is affected by the t_{rec} period.

The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control the rise time.

3 Clock operation

The M41T8x is driven by a quartz-controlled oscillator with a nominal frequency of 32.768kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The 8-byte clock register (see *Table 2 on page 23* and *Table 4 on page 25*) is used to both set the clock and to read the date and time from the clock, in binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a '0' the oscillator restarts within one second (typical).

Note: Upon initial power-up, the user should set the ST bit to a '1,' then immediately reset the ST bit to '0.' This provides an additional "kick-start" to the oscillator circuit.

Bits D6 and D7 of clock register 03h (century/ hours register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1). Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the digital calibration register, while the analog calibration register is found at address 12h (these are both described in the clock calibration section). For the M41T83, bit D7 of register 09h (Watchdog register) contains the Oscillator Fail Interrupt Enable bit (OFIE). When the user sets this bit to '1,' any condition which sets the Oscillator Fail bit (OF) (see *Section 3.13: Oscillator fail detection on page 42*) will also generate an interrupt output.

Note: A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the ST bit and CB0-CB1 bits will result in an update of the system clock and a reset of the divider chain. This could result in an inadvertent change of the current time. These non-clock related bits should be written prior to setting the clock, and remain unchanged until such time as a new clock time is also written.

The eight clock registers may be read one byte at a time, or in a sequential block. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.1 Power-down time-stamp

When a power failure occurs, the Halt Update bit (HT) will automatically be set to a "1". This will prevent the clock from updating the clock registers, and will allow the user to read the exact time of the power-down event. Resetting the HT bit to a "0" will allow the clock to update the clock with the current time. For more information, see Application note AN1572.

3.2 Clock/control register map

The M41T8x offers 32 internal registers which contain clock, calibration (digital and analog), Alarm 1 and 2, Watchdog, Flags, Timer, and Square Wave (M41T83 only). The clock registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER® cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address (00h to 07h). The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). The update will resume either due to a Stop Condition or when the pointer increments to a non-clock address. Clock and alarm registers store data in BCD format. Calibration, Timer, Watchdog, and Square Wave bits are written in a binary format.

Table 2. M41T82 clock/control register map (32 bytes)(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				seconds	00-99
01h	ST	10 seconds			seconds				seconds	00-59
02h	0	10 minutes			minutes				minutes	00-59
03h	CB1	CB0	10 hours		Hours (24 hour format)				Century/hours	0-3/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	0	FT	DCS	DC4	DC3	DC2	DC1	DC0	Digital calibration	
09h	0	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	0	0	ABE	AI1 10M	Alarm1 month				AI1 month	01-12
0Bh	RPT14	RPT15	AI1 10 date		Alarm1 date				AI1 date	01-31
0Ch	RPT13	HT	AI1 10 hour		Alarm1 hour				AI1 hour	00-23
0Dh	RPT12	Alarm1 10 minutes			Alarm1 minutes				AI1 min	00-59
0Eh	RPT11	Alarm1 10 seconds			Alarm1 seconds				AI1 sec	00-59
0Fh	WDF	AF1	AF2(2)	BL	TF	OF	0	0	Flags	
10h	Timer countdown value								Timer value	
11h	TE	0	0	0	0	0	TD1	TD0	Timer control	
12h	ACS	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Analog calibration	
13h	0	0	0	0	0	0	AL2E	0	SQW	
14h	0	0	0	AI2 10M	Alarm2 month				SRAM/AI2 month	01-12
15h	RPT24	RPT25	AI2 10 date		Alarm2 month				SRAM/AI2 date	01-31
16h	RPT23	0	AI2 10 hour		Alarm2 date				SRAM/AI2 hour	00-23
17h	RPT22	Alarm2 10 minutes			Alarm2 minutes				SRAM/AI2 min	00-59
18h	RPT21	Alarm2 10 seconds			Alarm2 seconds				SRAM/AI2 sec	00-59
19h-1Fh	User SRAM (7 bytes)								SRAM	

1. See *Table 3: Key to Table 2: M41T82 clock/control register map (32 bytes)*
2. AF2 will always read '0', if the AL2E bit is set to '0'.

Table 3. Key to *Table 2: M41T82 clock/control register map (32 bytes)*

Code	Explanation
0	Must be set to zero
ABE	Alarm in battery back-up enable bit
AC0-AC6	Analog calibration bits
ACS	Analog calibration sign bit
AF1, AF2	Alarm flag bits
AL2E	Alarm 2 enable bit
BL	Battery low bit
BMB0-BMB4	Watchdog multiplier bits
CB0, CB1	Century bits
DC0-DC4	Digital calibration bits
DCS	Digital calibration Sign bit
FT	Frequency test bit
HT	Halt update bit
OF	Oscillator fail bit
RB0-RB2	Watchdog resolution bits
RPT11-RPT15	Alarm 1 repeat mode bits
RPT21-RPT25	Alarm 2 repeat mode bits
ST	Stop bit
TD0, TD1	Timer frequency bits
TE	Timer enable bit
TF	Timer flag
WDF	Watchdog flag

Table 4. M41T83 clock/control register map (32 bytes)(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				seconds	00-99
01h	ST	10 seconds			seconds				seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CB1	CB0	10 hours		Hours (24 hour format)				Century/hours	0-3/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	OUT	FT	DCS	DC4	DC3	DC2	DC1	DC0	Digital calibration	
09h	OFIE	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	A1IE	SQWE	ABE	AI1 10M	Alarm 1month				AI1 month	01-12
0Bh	RPT14	RPT15	AI1 10 date		Alarm1 date				AI1 date	01-31
0Ch	RPT13	HT	AI1 10 hour		Alarm1 hour				AI1 hour	00-23
0Dh	RPT12	Alarm1 10 minutes			Alarm1 minutes				AI1 min	00-59
0Eh	RPT11	Alarm1 10 seconds			Alarm1 seconds				AI1 sec	00-59
0Fh	WDF	AF1	AF2(2)	BL	TF	OF	0	0	Flags	
10h	Timer countdown value								Timer value	
11h	TE	$\overline{TI}$/TP	TIE	0	0	0	TD1	TD0	Timer control	
12h	ACS	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Analog calibration	
13h	RS3	RS2	RS1	RS0	0	0	AL2E	OTP	SQW	
14h	A2IE	0	0	AI2 10M	Alarm2 month				SRAM/AI2 month	01-12
15h	RPT24	RPT25	AI2 10 date		Alarm2 date				SRAM/AI2 date	01-31
16h	RPT23	0	AI2 10 hour		Alarm2 hour				SRAM/AI2 hour	00-23
17h	RPT22	Alarm2 10 minutes			Alarm2 minutes				SRAM/AI2 min	00-59
18h	RPT21	Alarm2 10 seconds			Alarm2 seconds				SRAM/AI2 sec	00-59
19h-1Fh	User SRAM (7 bytes)								SRAM	

1. See *Table 5: Key to Table 4: M41T83 clock/control register map (32 bytes)*.
2. AF2 will always read '0', if the AL2E bit is set to '0'.

Table 5. Key to *Table 4: M41T83 clock/control register map (32 bytes)*

Code	Explanation
0	Must be set to zero
ABE	Alarm in battery back-up enable bit
A1IE, A2IE	Alarm interrupt enable bits
AC0-AC6	Analog calibration bits
ACS	Analog calibration sign bit
AF1, AF2	Alarm flag
AL2E	Alarm 2 enable bit
BL	Battery low bit
BMB0-BMB4	Watchdog multiplier bits
CB0, CB1	Century bits
DC0-DC4	Digital calibration bits
DCS	Digital calibration Sign bit
FT	Frequency test bit
HT	Halt update bit
OF	Oscillator fail bit
OUT	Output level
OFIE	Oscillator fail interrupt enable
OTP	OTP control bit
RB0-RB2	Watchdog resolution bits
RPT11-RPT15	Alarm 1 repeat mode bits
RPT21-RPT25	Alarm 2 repeat mode bits
RS0-RS3	SQW frequency
SQWE	Square wave enable
SRAM/$\overline{\text{ALM2}}$	SRAM/alarm 2 bit
ST	Stop bit
TD0, TD1	Timer frequency bits
TE	Timer enable bit
TF	Timer flag
$\overline{\text{TI}}$/TP	Timer interrupt or pulse
TIE	Timer interrupt enable
WDF	Watchdog flag

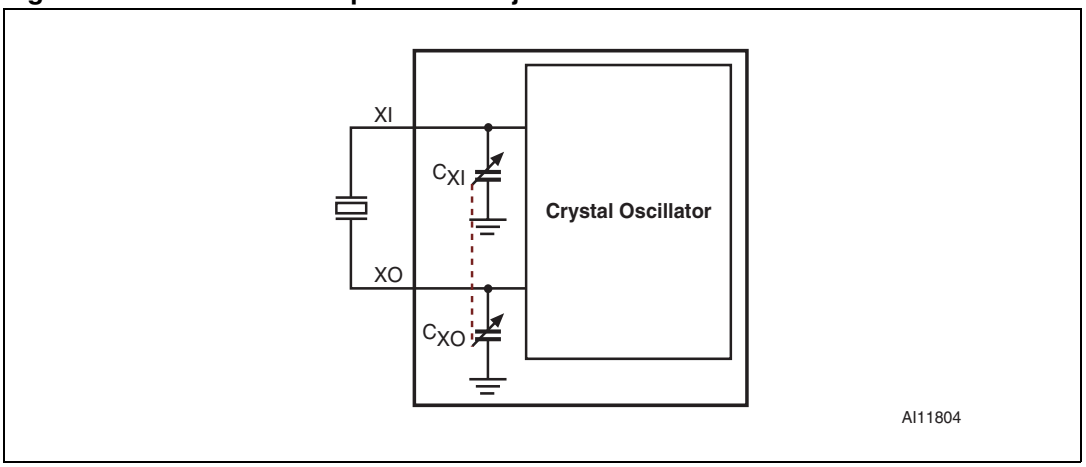
3.3 Real-time clock accuracy

The M41T8x is driven by a quartz controlled oscillator with a nominal frequency of 32,768Hz. The accuracy of the real-time clock is dependent upon the accuracy of the crystal, and the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Temperature also affects the crystal frequency, causing additional error (see *Figure 17 on page 31*).

The M41T8x provides the option of clock correction through either manufacturing calibration or in-application calibration. The total possible compensation is typically –93 ppm to +156 ppm. The two compensation circuits that are available are:

1. An Analog Calibration register (12h) can be used to adjust internal (on-chip) load capacitors for oscillator capacitance trimming. The individual load capacitors C_{XI} and C_{XO} (see *Figure 16*), are selectable from a range of –18pF to +9.75pF in steps of 0.25pF. This translates to a calculated compensation of approximately ±30 ppm (see *Section 3.4.2: Analog calibration (programmable load capacitance) on page 30*).
2. A Digital Calibration register (08h) can also be used to adjust the clock counter by adding or subtracting a pulse at the 512Hz divider stage. This approach provides periodic compensation of approximately –63 ppm to +126 ppm (see *Section 3.4.1: Digital calibration (periodic counter correction) on page 28*).

Figure 16. Internal load capacitance adjustment



3.4 Clock calibration

The M41T8x oscillator is designed for use with a 12.5pF crystal load capacitance. When the calibration circuit is properly employed, accuracy improves to better than ±1 ppm at 25°C.

The M41T8x design provides the following two methods for clock error correction.

3.4.1 Digital calibration (periodic counter correction)

This method employs the use of periodic counter correction by adjusting the ratio of the 100Hz divider stage to the 512Hz divider stage. Under normal operation, the 100Hz divider stage outputs precisely 100 pulses for every 512 pulses of the 512Hz input stage to provide the input frequency to the Fraction of Seconds Clock register. By adjusting the number of 512Hz input pulses used to generate 100 output pulses, the clock can be sped up or slowed down, as shown in *Figure 19 on page 34*.

When a non-zero value is loaded into the five Calibration bits (DC4 – DC0) found in the Digital Calibration Register (08h) and the sign bit is ‘1’, (indicating positive calibration), the 100Hz stage outputs 100 pulses for every 511 input pulses instead of the normal 512. Since the 100 pulses are now being output in a shorter window, this has the effect of speeding up the clock by 1/512 seconds for each second the circuit is active. Similarly, when the sign bit is ‘0’, indicating negative calibration, the block outputs 100 pulses for every 513 input pulses. Since the 100 pulses are then being output in a longer window, this has the effect of slowing down the clock by 1/512 seconds for each second the circuit is active.

The amount of calibration is controlled by using the value in the calibration register (N) to generate the adjustment in one second increments. This is done for the first N seconds once every *eight* minutes for positive calibration, and for N seconds once every *sixteen* minutes for negative calibration (see *Table 6 on page 29*).

For example, if the Calibration register is set to '100010,' then the adjustment will occur for two seconds in every minute. Similarly, if the calibration register is set to '000011,' then the adjustment will occur for 3 seconds in every alternating minute.

The Digital Calibration bits (DC4 – DC0) occupy the five lower order bits in the Digital Calibration Register (08h). These bits can be set to represent any value between 0 and 31 in binary form. The sixth bit (DCS) is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within an 8-minute (positive) or 16-minute (negative) cycle. Therefore, each calibration step has an effect on clock accuracy of +4.068 or –2.034 ppm. Assuming that the oscillator is running at exactly 32,768Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month, which corresponds to a total range of +5.5 or –2.75 minutes per month.

Note: 1 The modified pulses are not observable on the Frequency Test (FT) output, nor will the effect of the calibration be measurable real-time, due to the periodic nature of the error compensation.

2 Positive digital calibration is performed on an eight minute cycle, therefore the value in the calibration register should not be modified more frequently than once every eight minutes for positive values of calibration. Negative digital calibration is performed on a sixteen minute cycle, therefore negative values in the calibration register should not be modified more frequently than once every sixteen minutes.

Table 6. Digital calibration values

Calibration value (binary)	Calibration value rounded to the nearest ppm	
DC4 – DC0	Negative calibration (DCS = 0)	Positive calibration (DCS = 1)
0 (00000)	0	0
1 (00001)	-2	4
2 (00010)	-4	8
3 (00011)	-6	12
4 (00100)	-8	16
5 (00101)	-10	20
6 (00110)	-12	24
7 (00111)	-14	28
8 (01000)	-16	33
9 (01001)	-18	37
10 (01010)	-20	41
11 (01011)	-22	45
12 (01100)	-24	49
13 (01101)	-26	53
14 (01110)	-28	57
15 (01111)	-31	61
16 (10000)	-33	65
17 (10001)	-35	69
18 (10010)	-37	73
19 (10011)	-39	77
20 (10100)	-41	81
21 (10101)	-43	85
22 (10110)	-45	90
23 (10111)	-47	94
24 (11000)	-49	98
25 (11001)	-51	102
26 (11010)	-53	106
27 (11011)	-55	110
28 (11100)	-57	114
29 (11101)	-59	118
30 (11110)	-61	122
31 (11111)	-63	126
N	N/491520 (per minute)	N/245760 (per minute)

3.4.2 Analog calibration (programmable load capacitance)

A second method of calibration employs the use of programmable internal load capacitors to adjust (or trim) the oscillator frequency.

By design, the oscillator is intended to be 0 ppm ± crystal accuracy at room temperature (25°C, see *Figure 17 on page 31*). For a 12.5pF crystal, the default loading on each side of the crystal will be 25pF. For incrementing or decrementing the calibration value, capacitance will be added or removed in increments of 0.25pF to each side of the crystal.

Internally, C_{LOAD} of the oscillator is changed via two digitally controlled capacitors, C_{XI} and C_{XO}, connected from the XI and XO pins to ground (see *Figure 16 on page 27*). The effective on-chip series load capacitance, C_{LOAD}, ranges from 3.5pF to 17.4pF, with a nominal value of 12.5pF (AC0-AC6 = '0').

The effective series load capacitance (C_{LOAD}) is the combination of C_{XI} and C_{XO}:

$$C_{LOAD} = 1/(1/C_{XI} + 1/C_{XO})$$

Seven analog calibration bits, AC0 to AC6, are provided in order to adjust the on-chip load capacitance value for frequency compensation of the RTC. Each bit has a different weight for capacitance adjustment. An Analog Calibration Sign (ACS) bit determines if capacitance is added (ACS bit = '0', negative calibration) or removed (ACS bit = '1', positive calibration). The majority of the calibration adjustment is positive (i.e. to increase the oscillator frequency by removing capacitance) due to the typical characteristic of quartz crystals to slow down due to changes in temperature, but negative calibration is also available.

Since the Analog Calibration Register adjustment is essentially "pulling" the frequency of the oscillator, the resulting frequency changes will not be linear with incremental capacitance changes. The equations which govern this mechanism indicate that smaller capacitor values of Analog Calibration adjustment will provide larger increments. Thus, the larger values of Analog Calibration adjustment will produce smaller incremental frequency changes. These values typically vary from 6-10 ppm/bit at the low end to <1 ppm/bit at the highest capacitance settings. The range provided by the Analog Calibration Register adjustment with a typical surface mount crystal is approximately ±30 ppm around the AC6-AC0 = 0 default setting because of this property (see *Table 7 on page 31*).

Figure 17. Crystal accuracy across temperature

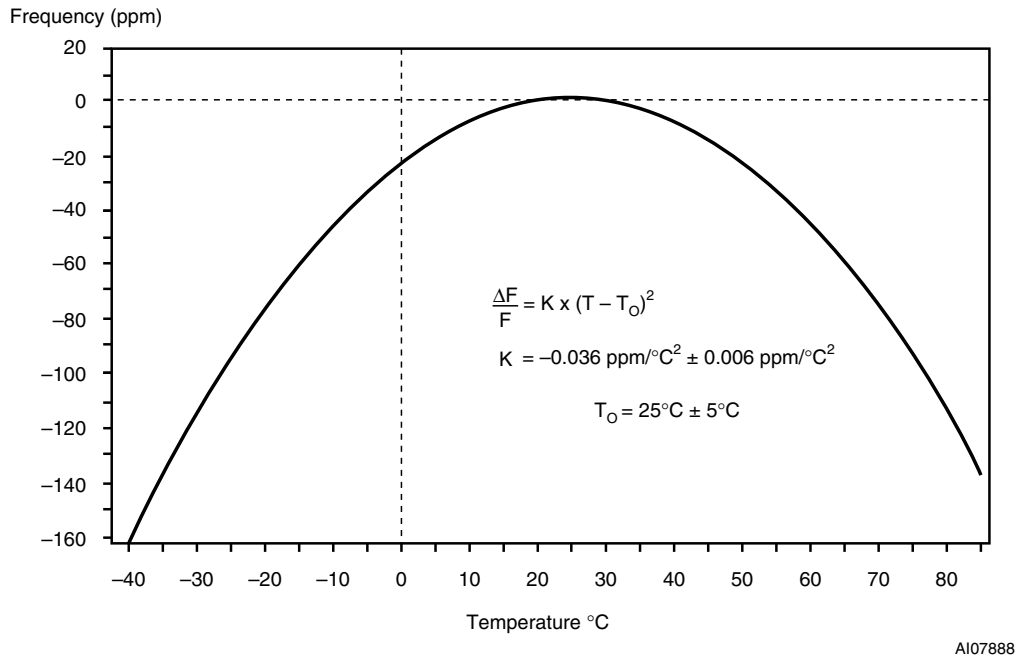


Table 7. Analog calibration values

Addr	Analog calibration value	D7	D6	D5	D4	D3	D2	D1	D0	C_{XI}, C_{XO}	C_{LOAD}(1)
		ACS (±)	AC6 (16pF)	AC5 (8pF)	AC4 (4pF)	AC3 (2pF)	AC2 (1pF)	AC1 (0.5pF)	AC0 (0.25pF)		½(C_{XI}, C_{XO})
12h	0pF	x	0	0	0	0	0	0	0	25pF	12.5pF
	3pF	0	0	0	0	1	1	0	0	28pF	14pF
	5pF	0	0	0	1	0	1	0	0	30pF	15pF
	–7pF	1	0	0	1	1	1	0	0	18pF	9pF
	9.75pF(2))	0	0	1	0	0	1	1	1	34.75pF	17.4pF
	–18pF(3)	1	1	0	0	1	0	0	0	7pF	3.5pF

1. $C_{LOAD} = 1/(1/C_{XI} + 1/C_{XO})$
2. Maximum negative calibration value
3. Maximum positive calibration value

The on-chip capacitance can be calculated as follows:

$$C_{LOAD} = \frac{1}{2}[(AC6-AC0\ value,\ decimal) \times 0.25pF] + 25pF$$

For example:

- C_{LOAD} (12h = x0000000) = 12.5pF,
- C_{LOAD} (12h =11001000) = 3.5pF, and
- C_{LOAD} (12h = 00100111) = 17.4pF.

The oscillator sees a minimum of 3.5pF with no programmable load capacitance selected.

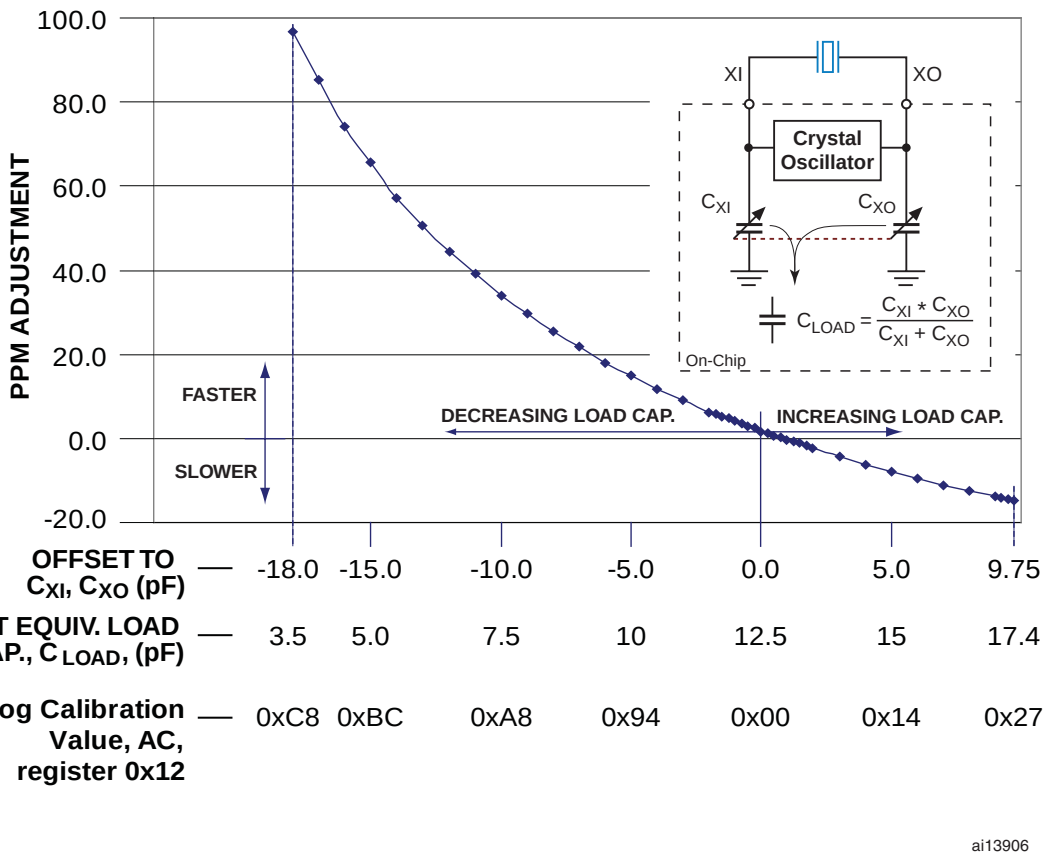
Note: These are typical values, and the total load capacitance seen by the crystal will include approximately 1-2pF of package and board capacitance in addition to the Analog Calibration register value.

Any invalid value of Analog Calibration will result in the default capacitance of 25pF.

The combination of analog and digital trimming can give up to –93 to +156 ppm of the total adjustment.

Figure 18 on page 33 represents a typical curve of clock ppm adjustment versus the Analog Calibration value. This curve may vary with different crystals, so it is good practice to evaluate the crystal to be used with an M41T8x device before establishing the adjustment values for the application in question.

Figure 18. Clock accuracy vs. on-chip load capacitance



Two methods are available for ascertaining how much calibration a given M41T8x may require:

- The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses either or both of the Calibration bytes.
- The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ1}}$/FT/OUT pin. The $\overline{\text{IRQ1}}$/FT/ OUT pin will toggle at 512Hz when FT and OUT bits = '1' (M41T83 only) and ST = '0.' Any deviation from 512Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124Hz would indicate a +20 ppm oscillator frequency error, requiring either a –10 (xx001010) to be loaded into the Digital Calibration byte, or +6pF (00011000) into the Analog Calibration byte for correction.

Note: Setting or changing the Digital Calibration byte does not affect the Frequency Test, Square Wave, or Watchdog Timer frequency, but changing the Analog Calibration byte DOES affect all functions derived from the low current oscillator (see Figure 19).

Figure 19. Clock divider chain and calibration circuits

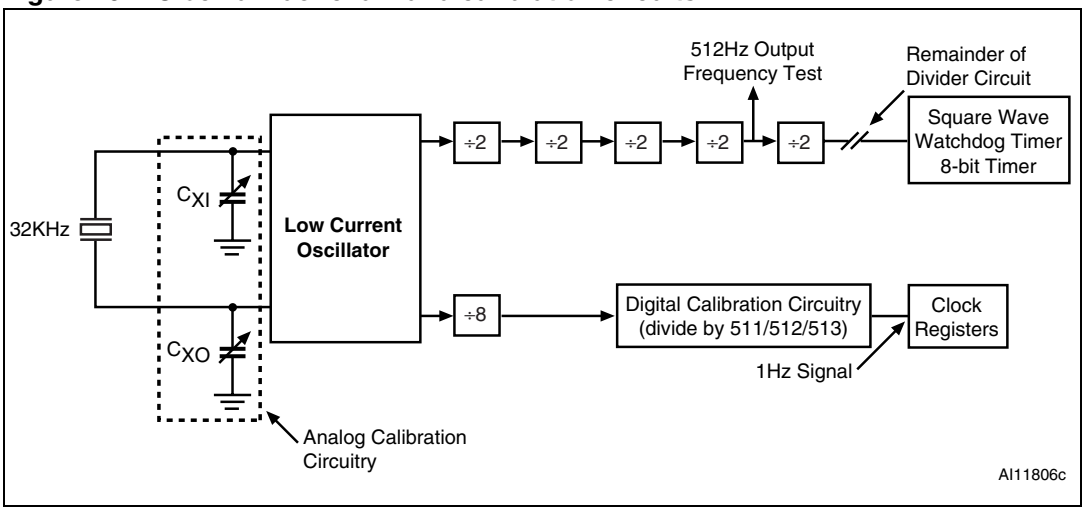
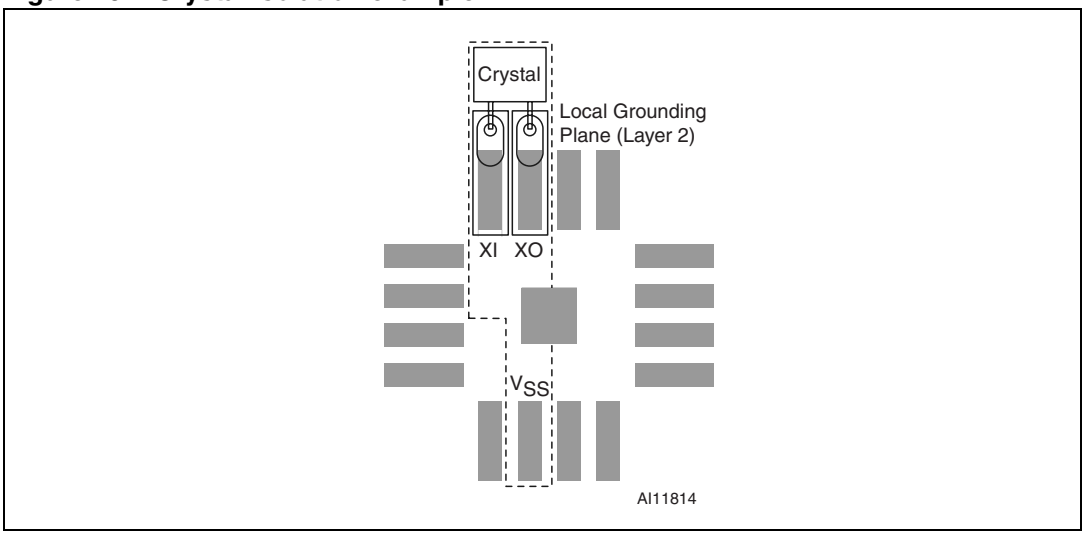


Figure 20. Crystal isolation example



1. Substrate pad should be tied to V_{SS}.

3.5 Setting the alarm clock registers

Address locations 0Ah-0Eh (Alarm 1) and 14h-18h (Alarm 2) contain the alarm settings. Either alarm can be configured independently to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. Bits RPT15–RPT11 and RPT25-RPT21 put the alarms in the repeat mode of operation. *Table 8 on page 37* shows the possible bit configurations.

Codes not listed in the table default to the once-per-second mode to quickly alert the user of an incorrect alarm setting. When the clock information matches the alarm clock settings based on the match criteria defined by RPT15–RPT11 and/or RPT25-RPT21, AF1 (Alarm 1 Flag) or AF2 (Alarm 2 Flag) is set. If A1IE (Alarm 1 Interrupt Enable), or A2IE (Alarm 2 Interrupt Enable) are also set, the alarm condition activates either the $\overline{IRQ1}$/FT/OUT, or $\overline{IRQ2}$ output pins. To disable either of the alarms, write a '0' to the Alarm Date Registers and to the RPTx5–RPTx1 bits.

Note: If the address pointer is allowed to increment to the Flag Register address, or the last address written is "Alarm Seconds," the address pointer will increment to the Flag address, and an alarm condition will not cause the Interrupt/Flag to occur until the address pointer is moved to a different address.

The $\overline{IRQ}$ output is cleared by a READ to the Flags Register (0Fh) as shown in *Figure 21*. A subsequent READ of the Flags Register is necessary to see that the value of the Alarm Flag has been reset to '0.'.

3.6 Optional second programmable alarm

When the Alarm 2 Enable (AL2E) bit (D1 of address 13h) is set to a logic '1', registers 14h through 18h provide control for a second programmable alarm which operates in the same manner as the alarm function described above. The A2IE (Alarm 2 Interrupt Enable) bit allows the second alarm to trigger a separate interrupt output ($\overline{IRQ2}$).

The AL2E bit defaults on initial power-up to a logic '0' (Alarm 2 disabled). In this mode, the five address bytes (14h-18h) function as additional user SRAM, for a total of 12 bytes of user SRAM.

The $\overline{IRQ1}$/FT/OUT pin can also be activated in the battery back-up mode (see *Figure 22 on page 36*).

Figure 21. Alarm interrupt reset waveform

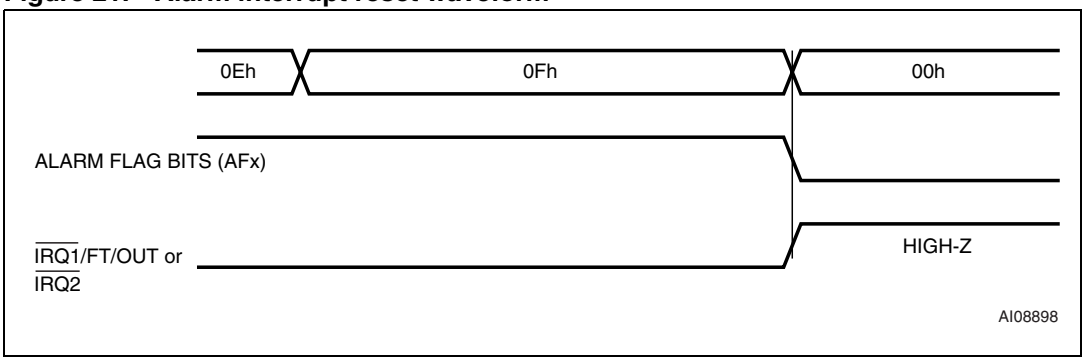
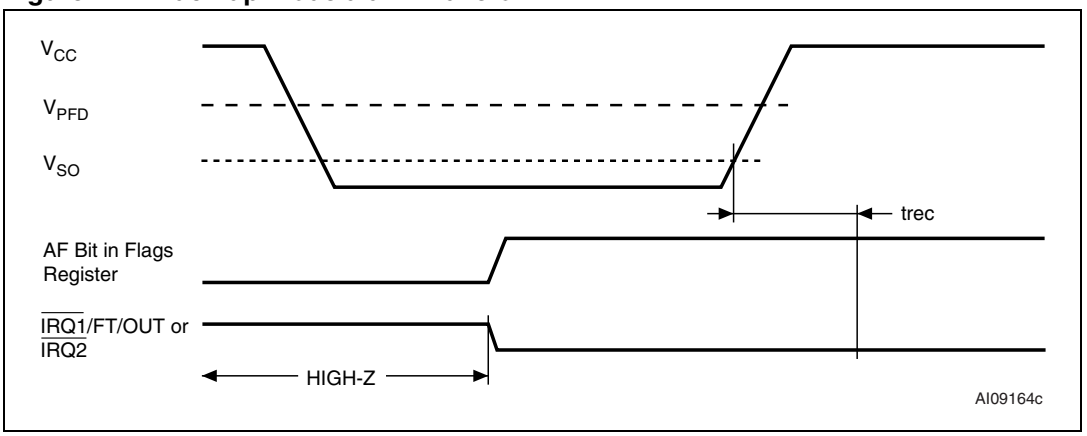


Figure 22. Back-up mode alarm waveform



1. ABE and A1IE bits = 1.

Table 8. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

3.7 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the Watchdog Register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3*1, or 3 seconds). If the processor does not reset the timer within the specified period, the M41T8x sets the WDF (Watchdog Flag) and generates a watchdog interrupt.

The watchdog timer can be reset by having the microprocessor perform a WRITE of the Watchdog Register. The time-out period then starts over.

Should the watchdog timer time-out, a value of 00h needs to be written to the Watchdog Register in order to clear the $\overline{\text{IRQ1}}$/FT/OUT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the Flags Register will reset the Watchdog Flag (bit D7; Register 0Fh).

The watchdog function is automatically disabled upon power-up and the Watchdog Register is cleared. If the watchdog function is set, the frequency test function is activated, and the SQWE bit is '0,' the watchdog function prevails and the frequency test function is denied.

3.8 8-bit (countdown) timer

The Timer Value Register is an 8-bit binary countdown timer. It is enabled and disabled via the Timer Control Register (11h) TE bit. Other timer properties such as the source clock, or interrupt generation are also selected in the Timer Control Register (see *Table 9*). For accurate read back of the countdown value, the I^2C-bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock.

The Timer Control register selects one of four source clock frequencies for the timer (4096, 64, 1, or 1/60Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the Timer Flag (TF) bit. The TF bit can only be cleared by software. When asserted, the timer flag (TF) can also be used to generate an interrupt ($\overline{IRQ1}$/FT/OUT) on the M41T83. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. The Timer Interrupt/Timer Pulse ($\overline{TI}$/TP) bit is used to control this mode selection. When reading the timer, the current countdown value is returned.

Table 9. Timer control register map(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function
0Fh	WDF	AF1	AF2	BL	TF	OF	0	0	Flags
10h	Timer countdown value								Timer value
11h	TE	$\overline{TI}$/TP	TIE	0	0	0	TD1	TD0	Timer control

1. *Bit positions labeled with '0' should always be written with logic '0.'*

3.8.1 Timer interrupt/timer pulse ($\overline{TI}$/TP, M41T83 only)

- $\overline{TI}$/TP = 0
  $\overline{IRQ1}$/FT/OUT is active when TF is logic '1' (subject to the status of the Timer Interrupt Enable bit (TIE).
- $\overline{TI}$/TP = 1
  $\overline{IRQ1}$/FT/OUT pulses are active when TF is logic '1' according to *Table 10* (subject to the status of the TIE bit).

Note: If an Alarm condition, Watchdog time-out, Oscillator Failure, or OUT = 0 causes $\overline{IRQ1}$/FT/OUT to be asserted low, then $\overline{IRQ1}$/FT/OUT will remain asserted even if $\overline{TI}$/TP is set to '1'. When in pulse mode ($\overline{TI}$/TP = 1), clearing the TF bit will not stop the pulses on $\overline{IRQ1}$/FT/OUT. The output pulses will only stop if TE, TIE, or $\overline{TI}$/TP are reset to '0'.

Table 10. Interrupt operation (bit $\overline{TI}$/TP = 1)

Source clock (Hz)	$\overline{IRQ}$[1] periods	
	n[2] = 1	n > 1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

1. TF and $\overline{IRQ1}$/FT/OUT become active simultaneously.
2. n = loaded countdown timer value. The timer is stopped when n = 0.

3.8.2 Timer flag (TF)

At the end of a timer countdown, TF is set to logic '1.' If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading the flag bits. The timer will auto-reload and continue to count down regardless of the state of TF bit (or $\overline{TI}$/TP bit). The TF bit is cleared by reading the Flags Register.

3.8.3 Timer interrupt enable (TIE, M41T83 only)

In Level mode ($\overline{TI}$/TP = 0), when TF is asserted, the interrupt is asserted (if TIE = 1). To clear the interrupt, the TF bit or the TIE bit must be reset.

3.8.4 Timer enable (TE)

- TE = 0

  When the Timer Register (10h) is set to ‘0’, the timer is disabled.
- TE = 1

  The timer is enabled. TE is reset (disabled) on power-down. When re-enabled, the counter will begin from the same value as when it was disabled.

3.8.5 TD1/0

These are the timer source clock frequency selection bits (see *Table 11*). These bits determine the source clock for the countdown timer (see *Table 12*). When not in use, the TD1 and TD0 bits should be set to ‘11’ (1/60Hz) for power saving.

Table 11. Timer source clock frequency selection (244.1µs to 4.25 hrs)

TD1	TD0	Timer source clock frequency (Hz)
0	0	4096 (244.1µs)
0	1	64 (15.6ms)
1	0	1 (1s)
1	1	1/60 (60s)

Table 12. Timer countdown value register bits (addr 11h)(1)

Bit	Symbol	Description
7 - 0	<timer countdown value>	This register holds the loaded countdown value ‘n’.
		Countdown period = n / source clock frequency.

1. *Writing to the timer register will not reset the TF bit or clear the interrupt.*

3.9 Square wave output (M41T83 only)

The M41T83 offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in *Table 13*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the Square Wave Enable bit (SQWE) located in Register 0Ah.

Note: If the SQWE bit is set to '1' and V_{CC} falls below the switchover (V_{SO}) voltage, the square wave output will be disabled.

Table 13. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.10 Battery low warning

The M41T8x automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The Battery Low (BL) bit, bit D4 of Flags Register 0Fh, will be asserted if the battery voltage is found to be less than approximately 2.5V. The BL bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity. Clock data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the battery should be replaced.

The M41T8x only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

3.11 Century bits

These two bits will increment in a binary fashion at the turn of the century, and handle all leap years correctly. See *Table 14* for additional explanation.

Table 14. Century bits examples

CB0	CB1	Leap Year?	Example(1)
0	0	Yes	2000
0	1	No	2100
1	0	No	2200
1	1	No	2300

1. Leap year occurs every four years (for years evenly divisible by four), except for years evenly divisible by 100. The only exceptions are those years evenly divisible by 400 (the year 2000 was a leap year, year 2100 is not).

3.12 Output driver pin

When the OFIE bit, A1IE bit, and Watchdog Register are not set to generate an interrupt, the $\overline{IRQ1}$/FT/OUT pin becomes an output driver that reflects the contents of D7 of register 08h. In other words, when D7 (OUT bit) is a '0,' then the $\overline{IRQ1}$/FT/OUT pin will be driven low.

Note: The $\overline{IRQ1}$/FT/OUT pin is an open drain which requires an external pull-up resistor.

3.13 Oscillator fail detection

If the Oscillator Fail (OF) bit is internally set to a '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time. This bit can be used to judge the validity of the clock and date data. This bit will be set to '1' any time the oscillator stops.

In the event the OF bit is found to be set to '1' at any time other than the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.' This will restart the oscillator. The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a '1' on power-up).

Note: If the OF bit cannot be written to '1' 4 seconds after the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.'

- The voltage present on V_{CC} or battery is insufficient to support oscillation.
- The ST bit is set to '1.'
- External interference of the crystal

For the M41T83, if the Oscillator Fail Interrupt Enable bit (OFIE) is set to a '1,' the $\overline{IRQ1}$/FT/OUT pin will also be activated. The $\overline{IRQ1}$/FT/OUT output is cleared by resetting the OFIE or OF bit to '0' (NOT by reading the Flag Register).

The OF bit will remain set to '1' until written to logic '0.' The oscillator must start and have run for at least 4 seconds before attempting to reset the OF bit to '0.' If the trigger event occurs during a power down condition, this bit will be set correctly.

3.14 Oscillator fail interrupt enable (M41T83 only)

If the Oscillator Fail Interrupt Enable bit (OFIE) is set to a '1,' the $\overline{IRQ1}$/FT/OUT pin will also be activated. The $\overline{IRQ1}$/FT/OUT output is cleared by resetting the OFIE or OF bit to '0' (not by reading the Flags Register).

3.15 Initial power-on defaults

Upon initial application of power to the device, the register bits will initially power-on in the state indicated in *Table 15* and *Table 16*.

Table 15. Initial power-on default values (part 1)

Condition(1)	ST	CB1	CB0	OUT	FT	DCS ACS	Digital calib.	Analog calib.	OFIE (2)	Watchdog (3)	A1IE (2)	SQWE (2)	ABE
Initial Power-up	0	0	0	1	0	0	0	0	0	0	0	1	0
Subsequent Power-up(4) (5)	UC	UC	UC	UC	0	UC	UC	UC	UC	0	UC	UC	UC

1. All other control bits power-up in an undetermined state.
2. M41T83 only.
3. BMB0-BMB4, RB0, RB1.
4. With battery back-up.
5. UC = unchanged.

Table 16. Initial power-up default values (part 2)

Condition[1]	RPT11-15	HT	OF	TE	$\overline{TI}$/TP (2)	TIE (2)	TD1	TD0	RS0	RS1-3	OTP (2)	A2IE (2)	RPT21-25	AL2E
Initial Power-up	0	1	1	0	0	0	1	1	1	0	0	0	0	0
Subsequent Power-up[3] [4]	UC	1	UC	0	UC	UC	UC	UC	UC	UC	UC	UC	UC	UC

1. All other control bits power-up in an undetermined state.
2. M41T83 only.
3. With battery back-up.
4. UC = unchanged.

3.16 OTP bit operation (M41T83 in SOX18 package only)

When the OTP (One Time Programmable) bit is set to a '1,' the value in the internal OTP registers will be transferred to the analog calibration register (12h) and are “Read only.” The OTP value is programmed by the manufacturer, and will contain the calibration value necessary to achieve ±5 ppm at room temperature after two SMT reflows. This clock accuracy can then be guaranteed to drift no more than ±3 ppm the first year, and ±1 ppm for each following year due to crystal aging.

If the OTP bit is set to '0,' the analog calibration register will become a WRITE/READ register and function like standard SRAM memory cells, allowing the user to implement any desired value of analog calibration.

When the user sets the OTP bit, they need to wait for approximately 8ms before the analog registers transfer the value from the OTP to the analog registers due to the OTP Read operation.

4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 17. Absolute maximum ratings

Sym	Parameter		Value(1)	Unit
T_{STG}	Storage temperature (V_{CC} off, Oscillator off)		–55 to 125	°C
V_{CC}	Supply voltage		–0.3 to 7.0	V
T_{SLD}(2)	Lead solder temperature for 10 seconds	QFN16 SO8	260	°C
		SOX18	245	°C
V_{IO}	Input or output voltages		–0.2 to Vcc+0.3	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. Data based on characterization results, not tested in production.
2. Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the dc and ac characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 18. Operating and AC measurement conditions(1)

Parameter	M41T8x
Supply voltage (V_{CC})	2.38V to 5.5V
Ambient operating temperature (T_A)	–40 to 85°C
Load capacitance (C_L)	50pF
Input rise and fall times	≤ 5ns
Input pulse voltages	$0.2V_{CC}$ to $0.8\ V_{CC}$
Input and output timing ref. voltages	$0.3V_{CC}$ to $0.7\ V_{CC}$

1. *Output Hi-Z is defined as the point where data is no longer driven.*

Figure 23. Measurement AC I/O waveform

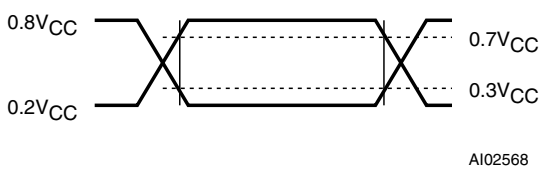


Table 19. Capacitance

Symbol	Parameter(1,2)	Min	Max	Unit
C_{IN}	Input capacitance		7	pF
C_{OUT}(3)	Output capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

1. Effective capacitance measured with power supply at 3.6V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 20. DC characteristics

Sym	Parameter	Test condition(1)		Min	Typ	Max	Unit
V_{CC}	Operating voltage (S)	–40 to 85°C		3.00		5.50	V
	Operating voltage (R)	–40 to 85°C		2.70		5.50	V
	Operating voltage (Z)	–40 to 85°C		2.38		5.50	V
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$				±1	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$				±1	µA
I_{CC1}	Supply current	SCL = 400kHz (No load)	5.5V		125	150	µA
			3.0V		55		µA
			2.5 (Z only)		45		µA
I_{CC2}	Supply current (standby)	SCL = 0Hz; All inputs $\ge V_{CC} - 0.2V$ or $\le V_{SS} + 0.2V$ (SQWE bit = 0)	5.5V		8	10	µA
			3.0V		6.5		µA
V_{IL}	Input low voltage			–0.3		$0.3V_{CC}$	V
V_{IH}	Input high voltage			$0.7V_{CC}$		$V_{CC}+0.3$	V
V_{OL}	Output low voltage	$\overline{RST}$, FT/$\overline{RST}$	V_{CC}/V_{BAT} = 3.0V, I_{OL} = 1.0mA			0.4	V
		SQW, $\overline{IRQ1}$/FT/OUT	V_{CC} = 3.0V, I_{OL} = 1.0mA			0.4	V
		SCL, SDA	V_{CC} = 3.0V, I_{OL} = 3.0mA			0.4	V
V_{OH}	Output high voltage	V_{CC} = 3.0V, I_{OH} = –1.0mA (push-pull)		2.4			V
	Pull-up supply voltage (open drain)	$\overline{IRQ1}$/FT/OUT				5.5	V
V_{BAT}	Battery back-up supply voltage(2)			2.5		5.5	V
V_{CAP}	Capacitor back-up supply voltage			2.0		5.5	V
I_{BAT}	Battery supply current	25°C; V_{CC} = 0V; OSC On; V_{BAT} = 3V; 32KHz Off			365	450	nA

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.38V to 5.5V (except where noted).
2. For non-rechargeable Lithium battery.

Figure 24. I_{CC2} vs. temperature

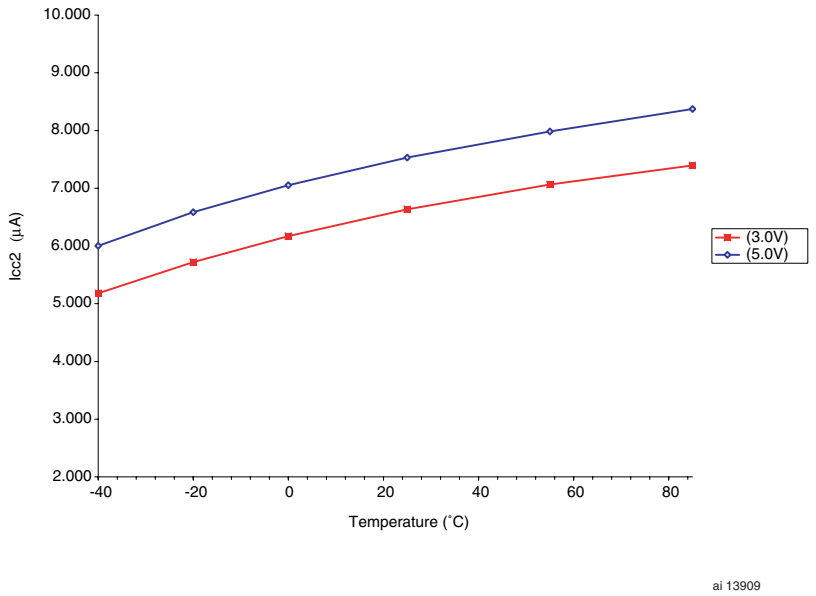


Table 21. Crystal electrical characteristics

Symbol	Parameter[1][2]	Min	Typ	Max	Units
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			65[3]	kΩ
C_L	Load capacitance		12.5		pF

1. Externally supplied if using the QFN16 or SO8 package. STMicroelectronics recommends the Citizen CFS-145 (1.5x5mm) and the KDS DT-38 (3x8mm) for thru-hole, or the KDS DMX-26S (3.2x8mm) or Micro Crystal MS3V-T1R (1.5x5mm) for surface-mount, tuning fork-type quartz crystals. For contact information, see *Section 8: References on page 56*.
2. Load capacitors are integrated within the M41T8x. Circuit board layout considerations for the 32.768kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. Guaranteed by design.

Table 22. Oscillator characteristics

Symbol	Parameter[1][2]	Conditions	Min	Typ	Max	Units
V_{STA}	Oscillator start voltage	≤ 4s	2.0			V
t_{STA}	Oscillator start time	$V_{CC} = V_{SO}$			1	s
C_{XI}, C_{XO}[1]	Capacitor input, capacitor output			25		pF
	IC-to-IC frequency variation[2][3]		–10		+10	ppm

1. With default analog calibration value (= 0).
2. Reference value.
3. $T_A = 25°C$, $V_{CC} = 5.0V$.

Figure 25. Power down/up mode AC waveforms

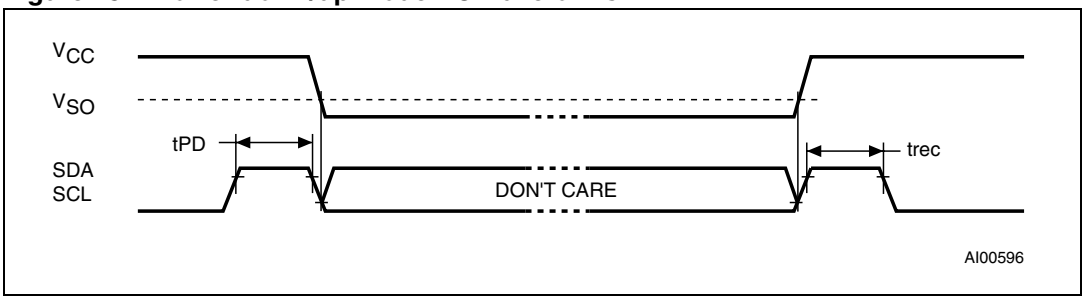


Table 23. Power down/up trip points DC characteristics

Sym	Parameter(1) (2) (1,2)		Min	Typ	Max	Unit
V_{RST}	Reset threshold voltage	S	2.85	2.93	3.0	V
		R	2.55	2.63	2.7	V
		Z	2.25	2.32	2.38	V
V_{SO}	Battery back-up switchover			V_{RST}		V
	Hysteresis			25		mV
t_{rec}	Reset Pulse width (V_{CC} Rising)		140		280	ms
	V_{CC} to Reset Delay, V_{CC} = (V_{RST} + 100mV), falling to (V_{RST} – 100mV; for V_{CC} slew rate of 10mV/µs			2.5		µs

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.38 to 5.5V (except where noted).

Figure 26. Bus timing requirement sequence

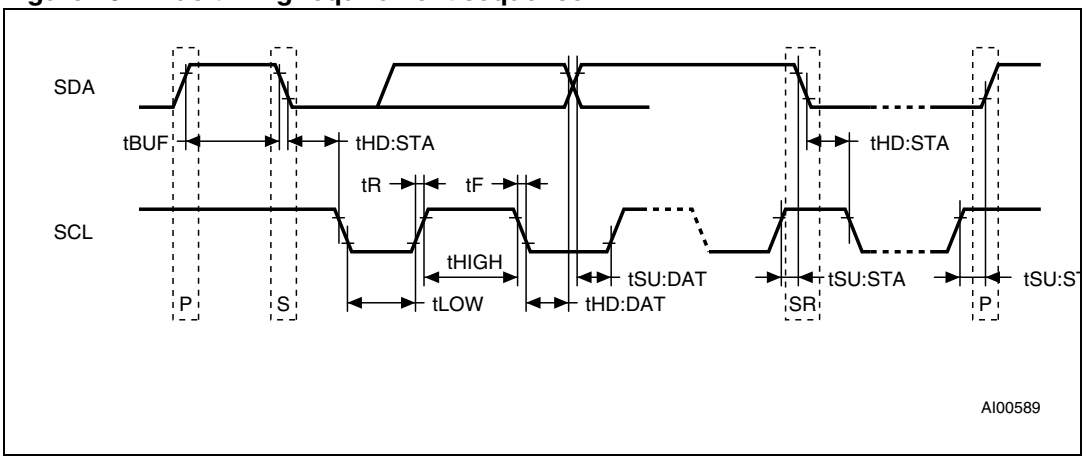


Table 24. AC characteristics

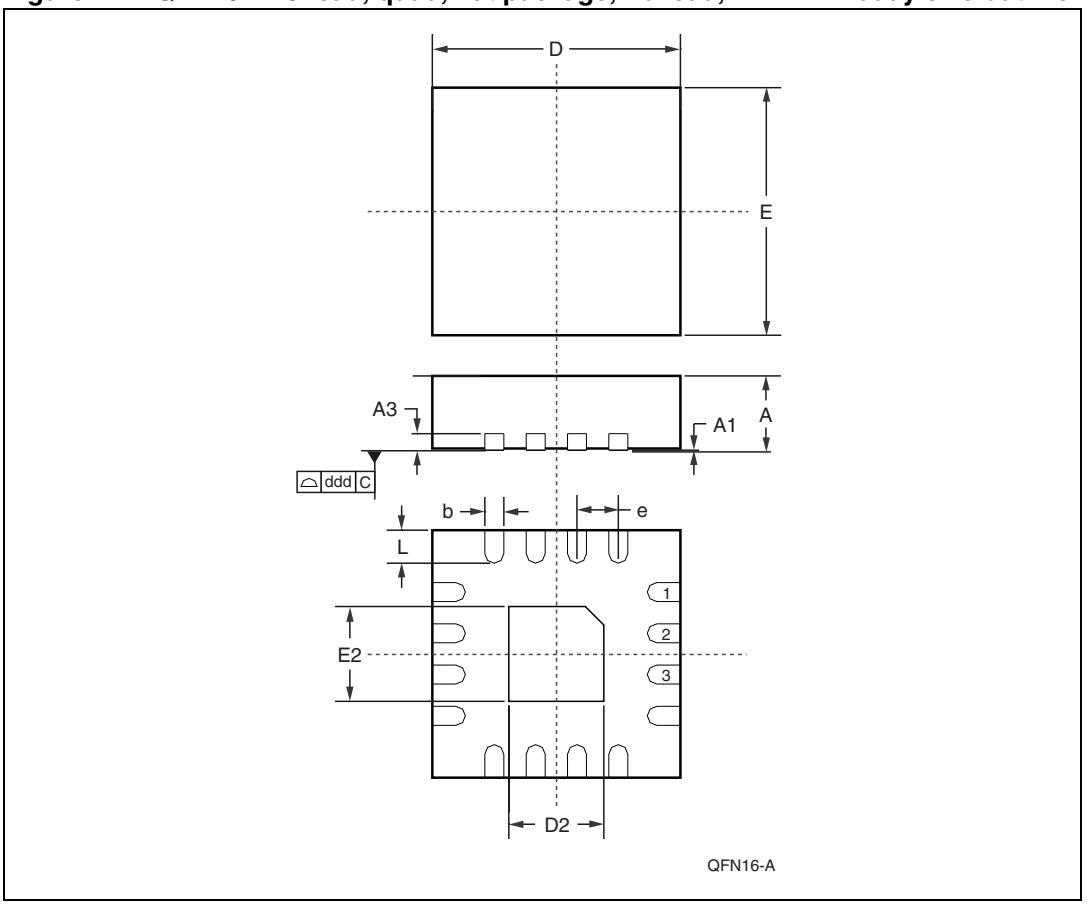
Sym	Parameter[1]	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	0		400	Hz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$[2]	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:STO}$	STOP condition setup time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.38 to 5.5V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of SCL.

6 Package mechanical information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 27. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm body size outline

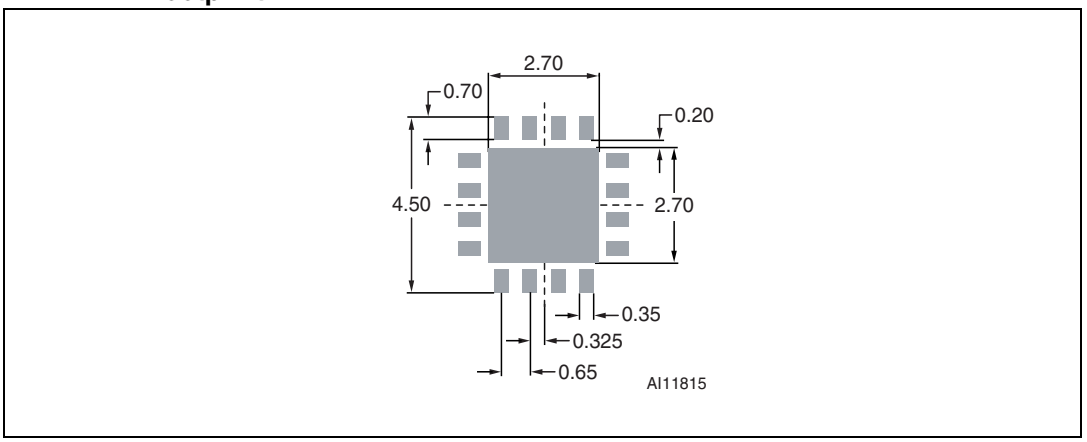


1. Drawing is not to scale.

Table 25. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm mech. data

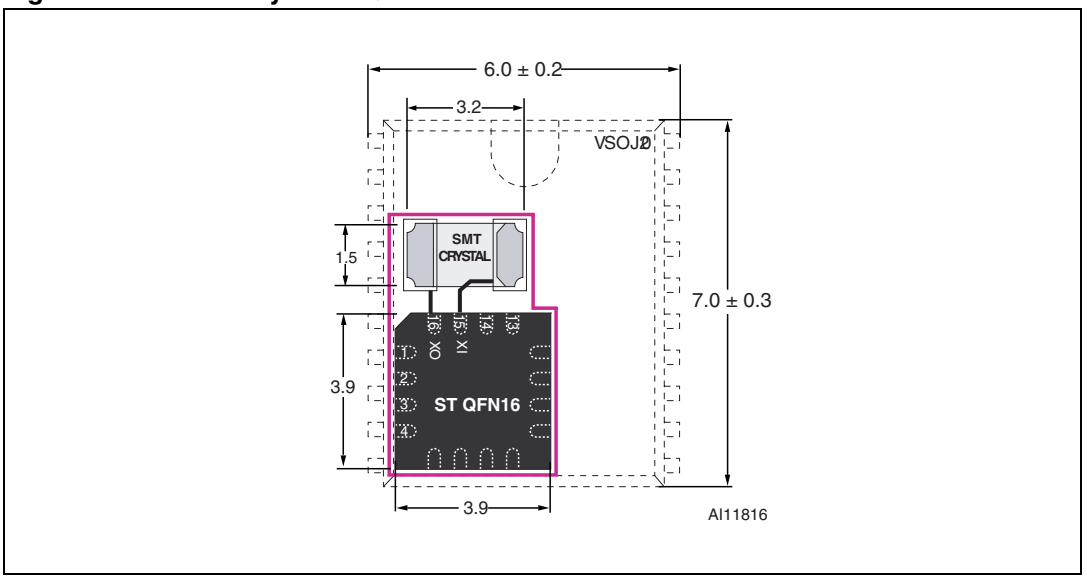
Sym	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.90	0.80	1.00	0.035	0.031	0.039
A1	0.02	0.00	0.05	0.001	0.000	0.002
A3	0.20	–	–	0.008	–	–
b	0.30	0.25	0.35	0.012	0.010	0.014
D	4.00	3.90	4.10	0.157	0.154	0.161
D2	–	2.50	2.80	–	0.098	0.110
E	4.00	3.90	4.10	0.157	0.154	0.161
E2	–	2.50	2.80	–	0.098	0.110
e	0.65	–	–	0.026	–	–
L	0.40	0.30	0.50	0.016	0.012	0.020
ddd	–	0.08	–	–	0.003	–

Figure 28. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm, recommended footprint



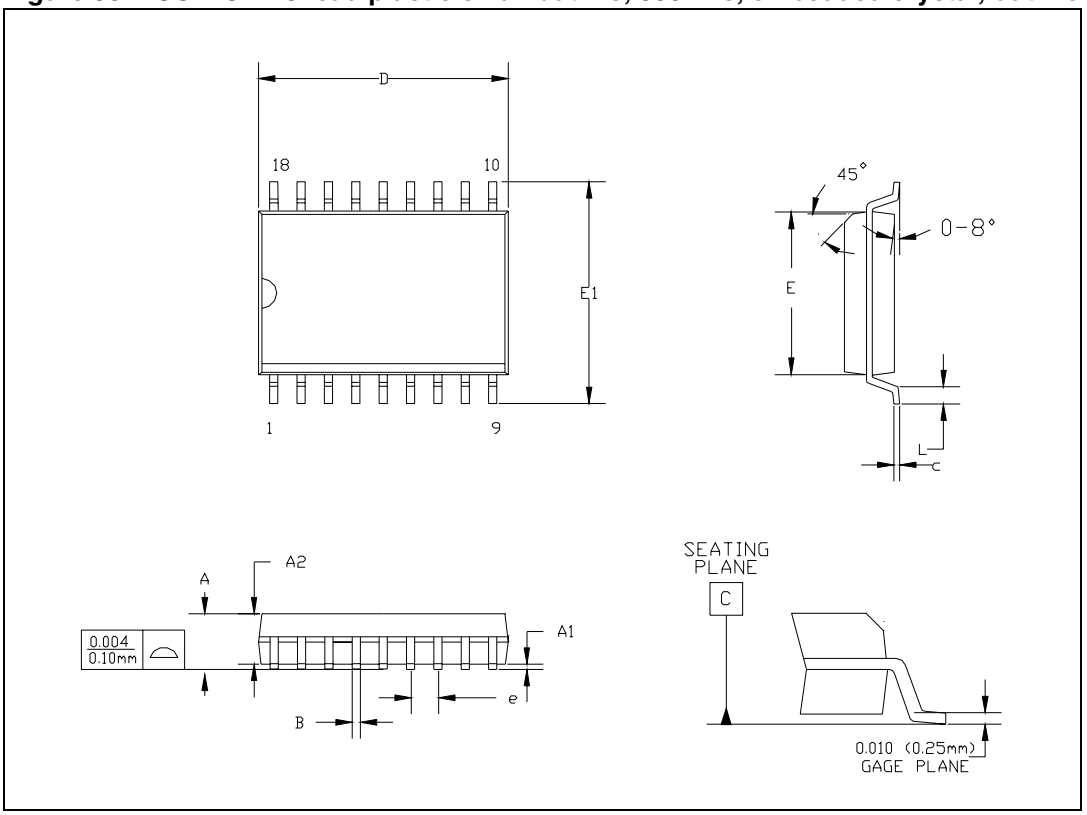
1. Dimensions are shown in millimeters (mm).

Figure 29. 32KHz crystal + QFN16 vs. VSOJ20 mechanical data



1. Dimensions shown are in millimeters (mm).

Figure 30. SOX18 – 18-lead plastic small outline, 300mils, embedded crystal, outline

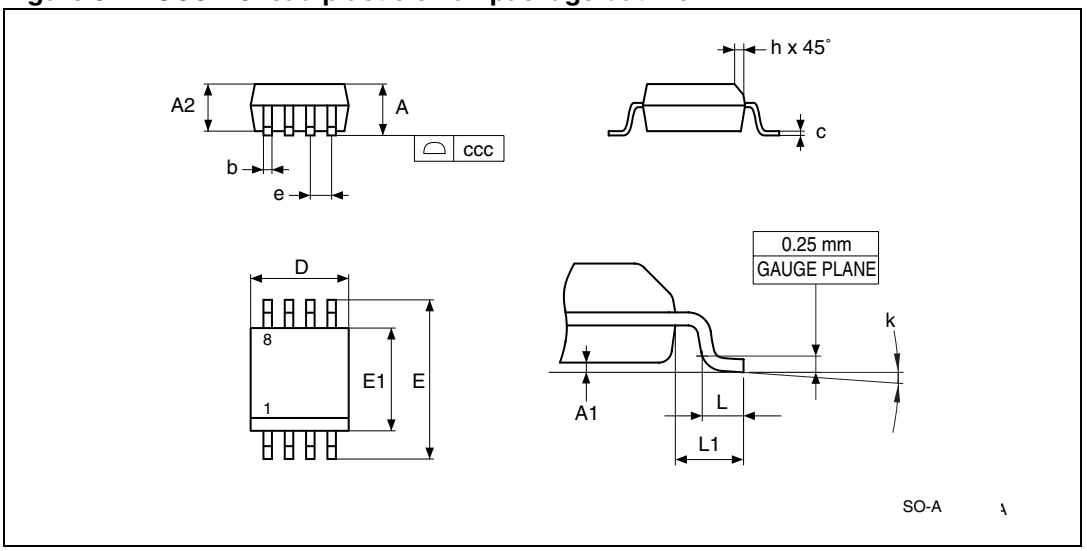


1. Drawing is not to scale.

Table 26. SOX18 – 18-lead plastic small outline, 300mils, embedded crystal, package mech.

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	2.57	2.44	2.69	0.101	0.096	0.106
A1	0.23	0.15	0.31	0.009	0.006	0.012
A2	2.34	2.29	2.39	0.092	0.090	0.094
B	0.46	0.41	0.51	0.018	0.016	0.020
c	0.25	0.20	0.31	0.010	0.008	0.012
D	11.61	11.56	11.66	0.457	0.455	0.459
E	7.62	7.57	7.67	0.300	0.298	0.302
E1	10.34	10.16	10.52	0.407	0.400	0.414
e	1.27	–	–	0.050	–	–
L	0.66	0.51	0.81	0.026	0.020	0.032

Figure 31. SO8 – 8-lead plastic small package outline



1. Drawing is not to scale.

Table 27. SO8 – 8-lead plastic small outline (150 mils body width), package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	-	-	0.050	-	-
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	0.127		0.016	0.050
L1	1.04			0.041		

7 Part numbering

Table 28. Ordering information

Example: M41T 83 S QA 6 E

Device family

M41T

Device type

82 (SO8 package only)

83

Operating voltage

S = V_{CC} = 3.00 to 5.5V

R = V_{CC} = 2.70 to 5.5V

Z = V_{CC} = 2.38 to 5.5V

Package

QA = QFN16 (4mm x 4mm)

M(1) = SO8

MY(2)= SOX18

Temperature range

6 = –40°C to 85°C

Shipping method

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

1. M41T82 only.
2. The SOX18 package includes an embedded 32,768Hz crystal.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

8 References

Below is a listing of the crystal component suppliers mentioned in this document.

- KDS can be contacted at **kouhou@kdsj.co.jp** or **http://www.kdsj.co.jp**.
- Citizen can be contacted at **csd@citizen-america.com** or **http://www.citizencrystal.com**.
- Micro Crystal can be contacted at **sales@microcrystal.ch** or **http://www.microcrystal.com**.

9 Revision history

Table 29. Document revision history

Date	Revision	Changes
27-Jul-2006	1	First edition
17-Oct-2006	2	Updated package mechanical data in *Figure 31: SO8 – 8-lead plastic small package outline* and *Table 27: SO8 – 8-lead plastic small outline (150 mils body width), package mech. data*; small text changes for entire document, amended footnotes in *Table 1*, *Table 14* and *Figure 5*.
19-Dec-2006	3	Document status upgraded to full datasheet; added footnote to diagram in *Features*; amended footnotes in *Figure 2* and updated footnotes in *Table 28*; updated 'typical data' for I_{CC1} and I_{CC2} in *Table 20*; Updated package mechanical data for the QFN16 and SOX18 in *Section 6*; changed kHz to KHz through document; made small text changes throughout document.
08-Mar-2007	4	Updated cover page (features and amended footnote concerning availability), *Figure 18: Clock accuracy vs. on-chip load capacitance*, and ordering information (*Table 28*).
08-May-2007	5	Updated title of product (added I^2C bus) on cover page; updated *Section 3.16*, *Section 3.4.1*, *Table 17*, *20*, *28*, *Figure 29*; added *Figure 24*; added Micro Crystal information (*Table 21*).
12-Nov-2007	6	Updated Features on cover page; minor formatting changes; modified footnote 1 in *Table 21*; added *Section 8: References*.

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