MITSUBISHI MICROCOMPUTERS

M50747-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50747-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50747-XXXSP and the M50747-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

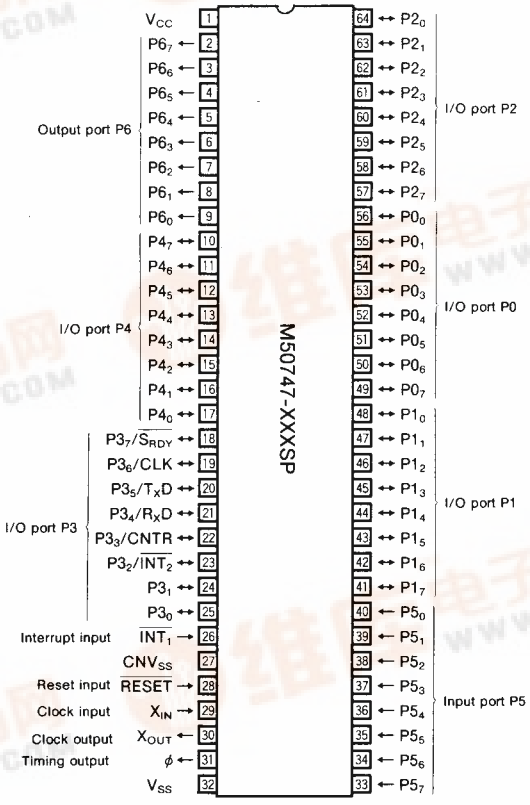
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 8192 bytes
  RAM ..... 256 bytes
- Instruction execution time
  ..... 1 μs (minimum instructions at 8MHz frequency)
- Single power supply f(X_{IN})=8MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 128 levels (max.)
- Interrupt ..... 7 types, 5 vecters
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 8
- Serial I/O (Clock synchronized or UART) 1

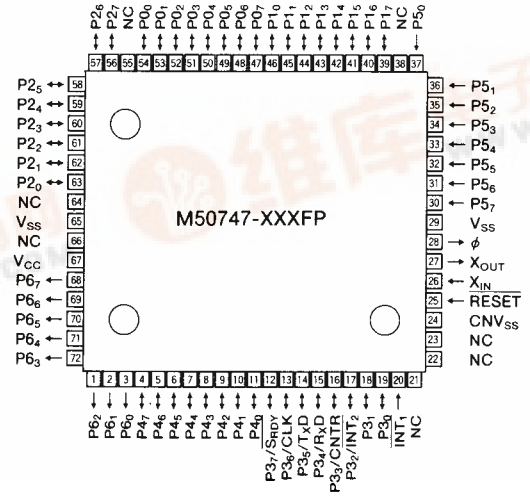
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



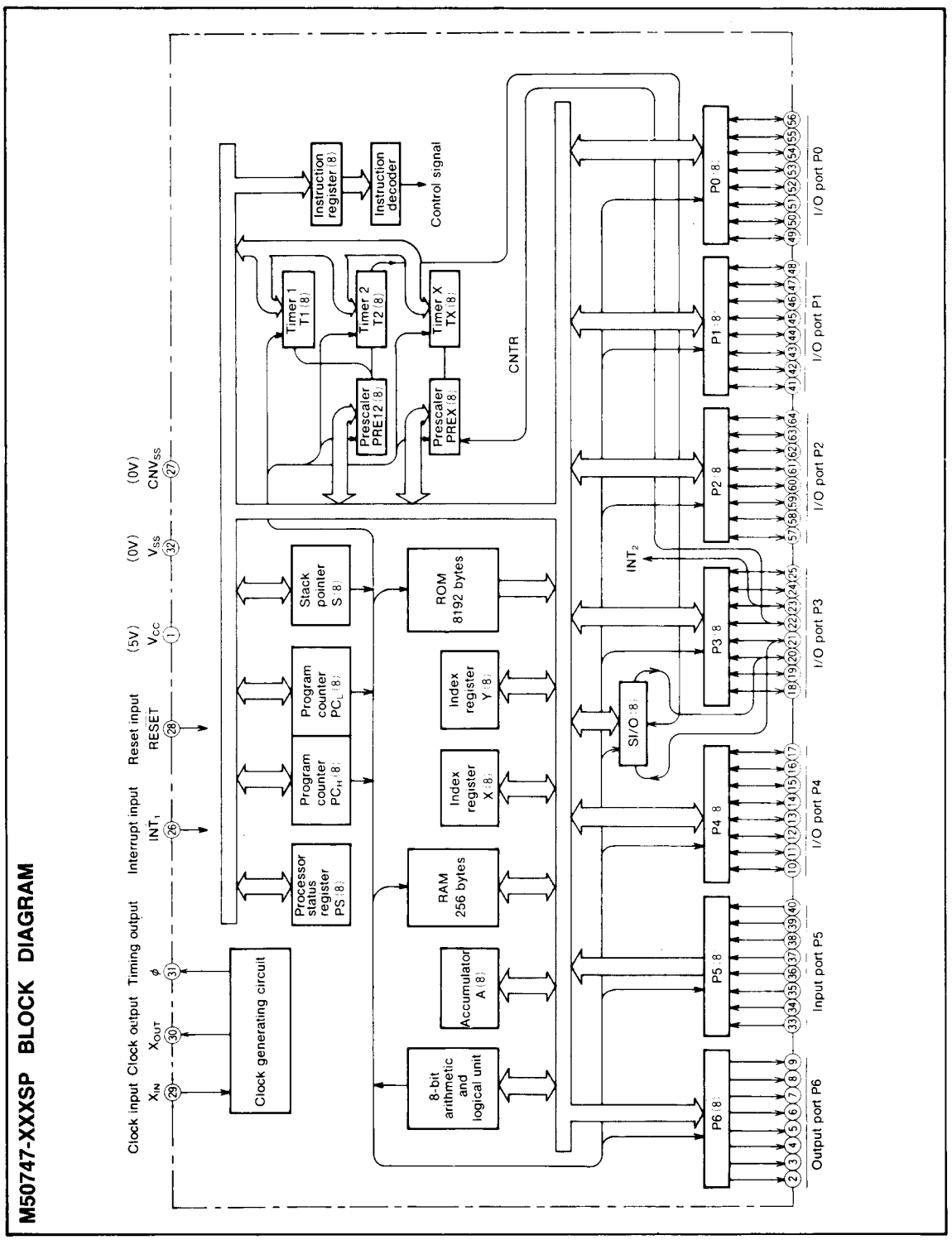
Outline 64P4B



Outline 72P6

NC : No connection

M50747-XXXSP BLOCK DIAGRAM



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M50747-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz of frequency)
Clock frequency			8MHz
Memory size	ROM		8192bytes
	RAM		256bytes
Input/Output port	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (Part of P3 are in common with Input/output of serial I/O, timer I/O and $\overline{INT_2}$ interrupt input)
	P5	Input	8-bit×1
	P6	Output	8-bit×1
Serial I/O			8-bit or 9-bit×1
Timers			8-bit prescaler×2+8-bit timer×3 (8-bit timer×2 when serial I/O is used)
Subroutine nesting			128 levels (max.)
Interrupts			Two external interrupts (1 of external interrupt is in common with port $P3_2$) Three timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Built-in (Ceramic or Quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at high-speed operation		30mW (at 8MHz frenquency)
Input/Output characteristics	Input/output voltage		5V
	Output current		5mA (Ports P3, P4, P6)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M50747-XXXSP		64-pin shrink plastic molded DIP
	M50747-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an I/O pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_6$, $P3_5$, and $P3_4$ work as CLK, T_XD pins, respectively. When clock synchronous serial I/O is used, $P3_7$ works as $\overline{S_{RDY}}$. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest order interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$P6_0$~$P6_7$	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is CMOS output.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50747-XXXSP is shown in Figure 1. Addresses $E000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 8192 bytes.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $013F_{16}$ are assigned to the built-in RAM and respectively consist of 192 bytes and 64 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

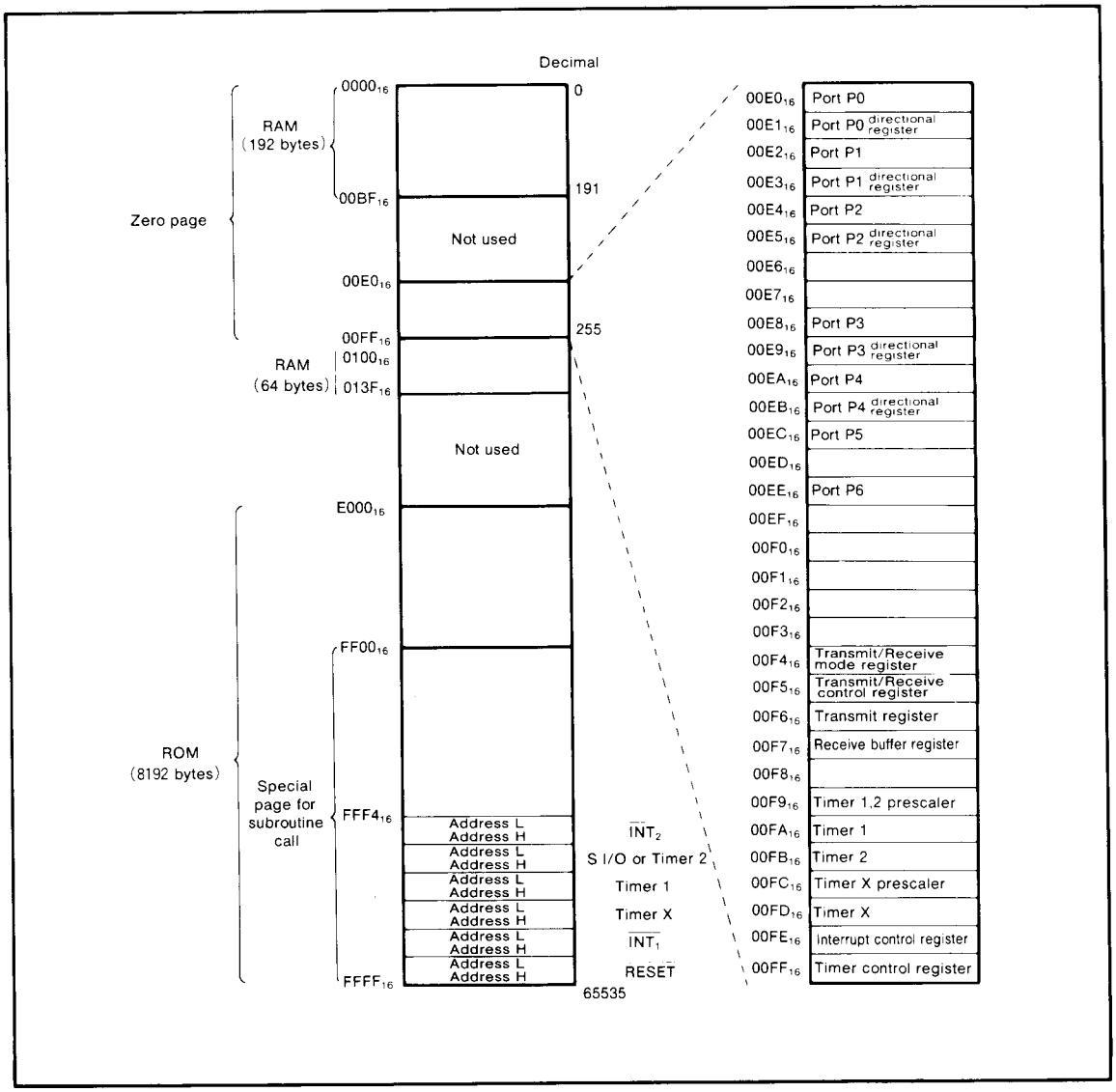


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

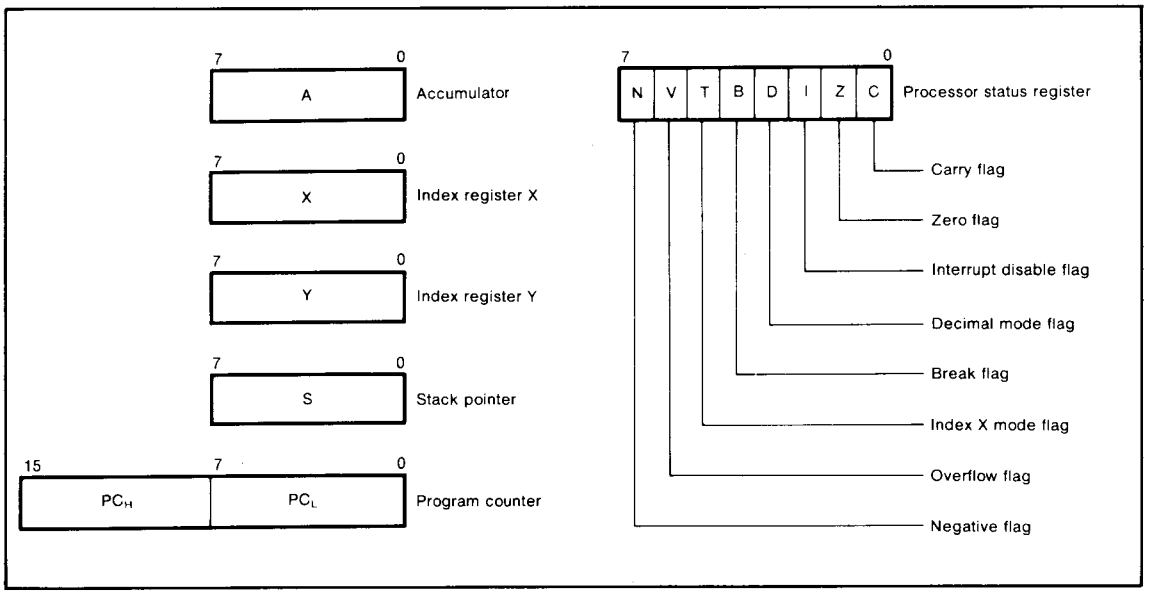


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{INT_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{INT_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50747-XXXSP can be interrupted from seven souces; $\overline{INT_1}$, timer X, timer 1, timer 2/serial I/O, or $\overline{INT_2}$/BRK instruction.

However, the $\overline{INT_2}$ pin is used with port $P3_2$ and the corresponding directional register bit should be set to "0" when $P3_2$ is used as an interrupt input pin.

The value of bit 2 and bit 3 of the transmit/receive mode register (address $00F4_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When these bits are "00" the interrupt is from timer 2, otherwise the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure

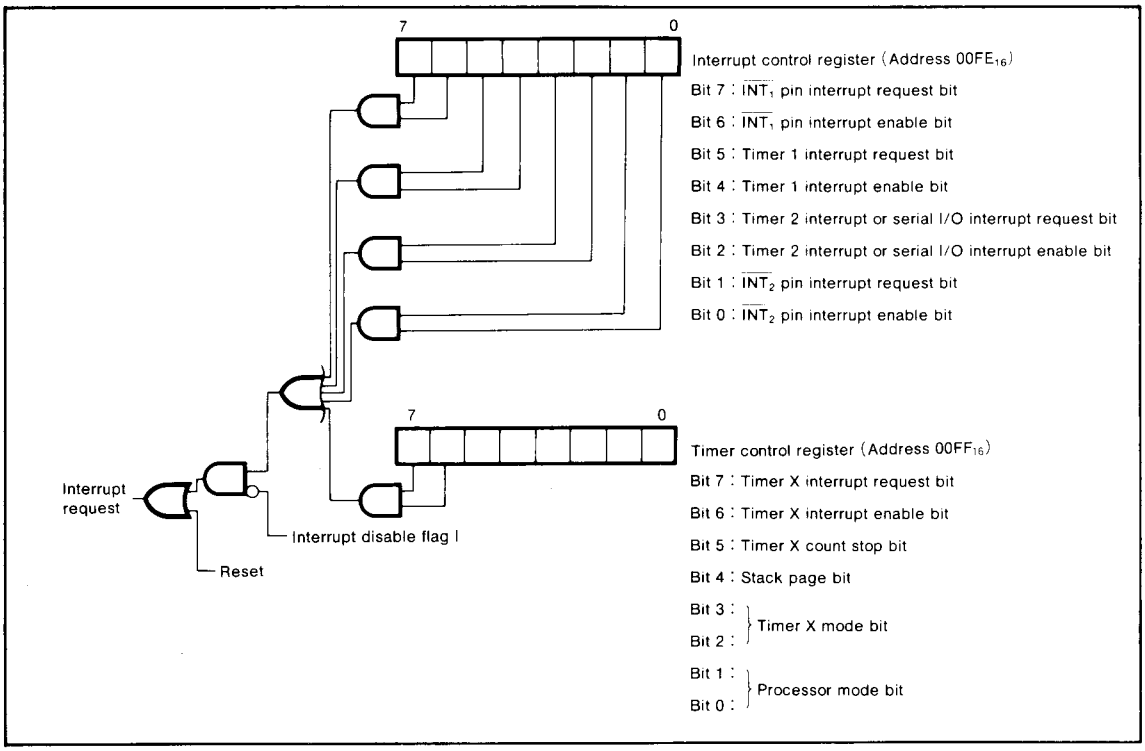


Fig.3 Interrupt control

3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

The interrupt from serial I/O is used switching with that from timer 2. This interrupt is slightly different from the others. When serial I/O is selected, the interrupt becomes automatically the interrupt from serial I/O. Because the interrupt request bit of timer 2 is edge-senced and not level-senced, when interrupts are generated from both transmit and receive sides as illustrated in Figure 5, transmit interrupts will not be accepted by only taking OR of receive interrupt flag RI and transmit flag TI. Even if RI is cleared to "0" by executing receive interrupt processing and is returned to the main routine, TI is "1" and its level will not be changed. In order to accept interrupts in the above state, when RI or TI is cleared from "1" to "0" the pulse is generated automatically and lets the request bit go from "H" to "L". By doing so, the level will be changed. The interrupt processing routine of serial I/O is shown in Figure 4.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

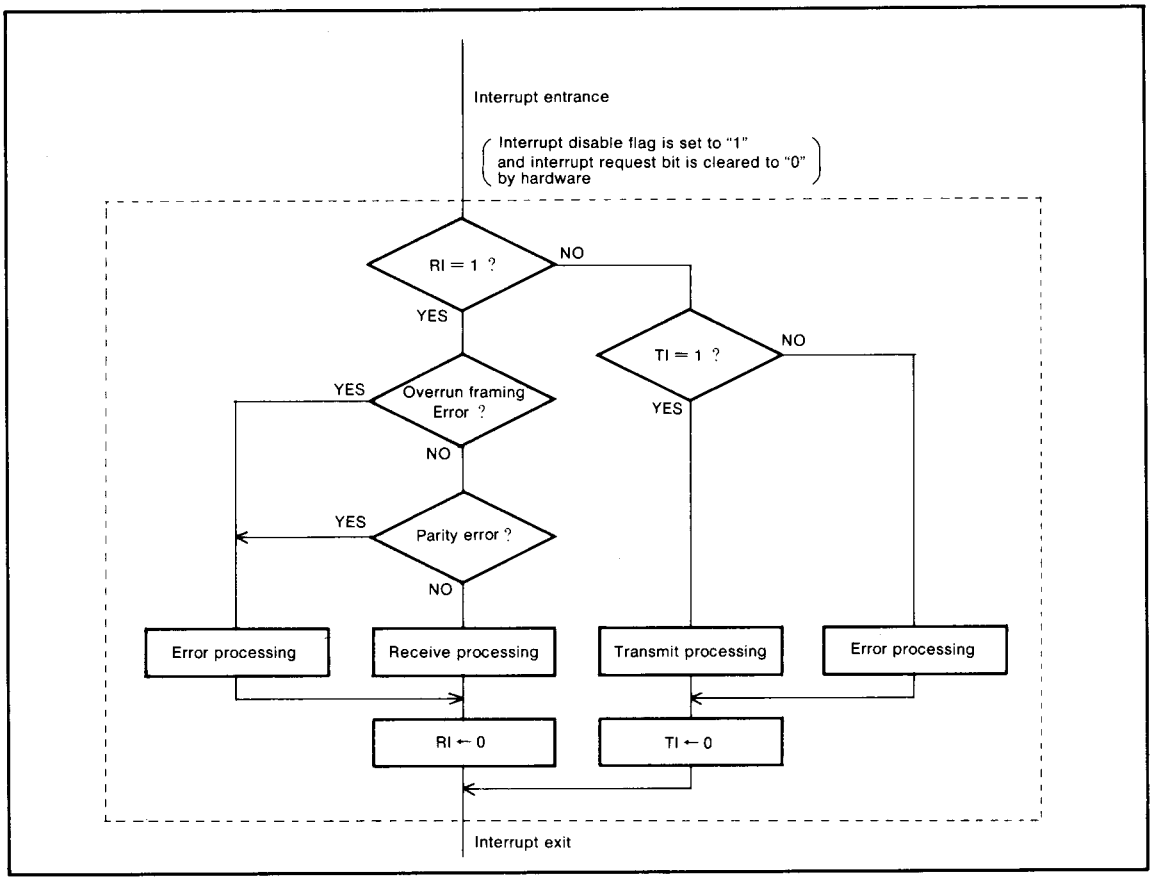


Fig.4 Interrupt processing routine

TIMER

The M50747-XXXSP has three timers; timer X, timer 1, and timer 2. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in.

A block diagram of timer X, timer 1, timer 2 and serial I/O is shown in Figure 5.

The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section).

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

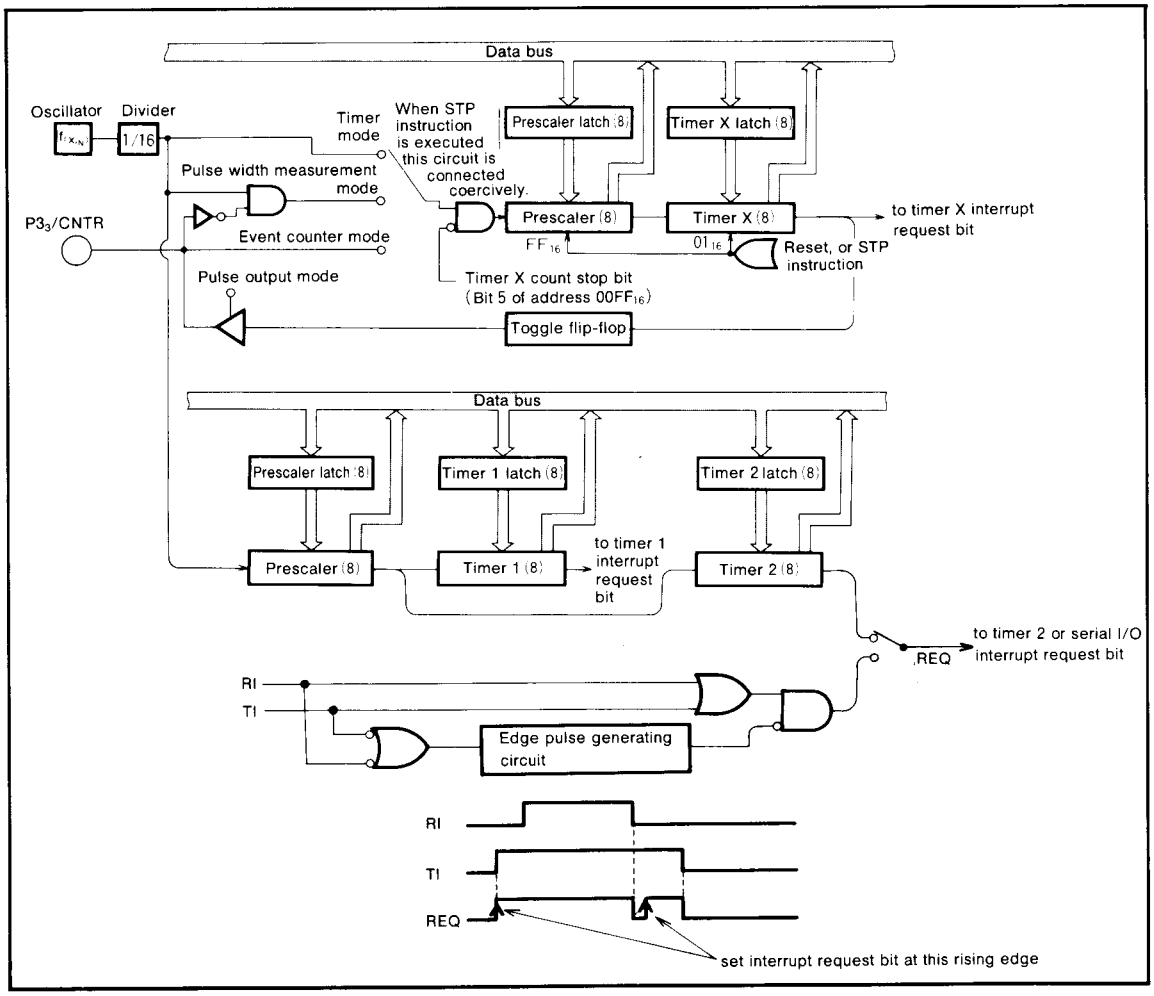


Fig.5 Interrupt block diagram of timer X, timer 1, timer 2 and serial I/O

(3) Event counter mode (10)

This mode operates in the same manner as the timer mode except the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode (11)

This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 6.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

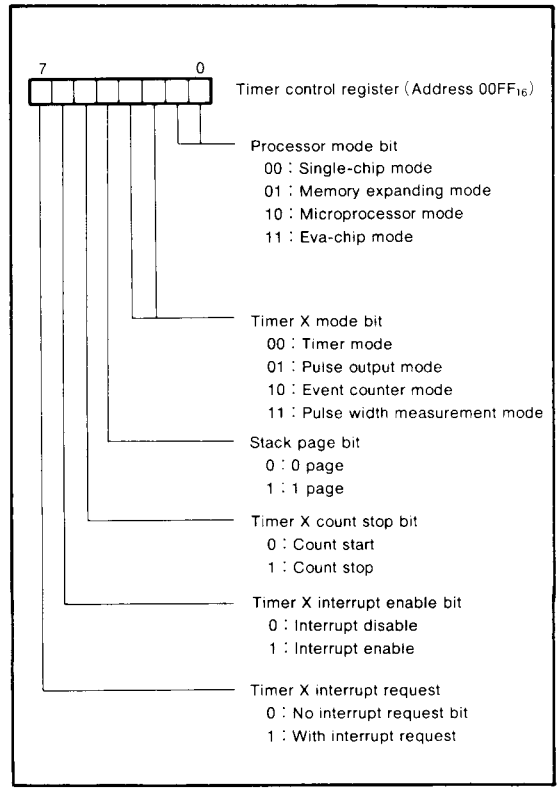


Fig.6 Structure of timer control register

SERIAL I/O

Figure 7 is a block diagram of the serial I/O. Two types exist in serial data transfer: the clock synchronous type in which data is transferred, synchronized with the clock, and the asynchronous type (UART) in which data is transferred using the start and stop bits. The user can choose either type. There are two asynchronous type modes: 8-bit data transfer and 9-bit data transfer. The receive ready signal ($\overline{S_{RDY}}$), clock I/O (CLK), data I/O (T_XD and R_XD) pins share the same pins as $P3_7$, $P3_6$, $P3_5$, $P3_4$.

Figure 8 gives the bit configuration for the transmisson/receive mode register and transmisson/receive control register. The transmit/receive mode register ($00F4_{16}$) is a 5-bit register. Bits 1 and 0 are used to define the clock source for synchronization. When the contents of bits 1 and 0 are [00] or [01], respectively, the external clock is used. The external clock is input to pin $P3_6$. Use an external clock with a 50% duty cycle and a frequency lower than 500kHz.

When the contents of bits 1 and 0 are [10] or [11], respectively, the built-in clock is used.

When the contents are [10], the overflow signal from timer 2 is used for the clock source. Therefore, by changing the division rate, the data transfer speed can be controlled.

When the contents are [11], the frequency obtained by dividing the oscillation frequency by 16 is used as the clock source.

Bits 2 and 3 are used to define which pins on port P3 are to be used as serial I/O, and which type of serial I/O to used.

When the contents are [00], respectively, port P3 is used as a normal parallel port.

When the contents are [01], respectively, the clock synchronous type serial I/O is used.

$P3_7/\overline{S_{RDY}}$ on port P3 is used as the receive ready signal pin. $P3_6$/CLK is used as the input or output pin. When an external clock is to be used, the signal from the clock is connected to this pin. When the built-in clock is to be used, the signal from the clock is output to this pin. $P3_5/T_XD$ is used as the serial data output pin. $P3_4/R_XD$ is used as the serial data input pin. When this pin is not used as the serial data input pin, it can be used as the normal input/output pin. When this pin is used as the serial data input pin, set the directional register to the input mode.

When the contents are [10], this serial I/O is used as an 8-bit asynchronous serial I/O. If the external clock source is selected together with the bit contents [10], the clock signal is input to $P3_6$/CLK on port P3. The data transfer speed is 1/16 of the clock frequency. When the built-in clock is used, this can be used as the normal input/output pin. $P3_5/T_XD$ is used as the serial data output pin. $P3_4/R_XD$ is used as the serial data input pin. When this is not used as the serial data input pin, it can be used as a normal input/output pin. When this pin is used as a serial data input pin, set the directional register to the input mode. When the contents are [11], a 9-bit asynchronous serial I/O is selected. The functions on port P3 are the same as in the 8-bit case.

Bit 4 is used to select the sleep mode. The sleep mode is valid only for asynchronous transmission. See the section on the sleep mode for further explanation. When the contents are "0", the sleep mode is disabled. When the contents are "1", the sleep mode is enabled.

The transmission/receive control register is an 8-bit register. Bits 1, 3, 4, 5 and 7 are for read only. Each bit is explained as follows.

Transmit enable bit (TE)

When this bit is set to "0", the send clock is pulled up to "H", the transmit completion bit (TI) is cleared to "0", transmission is terminated, and the serial I/O is initialized. When this bit is set to "1", transmission starts. Therefore, send data must be written into the transmission register prior to setting it to "1". When the transmission is completed, the serial I/O stops and the transmission clock is pulled up to "H" automatically.

Once the above operation has been peformed, transmission starts by writing data into the transmission register.

Transmit completion bit (TI)

This bit is cleared to "0" when the transmit enable bit (TE) is set to "0", or when data is written into the transmission register. When transmission is completed, this bit is set to "1". An OR operation is performed between the transmit completion bit (TI) and the receive completion bit (RI), and the result is input into the interrupt request bit (bit 3 of address $00FE_{16}$). See the section on interrupts for more information.

Receive enable bit (RE)

When this bit is cleared to "0", the receive completion bit (RI), the overrun framing error (OFR), and the receive parity error bit (PER) are cleared and initialized. When this bit is set to "1", the I/O enters the receive enable status. For the clock synchronous type serial I/O, data is fetched from the $P3_4/R_XD$ pin and the contents of the receive register are shifted by 1 bit every time the receive clock changes from "L" to "H". For the asynchronous type I/O, receiving starts when a start bit is forwarded to $P3_4/R_XD$.

Receive completion bit (RI)

This bit is cleared to "0" when the receive enable bit is set to "0", or when writing is performed to the receive buffer register. If the receive buffer is written to, no data is written in the register and the previous data is preserved. When a set of data arrives in the receive buffer, and the receive completion bit (RI) is "0", data is transferred to the receive buffer register. With this operation, receiving terminates and the receive completion bit (RI) is set to "1". An OR operation is performed between the receive completion bit (RI), the transmit completion bit (TI), and the result is input to the interrupt request bit (bit 3 at address $00FE_{16}$). For more information on the interrupts, see the corresponding section.

Overrun framing error bit (OFR)

When the receive enable bit (RE) is set to "0" or when writing is performed to the receive buffer register, this bit is cleared to "0". If an overrun or framing error occurs, this bit is set to "1". An overrun error occurs when the receive completion bit (RI) remains set to "1" and the next data is transferred from the receive register to the receive buffer register. A framing error occurs when data arrives in the receive register, (which should be transferred to the receive buffer register), and no stop bit exists. This bit is valid only for asynchronous transmission.

Receive parity error bit (PER)

When the number of "1"s is in the received data register is odd, this bit is set to "1". This bit is cleared to "0" when the receive enable bit (RE) is set to "0" or when writing is performed to the receive buffer register.

Receive data bit (T8)

For 9-bit asynchronous transmission, this bit is transmitted as bit 8 data.

Receive data bit 8 (R8)

For 9-bit asynchronous transmission, this bit is used to receive the bit 8 data.

The operation of each transmission method is described below.

CLOCK SYNCHRONOUS TYPE SERIAL TRANSMISSION

Receiving starts when the receive enable bit (RE) is set to "1". Every time the receive clock changes from "L" to "H", data is fetched from $P3_4/R_XD$ pin and, simultaneously, the contents of the receive register are shifted by 1 bit. Data transmission starts from the least significant bit. When 8 bits of data are received, the receive completion bit (RI) is set to "1". When RI changes from "0" to "1", the interrupt request bit is set to "1". When the internal clock is used, the receive clock stops in the "H" condition. When the external clock is used, the clock does not stop. In this case, control this clock using external devices. Once the receive enable bit (RE) is set to "1", writing to the receive buffer register clears the receive completion bit (RI) and receiving restarts. Set a "0" in the transmission enable bit during receiving.

Setting "1" in the transmission enable bit (TE) starts the transmission. Accordingly, write data in the transmission register before setting TE to "1". Every time the transmission clock changes from "H" to "L", data is output from the $P3_5/T_XD$ pin. Data transmission starts from the least significant bit. The transmission completion bit (TI) is set to "1" for each 8 bits of data transmitted. When TI changes from "0" to "1", the interrupt request bit is set to "1". When the internal clock is used, the clock stops in the "H" position after transmitting 8 bits of data. When an external clock is used, the clock does not stop. In this case, control this clock using external devices. Once the transmission enable bit is set to "1", writing data to the transmission register clears the transmission completion bit to "0" and starts the transmission. Set a "0" in the receive enable bit during transmission. When the external clock is used, the transmission speed is the same as that of the clock. When the internal clock is used, the clock frequency obtained by dividing the clock source by 16 is used for the transmission speed. Figure 9 gives the transmission timing. This figure also gives the timings for 8-bit and 9-bit asynchronous transmission, which is explained below.

8-BIT ASYNCHRONOUS TRANSMISSION

Setting the receive enable bit (RE) to "1" brings the I/O into the receiving ready status. Transmission starts when the first data that changes the level from "H" to "L" is received, and data is forwarded to the receive register. When 8 bits of data are received and the receive completion bit (RI) is set to "1", the 8-bits of data are transferred to the receive buffer register, and RI is set to "1". See the section on the interrupts for more information. If RI is set to "1", no transfer is performed. The overrun framing error bit (OFR) is set to "1" when RI is set to "1" and the next data is received. When the stop bit is set to "0", the OFR bit is set to "1" regardless of the RI bit status. No other condition will change the contents of this bit. When the number of "1"s in the received data register is odd, the receive error bit (PER) is set to "1". No other condition will change the contents of this bit. Bits RI, OFR, and PER are cleared to "0" when writing is performed to the receive buffer register. When 8-bits of data are received, receiving automatically halts and the start bit of the next data is ready.

When the transmission enable bit (TE) is set to "1" (after writing data to the transmit register), transmission starts. First, the start bit "0" is sent, and data is transferred starting from the least significant bit. When the stop bit "1" is sent, the transmission completion bit (TI) is set to "1" and the transmission terminates. For more information on the interrupt, see the corresponding section. After the above operation has been performed, the transmission completion bit (TI) is cleared to "0" and transmission restarts after writing to the transmit register is performed.

9-BIT ASYNCHRONOUS TRANSMISSION

Operation for 9-bit asynchronous transmission is same as 8-bit asynchronous transmission except that the transmission data consists of 9 bits. When receiving data, bit 8 of the received data is input to bit 7 on address $00F5_{16}$ (transmit/receive control register). When transmitting data, the contents of bit 6 in the transmit/receive control register is output as bit 8 of the send data.

SLEEP MODE

For 9-bit asynchronous transmission, when bit 4 (SM_4) of the transmit/receive mode register ($00F4_{16}$) is set to "1" and bit 8 of the receive data is "0", the received data is ignored. When bit 8 of the receive data is set to "1", data is received. When the contents of SM_4 is "0", data is received, regardless of the contents of bit 8 of the received data. For 8-bit asynchronous transmission, the stop bit works as bit 8 of the received data. The sleep mode is used when several local microcomputers are to be connected to a single host computer through the serial I/O.

First, the host computer sets T8 to "1" and sends data. The data contains the address of the local microcomputer to be accessed. All the local microcomputers receive the same data. Each local microcomputer checks the data (address), and if the address is that assigned to the local microcomputer, bit 4 of the transmit/receive mode register is set to "0". Bit 4 of the registers of all the other local microcomputers is set to "1". Then, the host computer starts transmission by setting T8 to "0". The local microcomputer whose SM_4 is "0" receives the transmitted data, while the other local microcomputers continue program execution without being interrupted by serial I/O. This is because SM_4 on these computers set to "1". Thus, the host computer can communicate with a specific microcomputer.

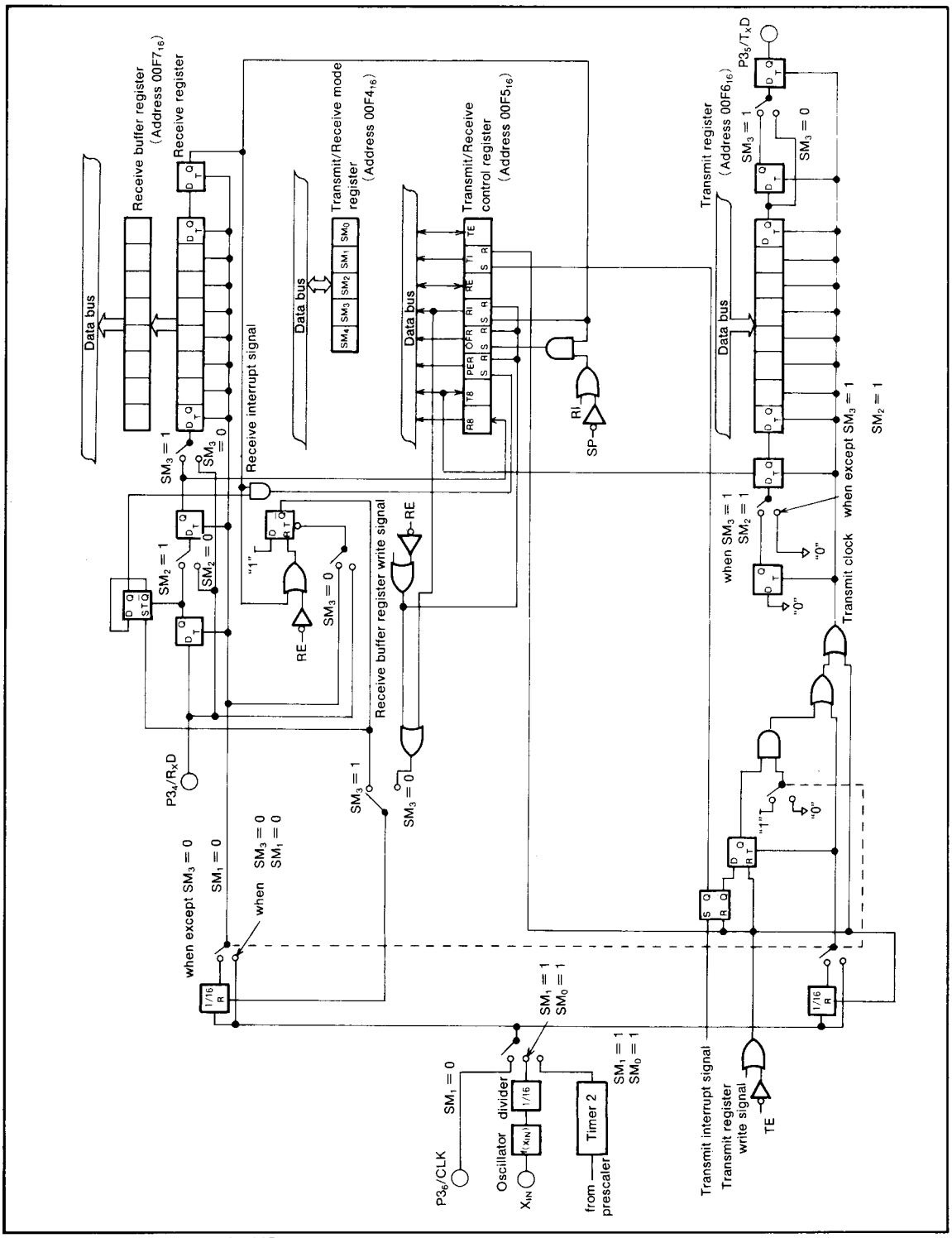


Fig.7 Block diagram of serial I/O

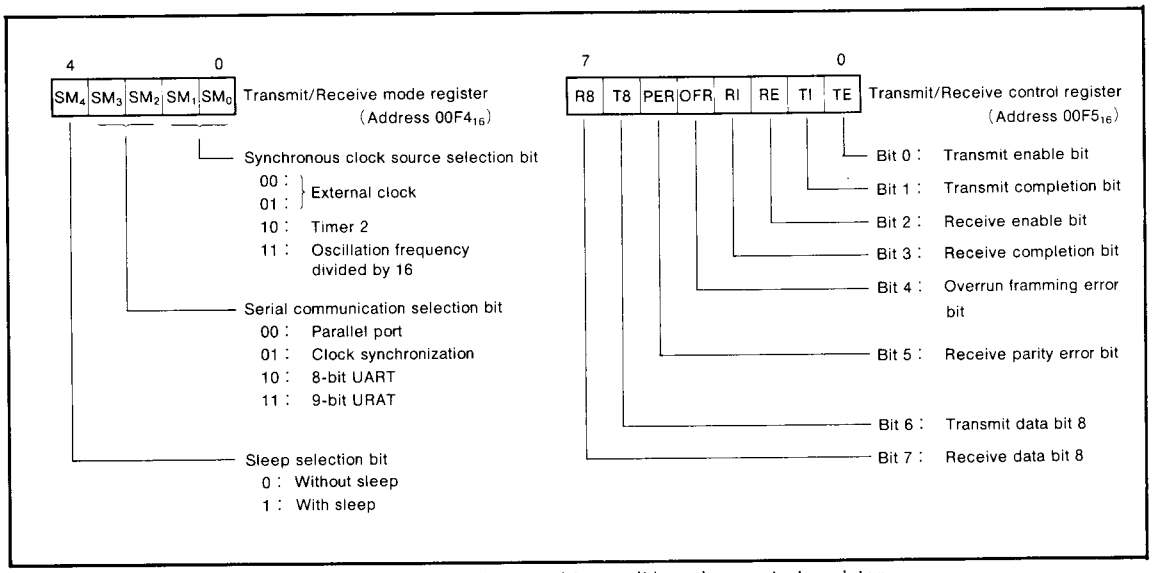


Fig.8 Bit structure of transmit/receive mode register and transmit/receive control register

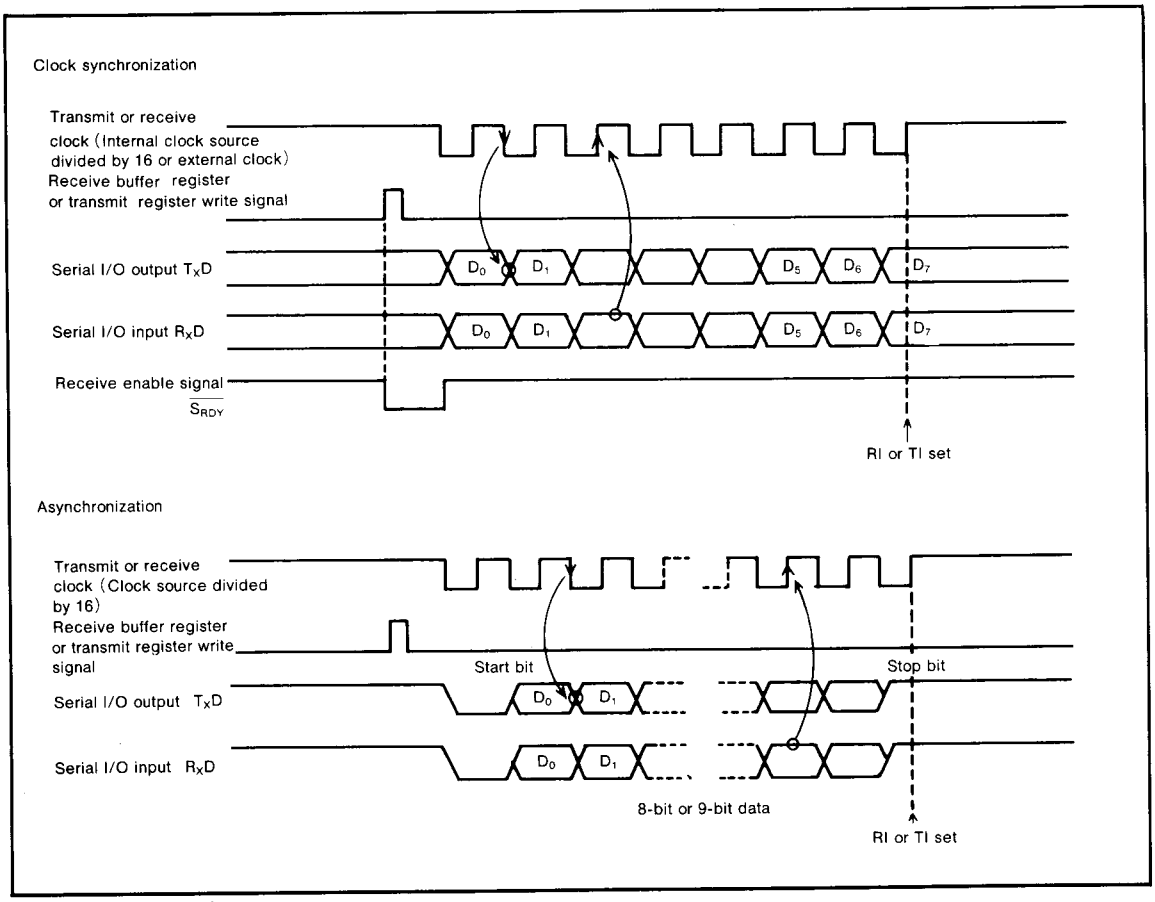


Fig.9 Serial I/O timing

RESET CIRCUIT

The M50747-XXXSP is reset according to the sequence shown in Figure 10. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 11.
An example of the reset circuit is shown in Figure 12.
When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

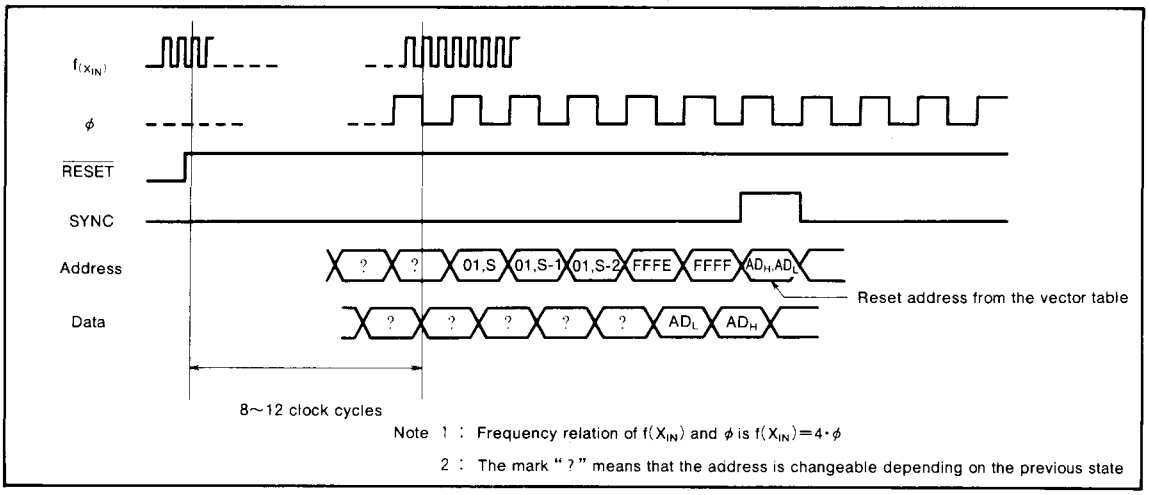


Fig.10 Timing diagram at reset

Address		
(1) Port P0 directional register	($E1_{16}$) ···	00_{16}
(2) Port P1 directional register	($E3_{16}$) ···	00_{16}
(3) Port P2 directional register	($E5_{16}$) ···	00_{16}
(4) Port P3 directional register	($E9_{16}$) ···	00_{16}
(5) Port P4 directional register	(EB_{16}) ···	00_{16}
(6) Port 6 (Note 1)	(EE_{16}) ···	FF_{16}
(7) Transmit/Receive mode register	($F4_{16}$) ···	0 0 0 0 0
(8) Transmit/Receive control register	($F5_{16}$) ···	0 0 0 0 0 0 0
(9) Prescaler X	(FC_{16}) ···	FF_{16}
(10) Timer X	(FD_{16}) ···	01_{16}
(11) Interrupt control register	(FE_{16}) ···	00_{16}
(12) Timer control register	(FF_{16}) ···	10_{16}
(13) Interrupt disable flag for processor status register	(PS) ···	1
(14) Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
	(PC_L) ···	Contents of address $FFFE_{16}$

Note 1 : Port P6 is the high-impedance state during reset. After return from reset, it is "FF_{16}".

Fig.11 Internal state of microcomputer at reset

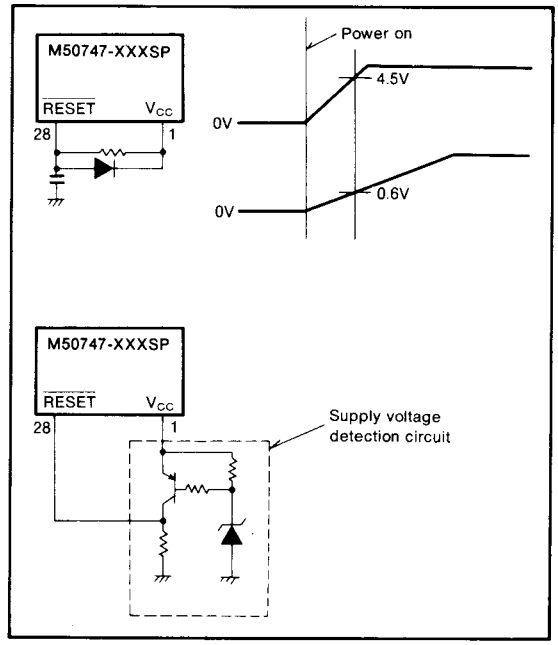


Fig.12 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O, $\overline{INT_2}$ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4

Port P4 has the same function as port P0 in the single-chip mode. This function does not change even though the processor mode changes.

(6) Port P5

Port P5 is an input.

(7) Port P6

Port P6 is a CMOS output port. See Figure 13 for more details.

(8) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

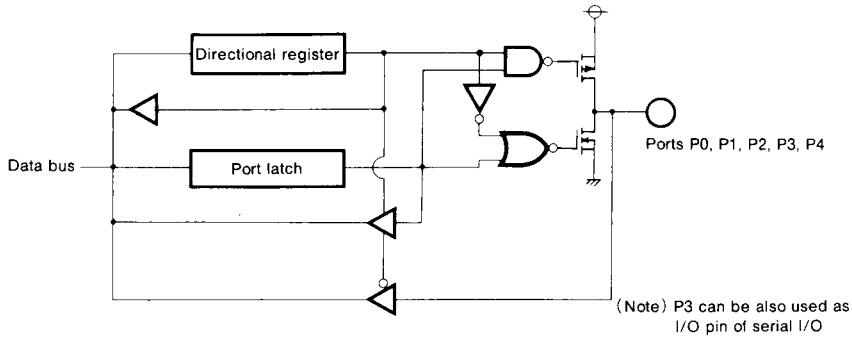
(10) $\overline{INT_2}$ pin ($P3_2/\overline{INT_2}$ pin)

The $\overline{INT_2}$ pin is an interrupt input pin used with $P3_2$. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

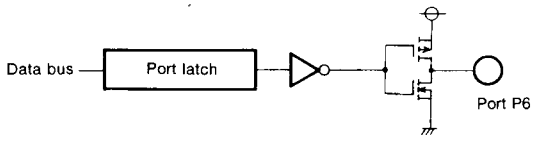
(11) CNTR pin ($P3_3$/CNTR pin)

The $P3_3$/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

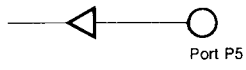
Ports P0, P1, P2, P3, P4



Port P6



Port P5



ϕ

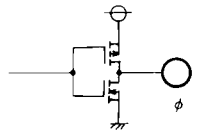


Fig.13 Block diagram of ports P0~P6 (single-chip mode), and ϕ output format

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 15 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 14.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

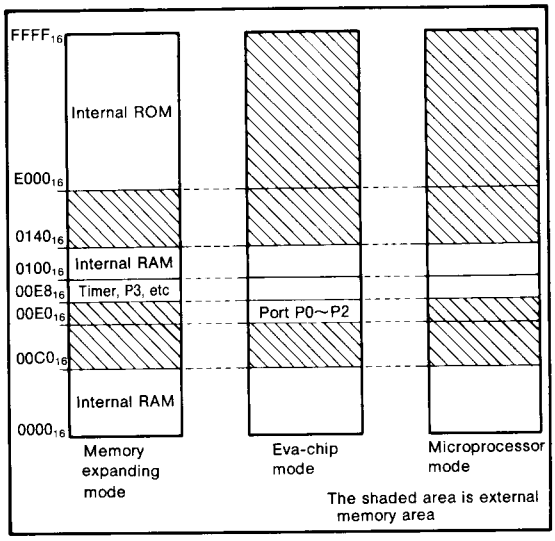


Fig.14 External memory area in processor mode

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]
The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.
In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. Port P2 becomes the data bus of D_7～D_0 (including instruction code) and loses its normal I/O functions. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively when ϕ enters into the "H" state. Port $P3_2$ functions as an input port during this same transition.

(3) Microprocessor mode [10]
After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.
In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D_7～D_0) and loses its normal I/O functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]
When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.
In this mode, the internal ROM is inhibited so the external memory is requierd.
The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.
Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.
The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.
The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.
The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

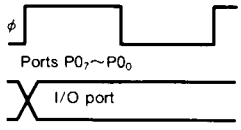
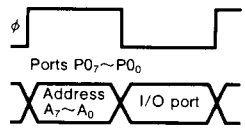
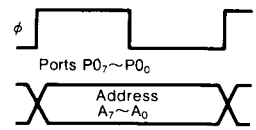
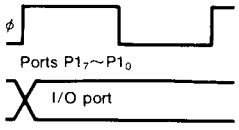
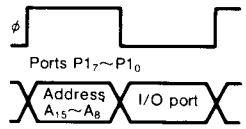
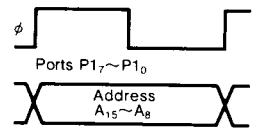
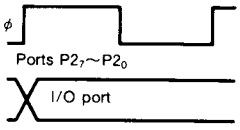
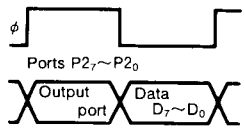
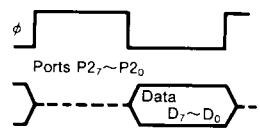
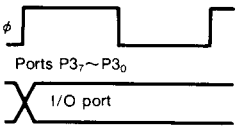
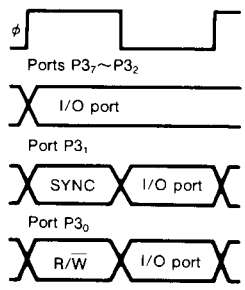
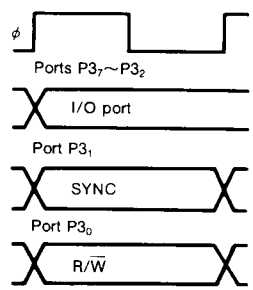
Port \ Mode	CM_1 = 0, CM_0 = 0 Single-chip mode	CM_1 = 1, CM_0 = 1 Eva-chip mode	CM_1 = 0, CM_0 = 1 Memory expanding mode	CM_1 = 1, CM_0 = 0 Microprocessor mode
Port P0				Same as left
Port P1				Same as left
Port P2				Same as left
Port P3				Same as left

Fig.15 Processor mode and functions of ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 18.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 16.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 17. X_{IN} is the input, and X_{OUT} is open.

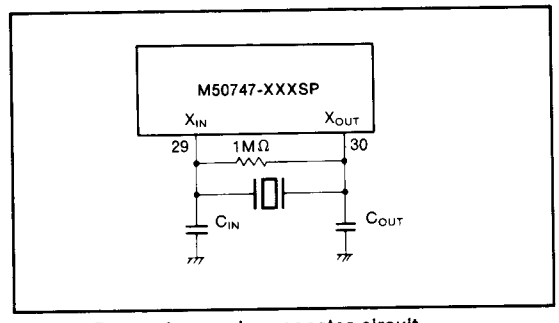


Fig.16 External ceramic resonator circuit

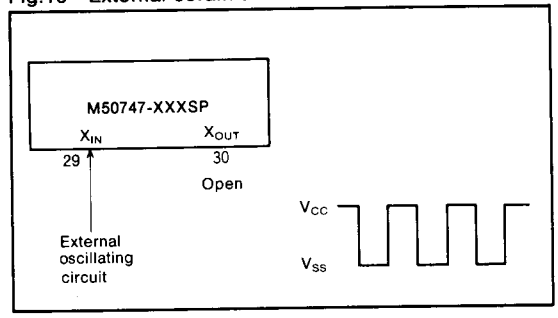


Fig.17 External clock input circuit

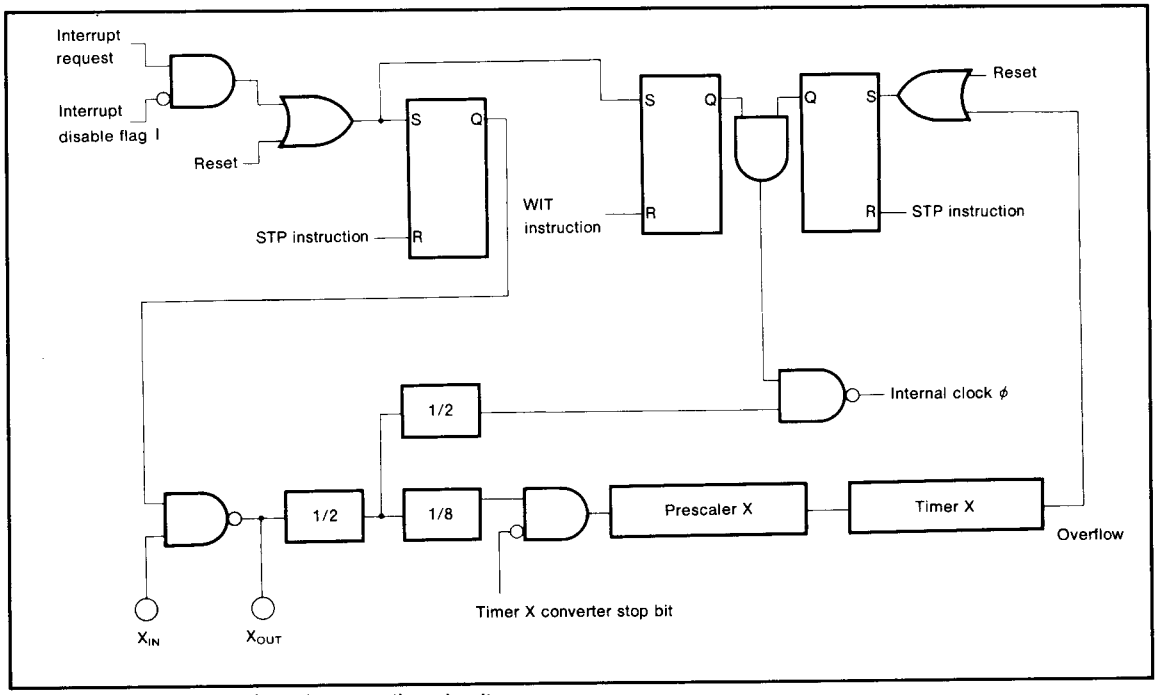


Fig.18 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off	−0.3～7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, $\overline{INT_1}$, $P5_0$～$P5_7$		−0.3～7	V
V_I	Input voltage, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$,		−0.3～V_{CC}+0.3	V
V_I	Input voltage, CNV_{SS}		−0.3～13	V
V_O	Output voltage, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P6_0$～$P6_7$, X_{OUT}, ϕ		−0.3～V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10～70	℃
Tstg	Storage temperature		−40～125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P5_0$～$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P5_0$～$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P6_0$～$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P6_0$～$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P6_0$～$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7P6_0$～$P6_7$, (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			8	MHz

Note 2 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms

3 : Total of $I_{OL(peak)}$, of ports P0, P1, and P2 is 20mA
Total of $I_{OH(peak)}$, of ports P0, P1, and P2 is 20mA
Total of $I_{IL(peak)}$, of ports P3, P4, and P6 is 80mA
Total of $I_{OH(peak)}$, of ports P3 and P4 is 20mA
Let the total of $I_{OH(peak)}$, of ports P6 below 60mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OH} = −10mA		3			V
V_{OH}	"H" output voltage, ϕ	I_{OH} = −2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OL} = 10mA				2	V
V_{OL}	"L" output voltage, ϕ	I_{OL} = 5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_6$	When used as CLK input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_2$	When used as $\overline{INT_2}$ pin		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_3$	When used as CNTR input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}			0.1		0.5	V
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 0V				−5	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 5V				5	μA
V_{RAM}	RAM retention voltage	At stop mode		2			V
I_{CC}	Supply current	Output terminals are opened, others to V_{SS}	$f_{(X_{IN})}$ = 8MHz Square wave		6	12	mA
			At stop mode T_a = 25℃			1	μA
			At stop mode T_a = 70℃			10	μA

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_c	External clock input cycle time	125			ns
t_w	External clock input pulse width	62			ns
t_r	External clock rising edge time			20	ns
t_f	External clock falling edge time			20	ns

Eva-chip mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	150			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	150			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.19			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns

Eva-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.19			150	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				150	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				150	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				150	ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.19			150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time		30		150	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns

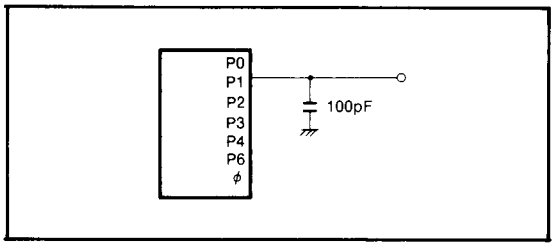
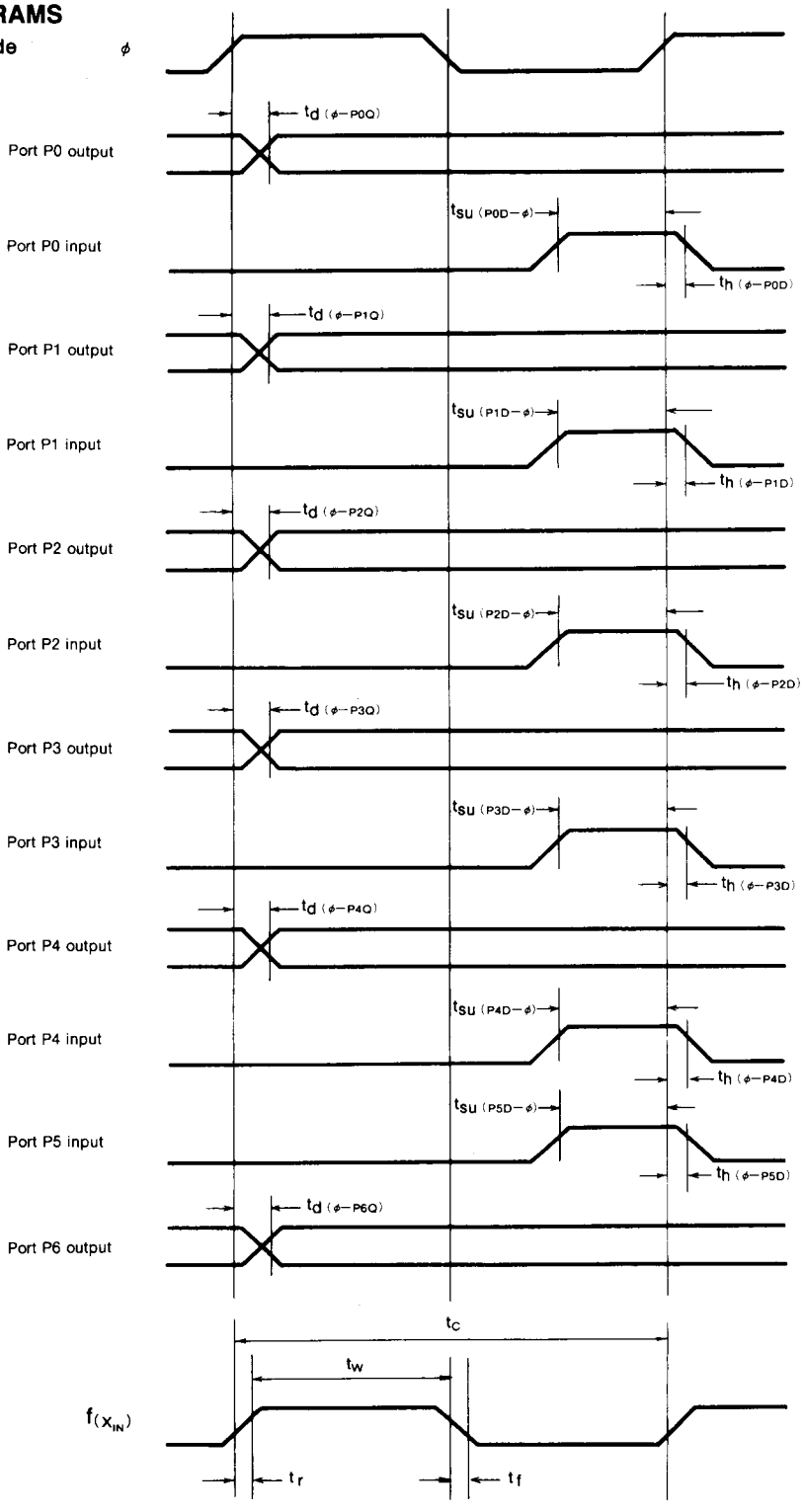


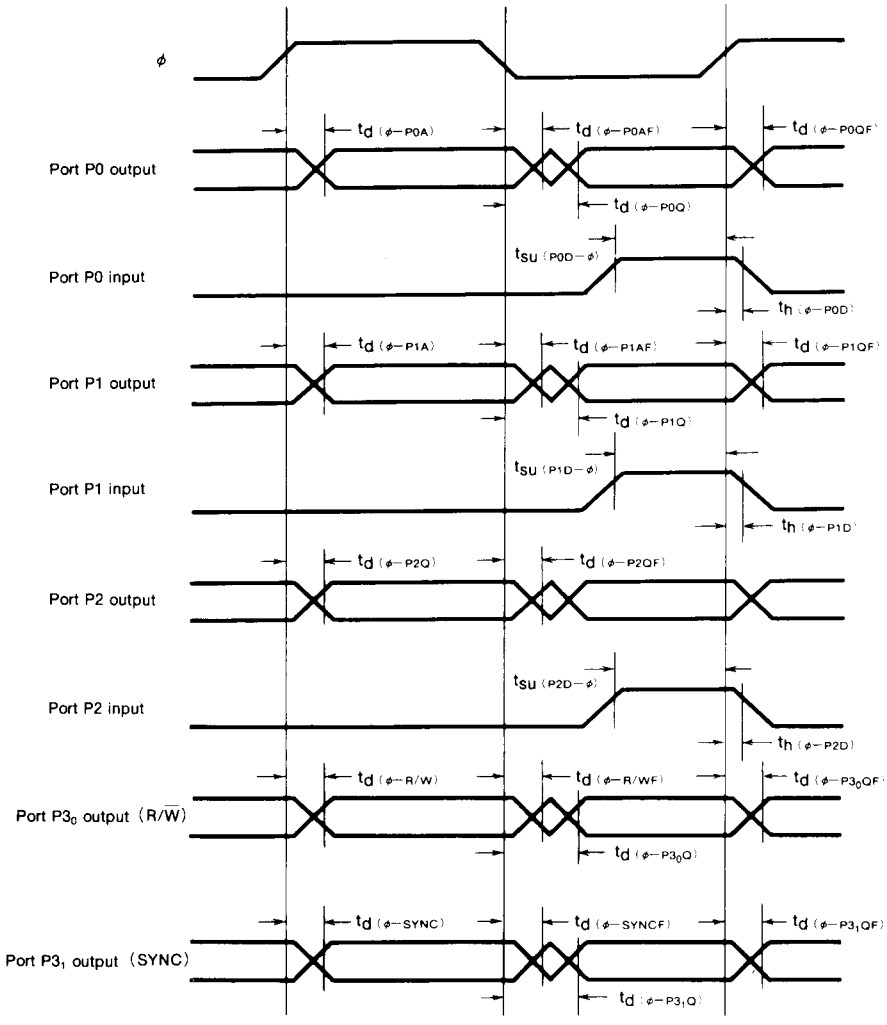
Fig.19 Ports P0~P4 and port P6 test circuit

TIMING DIAGRAMS

In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode