M512x : Mega I/O Controller with Plug & Play

- **Supports Windows 95 Plug and Play**
- **Supports 2 serial/1 parallel/FDC/RTC/KB and PS/2 mouse functions**
- **Supports 22 General Purpose I/O pins**
- **Enhanced ESD/LATCH up to over 4KV/300 mA**
- **Supports SPP, PS/2, EPP, ECP and 1284 compliance**
- **Supports 5 GPIO Alternative function pins for Remote Control**
- **Supports IR via UART1, UART2 and two additional IR pins**
- **Supports Fast Gate A20 and RC functions**
- **Supports KBC and RTC enable/disable functions**
- **Single-chip Notebook/Desktop solution**

FEATURES

- Supports Windows 95 Plug-and-Play
- Supports 2 Serial / 1 Parallel / FDC / RTC / KB / PS/2 Mouse functions
- Supports 22 General Purpose I/O pins
  - 3 GPIO ports (Ports 1, 2, 3)
  - 5 GPIO-ALT function pins for Remote Control (Pins 30-34)
  - 2 General Purpose chip select pins (Pins 24-25)
  - Supports I^2C Control Pins
- 2.88 MB Floppy Disk Controller
  - Software compatible with 82077 and supports 16-byte data FIFOs
  - High performance internal data separator
  - Supports standard 1 Mbps / 500 Kbps / 300 Kbps / 250 Kbps data rate
  - Supports 3 modes of 3.5" FDD (720K/1.2M/1.44MB)
  - Swappable drives A and B
- Supports FDC through Parallel Port pins
- Supports AT PS/2 KB and PS/2 Mouse
- Built-in Keyboard Controller and Real Time Clock
- Various modes of Parallel Port

  Supports ECP/ EPP / PS/2 / SPP and 1284 Compliance
  - IBM PC/XT, PC/AT and PS/2 compatible Bi-directional parallel port
  - Enhanced Parallel Port (EPP) compatible
  - Microsoft and Hewlett Packard Extended Capabilities Port (ECP) compatible
- Serial ports
  - Two high performance 16550 compatible UARTs with send/receive 16-byte FIFOs
  - Serial Infra Red (SIR) for wireless communications
  - MIDI (Musical Instrument Digital Interface) compatible
- High performance Power Management for FDC, UART and Parallel Port
- Supports XD-To-SD Bus Buffer and Control Pins
- Supports Enable/Disable KBC and RTC
- Supports Fast Gate A20 and RC function
- Supports External KBC programming pin functions
- Supports additional IrDA and ASK IR Pins
- Supports Phoenix KBC (M5123), AMI KBC(M5125)
- 160-pin PQFP package

Table of Contents :

Section 1 : Introduction

Features and Functions

The Acer Labs' M512x chip has two full-function universal asynchronous receiver/ transmitters (UARTs), a keyboard interface, real time clock, a floppy disk controller (FDC) with data separator, parallel port, standard XT/AT address decoding for on-chip functions, and a configuration register. It offers a single-chip solution to the most common IBM PC, XT, AT and Notebook peripherals.

The floppy disk controller is fully compatible with the industry-standard 765A and 82077SL architecture. It includes more advanced options such as a high performance data separator, extended track range to 4096, high performance power management, implied seek command, scan command, and supports both IBM and ISO 360K/1.2M/720K/1.44M/2.88M FDD formats. The UARTs are compatible with either the INS8250N-B, NS16450 and 16550. It has complete compatibility with the IBM AT's parallel port. The configuration register is one-byte wide and can be programmed via hardware or software. By controlling this register, the user can assign standard AT addresses and disable any major on-chip function (e.g., the FDC, either UART, or the parallel port) independent of the others. This allows for flexibility in system configuration when adapter boards contain duplicate functions.

The M512x provides support for the ISA Plug-and-Play standard and recommended functionality to support Windows ' 95. Through internal configuration registers, each of the M512x' s logic device' s I/O address, DMA channel and IRQ channel may be programmed. There are 96 I/O address location options, 13 IRQ options, and three DMA channel options for each logical device except KBC and RTC. KBC' s I/O address is not routable. RTC' s I/O address and IRQ are not routable as well.

1.2 M512x Block Diagrams

The following figures show the overall block diagram of the M512x.

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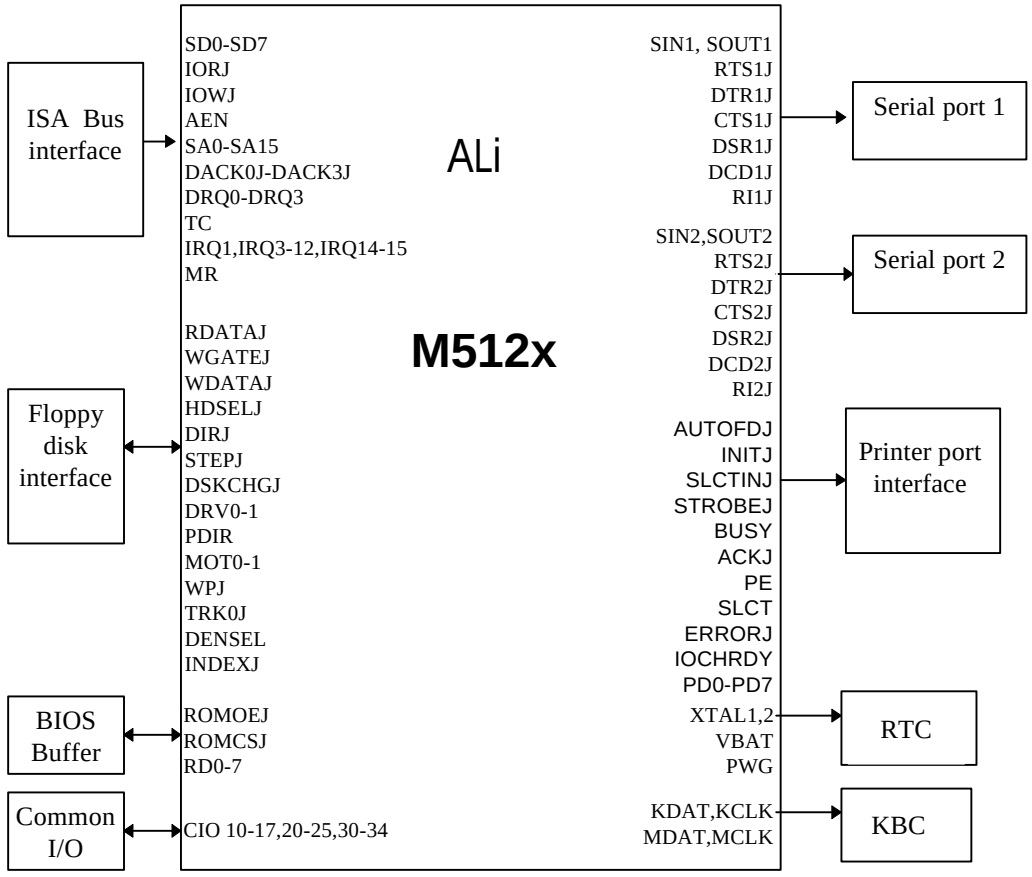

Figure 1-1 M512x Block Diagram

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1.3 Register Overview

Table 1-1 I/O Address Decode

Address Range	Block Name	Logical Device	Function
Base + (0-5) and + (7)	Floppy Disk	0	
Base + (0-7)	Serial Port COM1	4	IR support
Base + (0-7)	Serial Port COM2	5	IR support
	Parallel port	3	
Base + (0-3)	SPP		
Base + (0-7)	EPP		
Base + (0-3), + (400-402)	ECP		
Base + (0-7), + (400-402)	ECP+EPP+SPP		
0x60, 0x64	KBC	7	
0x70, 0x71	RTC	6	

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Section 2 : Pin Description

2.1 Pinout Diagram

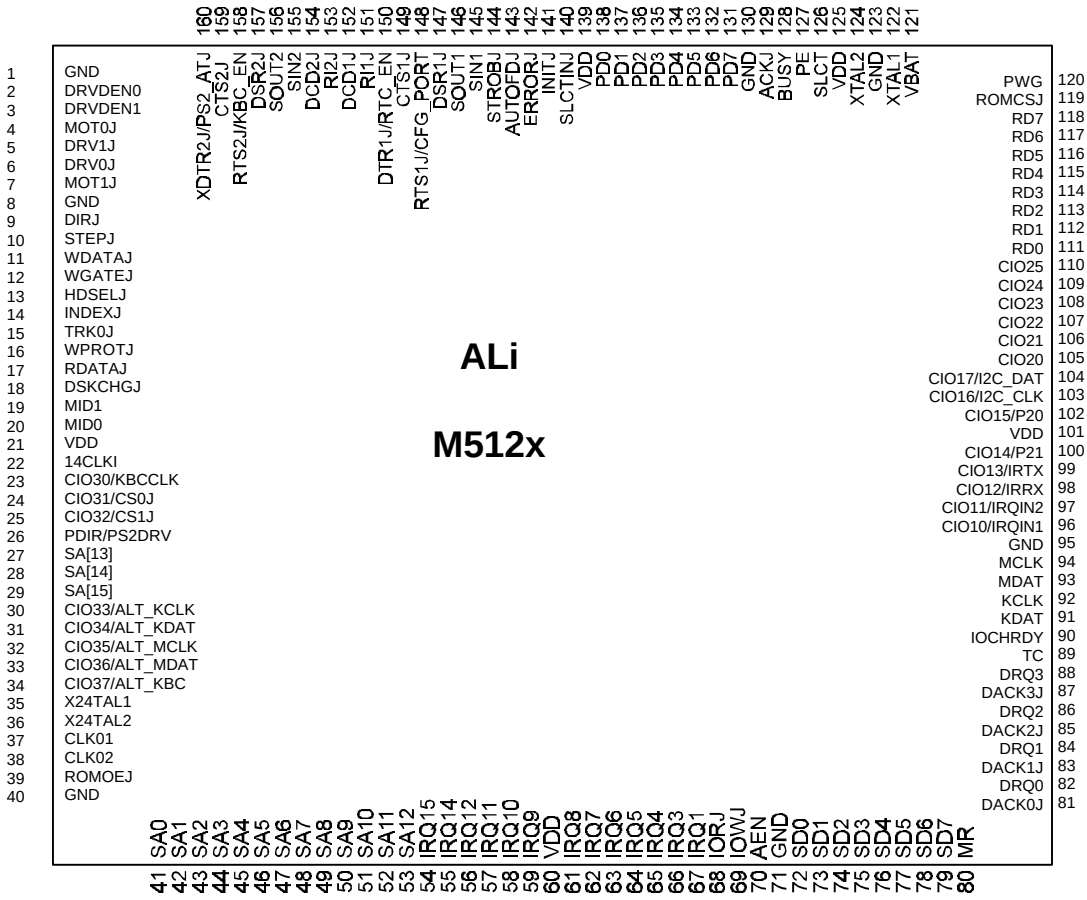

Figure 2-1. M512x Pin Diagram

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2.2 Pin Description

Table 2-1 lists the functions of all M512x pins. A low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Table 2-1 M512x Pin Description Table

Name	Number	Type	Description
HOST Processor Interface			
SD0-SD7	70-72	I/O	**Data bus**. These signals are used by the host microprocessor to transmit data to and from the M512x. These pins are in high impedance state when not in the output mode.
IORJ	68	I	**I/O Read**. This active low signal is issued by the host microprocessor to indicate a read operation.
IOWJ	69	I	**I/O Write**. This active low signal is issued by the host microprocessor to indicate a write operation.
AEN	70	I	**Address Enable**. This active high signal indicates DMA operations on the host data bus.
SA0-SA15	41-53, 27-29	I	**I/O Address**. These bits determine the I/O address to be accessed during IORJ and IOWJ cycles.
DACK0J-DACK3J	81,83,85,87	I	**DMA Acknowledge.** An active low input signal acknowledging the request for a DMA data transfer. This input enables the DMA read or write internally.
DRQ0-DRQ3	82,84,86,88	O	**DMA request**. This active high output is the DMA request for byte transfers of data to the host. This signal is cleared on the last byte of the data transfer by the DACKJ signal going low.
TC	89	I	**Terminal Count**. This signal indicates to the M512x that data transfer is complete. TC is only accepted when DACKJ is low. TC is active high in AT mode and active low in PS/2 mode.
IRQ1, IRQ3-12, IRQ14-15	67,66,65,64, 63,62,61,59, 58,57,56,55, 54	O	**Interrupt Requests**.
MR	80	IS	**Reset**. This active high signal resets the M512x and must be valid for 500 ns minimum. In M512x, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid 50 ns prior to this edge.
Floppy Disk Interface			
RDATAJ	17	IS	**Read Disk Data.** This raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
WGATEJ	12	O	**Write Gate**. This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. Unstable power prevents writing to the disk.
WDATAJ	11	O	**Write Data**. This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
HDSELJ	13	O	**Head Select**. This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
DIRJ	9	O	**Direction.** This active low output determines the direction of the head movement (low = step-in, high = step-out). During write or read modes, this output is high.
STEPJ	10	O	**Step.** This active low signal produces a pulse to move the head during a seek operation.
DSKCHGJ	18	IS	**Disk Change.** This disk interface signal indicates when the disk drive door is open. This signal is read from bit D7 of address xx7h.

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
Floppy Disk Interface :			
DRV0J, DRV1J	6, 5	O	**Drive Select 0, 1**. Active low, output select drives 0-1.
PDIR	26	O	This bit is used to indicate the direction of the Parallel port data bus. 0= output/write, 1= input / read.
PS2DRV		I	**Drive 2**. In PS/2 mode, this input indicates whether a second drive is connected; this signal should be low if a second drive is connected. This status is reflected in a read of Status Register A.
MID0-1	20,19	IS	**Media ID inputs.** In floppy enhanced mode, these inputs are the media ID inputs.
MOT0J, MOT1J	4, 7	O	**Motor on 0, 1**. These active-low outputs select motor drives 0-1.
WPROTJ	16	IS	**Write Protected**. This active-low Schmitt Trigger input senses from the disk drive that a disk is write-protected. Any write command is ignored.
TRK0J	15	IS	**Track 00**. This Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.
INDEXJ	14	IS	**Index**. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
DRVDEN 0-1	2-3	O	**Data Rate 0-1**. This output reflects bits 0-1 of the Data Rate Register.
Serial Port Interface :			
SIN1, SIN2	145,155	I	**Receive Data**. Receiver serial data input.
SOUT1, SOUT2	146,156	O	**Transmit Data**. Transmitter serial data output from Serial Port.
RTS1J	148	O	**Request to send**. Active low Request to send output for Primary Serial port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation.
CFGPORT		I	**Configuration port select**. During reset active, this input is read and latched to define the configuration register' s base address.
RTS2J	158	O	**Request to send**. This active low signal for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation.
KBC_EN		I	**KBC enable control**. During reset active, this input is read and latched to enable KBC after reset. The signal can be overwritten by configuration register.
DTR1J	150	O	**Data Terminal Ready**. This is an active low output for primary serial port. Handshake output signal signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation.
RTC_EN		I	**RTC enable control**. During reset active, this input is read and latched to enable RTC after reset. This signal can be overwritten by configuration register.

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
Serial Port Interface :			
DTR2J	160	O	**Data Terminal Ready**. This active low output is for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive mode (high). Forced inactive during loop mode operation.
PS2_ATJ		I	**KBC PS2 mode or AT mode select**. When active, this input is read and latched to define the KBC PS-2 or AT mode.
CTS1J CTS2J	149, 159	I	**Clear to Send**. This active low input for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTSJ signal state is directly comparative with the MSR bit after the last MSR read. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTSJ changes state. The CTSJ signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTSJ.
DSR1J DSR2J	147, 157	I	**Data Set Ready.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSRJ signal by reading bit5 of Modem Status Register (MSR). A DSRJ signal state change from low to high after the last MSR read will raise the MSR bit 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSRJ changes state. Note: Bit 5 of MSR is the complement of DSRJ.
DCD1J, DCD2J	152, 154	I	**Data Carrier Detect**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCDJ signal by reading bit 7 of Modem Status Register (MSR). A DCDJ signal state rises after the last MSR read will raise MSR bit 3. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. Note : bit 7 of MSR is the complement of DCDJ.
RI1J, RI2J	151, 153	I	**Ring Indicator**. This active low input is for primary and secondary serial ports. Handshake signal that notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RIJ signal by reading bit 6 of Modem Status Register (MSR). A risen RIJ signal state after the last MSR read will raise MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RIJ changes state. Note : bit 6 of MSR is the complement of RIJ.

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
Printer Port Interface			
AUTOFDJ	143	O	**Autofeed Output**. This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
INITJ	141	O	**Initiate Output**. This active low signal is bit 2 of the printer control register. This signal is used to initialize the printer.
SLCTINJ	140	O	**Printer select input**. This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
STROBEJ	144	O	**Strobe Output**. This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
BUSY	128	IS	**Busy**. This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
ACKJ	129	IS	**Acknowledge**. This active low signal from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACKJ input.
PE	127	IS	**Paper End**. This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
SLCT	126	IS	**Printer Selected Status**. This active high signal from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
ERRORJ	142	I	**Error**. This active low signal indicates an error condition at the printer.
PD0-PD7	138-131	I/O	**Port Data**. This bi-directional parallel data bus is used to transfer information between CPU and peripherals.
IOCHRDY	90	OD	**IOCHRDY**. In EPP mode, this pin is pulled low to extend the read/write command.
Real-Time Clock			
XTAL1	122	ICLK	**32Khz Crystal Input**.
XTAL2	124	OCLK	**32Khz Crystal Output**.
VBAT	121	P	**Battery Voltage.**
PWG	120	IS	**Power Good Input.**
Keyboard Controller			
KDAT	91	I/O	**Keyboard Data.**
KCLK	92	I/O	**Keyboard Clock.**
MDAT	93	I/O	**Mouse Data.**
MCLK	94	I/O	**Mouse Clock.**

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
BIOS Buffer :			
ROMOEJ	39	IS	**ROM Output Enable.**
ROMCSJ	119	IS	**ROM Chip Select.**
RD0-7	111-118	I/O	**ROM Bus.**
Common I/O :			
CIO10-11	96-97	I/O I	**Common I/O pin.** **IRQ In.**
CIO12	98	I/O I	**Common I/O pin.** **IRRX.**
CIO13	99	I/O O	**Common I/O pin.** **IRTX.**
CIO14	100	I/O O	**Common I/O pin.** **KBC P21 function.**
CIO15	102	I/O O	**Common I/O pin.** **KBC P20 function.**
CIO16	103	I/O O	**Common I/O pin.** **I^2C_CLK.**
CIO17	104	I/O I/O	**Common I/O pin.** **I^2C_DAT.**
CIO20-24	105-109	I/O	**Common I/O pin.**
CIO25	110	I/O I	**Common I/O pin.** **KEYLOCKJ.**
CIO30	23	I/O I	**Common I/O pin.** **KBC_CLK.**
CIO31	24	I/O O	**Common I/O pin.** **General Chip Select decoder CS0J.**
CIO32	25	I/O O	**Common I/O pin.** **General Chip Select decoder CS1J.**
CIO33	30	I/O O	**Common I/O pin.** **Alternative Keyboard Clock.**
CIO34	31	I/O O	**Common I/O pin.** **Alternative Keyboard Data.**
CIO35	32	I/O O	**Common I/O pin.** **Alternative Mouse Clock.**
CIO36	33	I/O O	**Common I/O pin.** **Alternative Mouse Data.**
CIO37	34	I/O I	**Common I/O pin.** **Alternative KBC select.**

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
Miscellaneous			
X24TAL1	35	ICLK	**Clock 1**. This is an external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used.
X24TAL2	36	OCLK	**Clock 2**. This is a 24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
X14CLKI	22	I	**Clock 14 In**. This is a 14.318 MHz clock source in.
XCLKO1	37	O	**Clock 14 out**. This is a 14.318 MHz clock out.
XCLKO2	38	O	**Clock 14 out**. This is the second 14.318 MHz clock out.
Power Pins			
Vcc	21,60,101, 125,139	P	**Power**. +5 Volt supply pin.
Vss	1,8,40,71,95, 123,130	P	**Ground pins**.

Type Description :

I	Input TTL compatible.
IS	Input with Schmitt Trigger.
ICLK	CLK input.
OCLK	CLK output.
O4	Output with 4 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
OD24	Open drain outputs, sinks 24 mA @ 0.4 V.

2.3 Numerical Pin List

Pin No.	Pin Name	Type
1	Vss	P
2	DRVDEN0	O
3	DRVDEN1	O
4	MOT0J	O
5	DRV1J	O
6	DRV0J	O
7	MOT1J	O
8	Vss	P
9	DIRJ	O
10	STEPJ	O
11	WDATAJ	O
12	WGATEJ	O
13	HDSELJ	O
14	INDEXJ	IS
15	TRK0J	IS
16	WPROTJ	IS
17	RDATAJ	IS
18	DSKCHGJ	IS
19	MID1	IS
20	MID0	IS
21	Vcc	P
22	X14CLKI	I
23	CIO30/ KBC_CLK	I/O
24	CIO31/CS0J	I/O
25	CIO32/CS1J	I/O
26	PDIR/PS2DRV	I/O
27	SA13	IS
28	SA14	IS
29	SA15	IS
30	CIO33/ ALT_KCLK	I/O
31	CIO34/ ALT_KDAT	I/O
32	CIO35/ ALT_MCLK	I/O
33	CIO36/ ALT_MDAT	I/O
34	CIO37/ ALT_KBC	I/O
35	X24TAL1	ICLK
36	X24TAL2	OCLK
37	XCLKO1	O
38	XCLKO2	O
39	ROMOEJ	IS
40	Vss	P

Pin No.	Pin Name	Type
41	SA0	IS
42	SA1	IS
43	SA2	IS
44	SA3	IS
45	SA4	IS
46	SA5	IS
47	SA6	IS
48	SA7	IS
49	SA8	IS
50	SA9	IS
51	SA10	IS
52	SA11	IS
53	SA12	IS
54	IRQ15	O
55	IRQ14	O
56	IRQ12	O
57	IRQ11	O
58	IRQ10	O
59	IRQ9	O
60	Vcc	P
61	IRQ8	O
62	IRQ7	O
63	IRQ6	O
64	IRQ5	O
65	IRQ4	O
66	IRQ3	O
67	IRQ1	O
68	IORJ	IS
69	IOWJ	IS
70	AEN	IS
71	Vss	P
72	SD0	I/O
73	SD1	I/O
74	SD2	I/O
75	SD3	I/O
76	SD4	I/O
77	SD5	I/O
78	SD6	I/O
79	SD7	I/O
80	MR	IS

Numerical Pin List (continued)

Pin No.	Pin Name	Type
81	DACK0J	IS
82	DRQ0	O
83	DACK1J	IS
84	DRQ1	O
85	DACK2J	IS
86	DRQ2	O
87	DACK3J	IS
88	DRQ3	O
89	TC	IS
90	IOCHRDY	OD
91	KDAT	I/O
92	KCLK	I/O
93	MDAT	I/O
94	MCLK	I/O
95	Vss	P
96	CIO10/IRQIN1	I/O
97	CIO11/IRQIN2	I/O
98	CIO12/IRRX	I/O
99	CIO13/IRTX	I/O
100	CIO14/GA20	I/O
101	Vcc	P
102	CIO15/KBRCJ	I/O
103	CIO16/I^2C_CLK	I/O
104	CIO17/I^2C_DAT	I/O
105	CIO20	I/O
106	CIO21	I/O
107	CIO22	I/O
108	CIO23	I/O
109	CIO24	I/O
110	CIO25	I/O
111	RD0	I/O
112	RD1	I/O
113	RD2	I/O
114	RD3	I/O
115	RD4	I/O
116	RD5	I/O
117	RD6	I/O
118	RD7	I/O
119	ROMCSJ	IS
120	PWG	IS

Pin No.	Pin Name	Type
121	VBAT	P
122	X32TAL1	ICLK
123	Vss	P
124	X32TAL2	OCLK
125	Vcc	P
126	SLCT	IS
127	PE	IS
128	BUSY	IS
129	ACKJ	IS
130	Vss	P
131	PD7	I/O
132	PD6	I/O
133	PD5	I/O
134	PD4	I/O
135	PD3	I/O
136	PD2	I/O
137	PD1	I/O
138	PD0	I/O
139	Vcc	P
140	SLCTINJ	O
141	INITJ	O
142	ERRORJ	I
143	AUTOFDJ	O
144	STROBJ	O
145	SIN1	IS
146	SOUT1	O
147	DSR1J	IS
148	RTS1J/ CFG_PORT	I/O
149	CTS1J	IS
150	DTR1J/RTC_EN	I/O
151	RI1J	IS
152	DCD1J	IS
153	RI2J	IS
154	DCD2J	IS
155	SIN2	IS
156	SOUT2	O
157	DSR2J	IS
158	RTS2J/KBC_EN	I/O
159	CTS2J	IS
160	DTR2J/PS2_ATJ	I/O

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2.4 Alphabetical Pin List

Pin No.	Pin Name	Type
129	ACKJ	IS
70	AEN	IS
143	AUTOFDJ	O
128	BUSY	IS
96	CIO10/IRQIN1	I/O
97	CIO11/IRQIN2	I/O
98	CIO12/IRRX	I/O
99	CIO13/IRTX	I/O
100	CIO14/GA20	I/O
102	CIO15/KBRCJ	I/O
103	CIO16/I^2C_CLK	I/O
104	CIO17/I^2C_DAT	I/O
105	CIO20	I/O
106	CIO21	I/O
107	CIO22	I/O
108	CIO23	I/O
109	CIO24	I/O
110	CIO25	I/O
23	CIO30/KBC_CLK	I/O
24	CIO31/CS0J	I/O
25	CIO32/CS1J	I/O
30	CIO33/ALT_KCLK	I/O
31	CIO34/ALT_KDAT	I/O
32	CIO35/ALT_MCLK	I/O
33	CIO36/ALT_MDAT	I/O
34	CIO37/ALT_KBC	I/O
149	CTS1J	IS
159	CTS2J	IS
81	DACK0J	IS
83	DACK1J	IS
85	DACK2J	IS
87	DACK3J	IS
152	DCD1J	IS
154	DCD2J	IS
9	DIRJ	O
82	DRQ0	O
84	DRQ1	O
86	DRQ2	O
88	DRQ3	O
2	DRVDEN0	O

Pin No.	Pin Name	Type
3	DRVDEN1	O
5	DRV1J	O
6	DRV0J	O
18	DSKCHGJ	IS
147	DSR1J	IS
157	DSR2J	IS
150	DTR1J/RTC_EN	I/O
160	DTR2J/PS2_ATJ	I/O
142	ERRORJ	I
13	HDSELJ	O
14	INDEXJ	IS
141	INITJ	O
90	IOCHRDY	OD
68	IORJ	IS
69	IOWJ	IS
67	IRQ1	O
66	IRQ3	O
65	IRQ4	O
64	IRQ5	O
63	IRQ6	O
62	IRQ7	O
61	IRQ8	O
59	IRQ9	O
58	IRQ10	O
57	IRQ11	O
56	IRQ12	O
55	IRQ14	O
54	IRQ15	O
91	KDAT	I/O
92	KCLK	I/O
94	MCLK	I/O
93	MDAT	I/O
19	MID1	IS
20	MID0	IS
4	MOT0J	O
7	MOT1J	O
80	MR	IS
138	PD0	I/O
137	PD1	I/O
136	PD2	I/O

Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
135	PD3	I/O
134	PD4	I/O
133	PD5	I/O
132	PD6	I/O
131	PD7	I/O
26	PDIR/PS2DRV	I/O
127	PE	IS
120	PWG	IS
111	RD0	I/O
112	RD1	I/O
113	RD2	I/O
114	RD3	I/O
115	RD4	I/O
116	RD5	I/O
117	RD6	I/O
118	RD7	I/O
17	RDATAJ	IS
151	RI1J	IS
153	RI2J	IS
119	ROMCSJ	IS
39	ROMOEJ	IS
148	RTS1J/CFG_PORT	I/O
158	RTS2J/KBC_EN	I/O
41	SA0	IS
42	SA1	IS
43	SA2	IS
44	SA3	IS
45	SA4	IS
46	SA5	IS
47	SA6	IS
48	SA7	IS
49	SA8	IS
50	SA9	IS
51	SA10	IS
52	SA11	IS
53	SA12	IS
27	SA13	IS
28	SA14	IS
29	SA15	IS
72	SD0	I/O

Pin No.	Pin Name	Type
73	SD1	I/O
74	SD2	I/O
75	SD3	I/O
76	SD4	I/O
77	SD5	I/O
78	SD6	I/O
79	SD7	I/O
145	SIN1	IS
155	SIN2	IS
140	SLCTINJ	O
126	SLCT	IS
146	SOUT1	O
156	SOUT2	O
10	STEPJ	O
144	STROBJ	O
89	TC	IS
15	TRK0J	IS
121	VBAT	P
21	Vcc	P
60	Vcc	P
101	Vcc	P
125	Vcc	P
139	Vcc	P
1	Vss	P
8	Vss	P
40	Vss	P
71	Vss	P
95	Vss	P
123	Vss	P
130	Vss	P
11	WDATAJ	O
16	WPROTJ	IS
12	WGATEJ	O
22	X14CLKI	I
35	X24TAL1	ICLK
36	X24TAL2	OCLK
122	X32TAL1	ICLK
124	X32TAL2	OCLK
37	XCLKO1	O
38	XCLKO2	O

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Section 3 : Configuration Description and Power Management Features

3.1 Configuration Port

This configuration is based on the typical Plug-and-Play architecture and allows the BIOS to assign resources at POST.

To assign M512x a configuration key, <0x51, 0x23> must be written to CONFIG PORT to enter the CONFIGURE mode. Then follow the Plug-and-Play procedure to configure each device.

A configuration key = < 0xBB > must be written to CONFIG PORT to exit the CONFIGURE mode and enter the RUN mode.

Note : After exiting the CONFIGURE mode, the current logic device select is cleared. You must select the logic device before you program it.

After a hard reset or Power on reset, the M512x is in the RUN mode with all logical devices disable except KBC and RTC. The hardware setting pins control the KBC and RTC. Then the normal configure procedure is also suitable for KBC and RTC. The hardware setting is listed on table 3-2.

All logical devices may be configured through 2 standard Configuration I/O Ports (INDEX and DATA) by placing the M512x into Configuration Mode. The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the M512x is in Configuration Mode.

A hardware setting pin CFG_PORT is latched to select the CFG_PORT as 3F0h or 370h.

Port Name	CFG_PORT=0	CFG_PORT=1	Type
CONFIG PORT	0x3F0	0x370	W
INDEX PORT	0x3F0	0x370	W
DATA PORT	0x3F1	0x371	R/W

CHIP LEVEL REGISTERS

Index name	**Hard reset, Soft reset default values**
Index 0x02h	0x00, 0x00
Bit 0	1 : Soft reset the configuration registers. This bit is automatically cleared after write. This register is write only.
Index 0x03h	0x03, N/A
Bit 1-0	Set CIO1, CIO2, and CIO3 selection register address. 00 : 0xE0 01 : 0xE2 10 : 0xE4 11 : 0xEA
Bit 7	0 : Disable access 1 : Enable access to CIO1, CIO2, and CIO3.
Index 0x07h	0x00, 0x00
Bit 3-0	Select the current logic device. This allows the access to each logical device' s registers.
Bit 7-4	Read as 0.
Index 0x20h	0x23, 0x23 ALi defined device identification. Read only.
Index 0x21h	0x51, 0x51 ALi defined device identification. Read only.

Index 0x22h 0x00, 0x00

Bit 0 Direct powerdown FDC (Note 3)
0 : disable
1 : enable

Bit 2-1 read as 0.

Bit 3 Direct powerdown Parallel Port (Note 3)
0 : disable
1 : enable

Bit 4 Direct powerdown UART1 (Note 3)
0 : disable
1 : enable

Bit 5 Direct powerdown UART2 (Note 3)
0 : disable
1 : enable

Bit 6 1: Turn off the oscillator.

Bit 7 read as 0.

Index 0x23h 0x00, N/A

Bit 2-0 read as 0.

Bit 3 Auto powerdown Parallel Port.
0 : disable
1 : enable

Bit 4 Auto powerdown UART1.
0 : disable
1 : enable

Bit 5 Auto powerdown UART2.
0 : disable
1 : enable

Bit 7-6 read as 0

Index 0x24h 0x00, N/A

Bit 5-0 read as 0.

Bit 6 0 : pin26 functions as PDIR
1 : pin26 functions as SDRV.

Bit 7 0 : IRQ8 is active high
1 : IRQ8 is active low.(Note 1)

Index 0x2Dh 0x00, N/A

Reserved for test purposes only

LOGICAL DEVICE 0 REGISTERS (FDC)

Index 0x30h 0x00, 0x00

Bit 0 FDC (Note 4)
0 : disable
1 : enable

Bit 7-1 read as 0.

Index 0x60h 0x03, 0x03
The higher address of the FDC's I/O base address.

Bit 7-2 read as 0.

Index 0x61h 0xF0, 0xF0
The lower address of the FDC's I/O base address.

Bit 2-0 set to 0.

Index 0x70h 0x06, 0x06

Bit 3-0 Select IRQ channel used by FDC.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Bit 7-4 read as 0.

Index 0x74h 0x02, 0x02

Bit 2-0 Select DMA channel used by FDC
000 : DMA0
001 : DMA1
010 : DMA2
011 : DMA3
100 : None

Bit 7-3 read as 0.

Index 0xF0h 0x08, N/A

Bit 0 0 : Normal mode
1 : Enhanced OS2 mode

Bit 1 0 : Burst DMA mode.
1 : Non-burst DMA mode

Bit 2, 7-5 read as 0.

Bit 3 0 : PS2 mode
1 : AT mode

Bit 4 0 : No swap.
1 : Swap Drive 0 and Drive 1

Index 0xF1h 0x00, N/A

Bit 1-0 External Floppy Select.
0x : internal FDC
10 : external FDC
11 : Drive A internal, Drive B external

Bit 3-2 Density Select.
0x : Normal
10 : force to 1
11 : force to 0

Bit 5-4 Media ID[1-0] polarity.
0 : normal
1 : inverted

Bit 7-6 Boot Floppy.
00 : FDD 0
01 : FDD 1
10 : FDD 2
11 : FDD 3

Index 0xF2h 0xFF, N/A

Bit 1-0 Floppy Drive A type.

Bit 3-2 Floppy Drive B type.

Bit 5-4 Floppy Drive C type.

Bit 7-6 Floppy Drive D type.

Index 0xF4h 0x00, N/A

Bit 1-0 DRVDEN[1-0] signal definition (refer to Table 3-4).

Bit 2, 7-5 read as 0.

Bit 4-3 Data Rate Table Select (refer to Table 3-3).

LOGICAL DEVICE 3 REGISTERS (Parallel Port)

Index 0x30h 0x00, 0x00

Bit 0 Activate Parallel Port. (Note 4)
0 : disable
1 : enable

Bit 7-1 read as 0.

Index 0x60h 0x03, 0x03
The higher address of the Parallel Port' s I/O base address.

Bit 7-2 read as 0.

Index 0x61h 0x78, 0x78
The lower address of the Parallel Port' s I/O base address.

Bit 1-0 set to 0.

Note : An 8-byte boundary is required if EPP is available

Index 0x70h 0x05, 0x05

Bit 3-0 Select IRQ channel used by Parallel Port.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Bit 7-4 read as 0.

Index 0x74h 0x04, 0x04

Bit 2-0 Select DMA channel used by Parallel Port.
000 : DMA0
001 : DMA1
010 : DMA2
011 : DMA3
100 : None

Bit 7-3 read as 0.

Index 0xF0h 0xBC, N/A

Bit 2-0 EPP Compatible mode.
000 : PS2
001 : EPP 1.9
010 : ECP
011 : ECP+EPP1.9
100 : SPP
101 : EPP 1.7
111 : ECP+EPP 1.7

Bit 6-3 ECP FIFO threshold value.
Default is 0001.

Bit 7 PP interrupt type (not valid when PP is in SPP or PS2 mode).
1 : IRQ active low.
0 : IRQ active high.

Index 0xF1h 0x05, N/A

Bit 0 0 : Non-burst DMA mode.
1 : Burst DMA transfer mode in ECP

Bit 1 EPP time-out interrupt.
0 : disable
1 : enable

Bit 2 PP operation clock.
0 : 24 Mhz.
1 : 12 Mhz

Bit 7-3 read as 0.

LOGICAL DEVICE 4 REGISTERS (UART1)

Index 0x30h	0x00, 0x00
Bit 0	UART1 (Note 4) 0 : disable 1 : enable
Bit 7-1	read as 0.
Index 0x60h	0x03, 0x03 The higher address of the UART1's I/O base address.
Bit 7-2	read as 0.
Index 0x61h	0xF8, 0xF8 The lower address of the UART1's I/O base address.
Bit 2-0	is set to 0.
Index 0x70h	0x04, 0x04
Bit 3-0	Select IRQ used by UART1. 0000 : None 0001 : IRQ1 0010 : N/A 0011 : IRQ3 0100 : IRQ4 0101 : IRQ5 0110 : IRQ6 0111 : IRQ7 1000 : N/A 1001 : IRQ9 1010 : IRQ10 1011 : IRQ11 1100 : IRQ12 1101 : N/A 1110 : IRQ14 1111 : IRQ15
Bit 7-4	read as 0.
Index 0xF0h	0x00, N/A
Bit 0	MIDI support 0 : disable 1 : enable
Bit 1	High speed mode 0 : disable 1 : enable
Bit 2	0 : Normal 1 : 8Mhz clock source for UART1
Bit 7-3	read as 0.
Index 0xF1h	0x00, N/A
Bit 0	IR receive polarity. 0 : active high 1 : active low
Bit 1	IR transmit polarity. 0 : active high 1 : active low
Bit 2	0 : Full duplex in IR 1 : Half duplex in IR
Bit 4-3	IR mode. 00 : Normal 01 : IrDA 10 : ASK IR 11 : Normal
Bit 7-5	read as 0.
Index 0xF2h	0x0C, N/A
Bit 0	Baud Rate output on RI1. 0 : disable 1 : enable
Bit 1	IR half-duplex Tx-to-Rx time- out timer. 0 : disable 1 : enable
Bit 2	IR half-duplex Rx-to-Tx time-out timer. 0 : disable 1 : enable
Bit 4-3	IR half-duplex time-out time control. 00: 41-bit time for TR, 39-bit time for RX. 01: 42-bit time for TR, 39-bit time for RX 1x: 40-bit time for TR and RX
Bit 7-5	read as 0.

LOGICAL DEVICE 5 REGISTERS (UART2)

Index 0x30h 0x00, 0x00

Bit 0 UART2 (Note 4)
0 : disable
1 : enable

Bit 7-1 read as 0.

Index 0x60h 0x02, 0x02
The higher address of the UART2' s I/O base address.

Bit 7-2 read as 0.

Index 0x61h 0xF8, 0xF8
The lower address of the UART2' s I/O base address.

Bit 2-0 set to 0.

Index 0x70h 0x03, 0x03

Bit 3-0 Select IRQ channel used by UART2.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Bit 7-4 read as 0.

Index 0xF0h 0x00, N/A

Bit 0 MIDI support
0 : disable
1 : enable

Bit 1 High speed mode
0 : disable
1 : enable

Bit 2 1 : 8 Mhz clock source for UART2
0 : Normal

Bit 7-3 read as 0.

Index 0xF1h 0x02, N/A

Bit 0 IR receive polarity.
0 : active high
1 : active low

Bit 1 IR transmit polarity.
0: active high
1: active low

Bit 2 1 : Half duplex in IR
0 : Full duplex in IR.

Bit 4-3 IR mode.
00 : Normal
01 : IrDA
10 : ASK IR
11 : Normal

Bit 5, 7 read as 0.

Bit 6 IR input source.
0 : use TX2 and RX2
1 : use IRRX2 and IRTX2

Index 0xF2h 0x0C, N/A

Bit 0 Baud Rate output on RI2
0 : disable
1 : enable

Bit 1 IR half-duplex Tx-to-Rx time-out timer.
0 : disable
1 : enable

Bit 2 IR half-duplex Rx-to-Tx time-out timer
0 : disable
1 : enable

Bit 4-3 IR half-duplex time-out time control.
1x : 40-bit time for TR and RX
01 : 42-bit time for TR, 39-bit time for RX
00 : 41-bit time for TR, 39-bit time for RX.

Bit 7-5 read as 0.

LOGICAL DEVICE 6 REGISTERS (RTC)

Index 0x30h 0x00, 0x00

Bit 0 0 : Deactivate RTC (Note 4)
1 : Activate RTC.
This is a hardware setting bit by DTR1J.

Bit 7-1 read as 0.

Index 0xF0h 0x00, N/A

Bit 0 CMOS RAM 0x80-0x9F
0 : Unlock
1 : Lock

Bit 1 CMOS RAM 0xA0-0xBF.
0 : Unlock
1 : Lock

Bit 2 CMOS RAM 0xC0-0xDF
0 : Unlock
1 : Lock

Bit 3 CMOS RAM 0xE0-0xFF.
0 : Unlock
1 : Lock

Bit 6-4 read as 0.

Bit 7 1: Select upper 128-byte bank of RAM
0: Select lower bank

LOGICAL DEVICE 7 REGISTERS (KEYBOARD)

Index 0x30h 0x00, 0x00

Bit 0 Keyboard controller. This is a hardware setting bit by RTS2J. (Note 4)
0 : disable
1 : enable

Bit 7-1 read as 0.

Index 0x70h 0x01, 0x01

Bit 3-0 Select IRQ channel used by Keyboard.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Bit 7-4 read as 0.

Index 0x72h 0x00, 0x00

Bit 3-0 Select IRQ channel used by PS/2 Mouse.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Bit 7-4 read as 0.

Index 0xF0h 0x00, 0x00

Bit 0 0 : KBC clock source is 8Mhz
1 : KBC clock source is 7.16Mhz.

Bit 1 Read only. Indicates the type of keyboard
0 : PS2.
1 : AT

Bit 7-2 read as 0.

LOGICAL DEVICE 8 REGISTERS (Common I/O)

Index 0x30h 0x00, 0x00

Bit 0 Common I/O port.
0 : disable
1 : enable

Bit 7-1 read as 0.

Index 0xE0h 0x01, N/A
CIO10 function definition

Bit 0 1 : input
0 : output

Bit 1 Input/Output signal polarity
0 : non-inverted
1 : inverted

Bit 2 read as 0.

Bit 3 0 : Normal function.
1 : Input function as IRQIN1

Bit 7-4 IRQ mapping for IRQIN1.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Index 0xE1h 0x01, N/A
CIO11 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted
1 : inverted

Bit 2 read as 0.

Bit 3 0 : Normal function.
1 : Input function as IRQIN2

Bit 7-4 IRQ mapping for IRQIN2
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Index 0xE2h 0x01, N/A
CIO12 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity
0 : non-inverted
1 : inverted

Bit 2 read as 0.

Bit 3 0 : Normal function
1 : Input function as IRRX2

Bit 7-4 read as 0.

Index 0xE3h 0x01, N/A
CIO13 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal function.
1 : Output function as IRTX2

Index 0xE4h 0x01, N/A
CIO14 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity
0 : non-inverted.
1 : inverted

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal function.
1 : Select KBC P21 function

Index 0xE5h 0x01, N/A
CIO15 function definition.

Bit 0 0 : output.
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted
1 : inverted

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal function
1 : Select KBC P20 function

Index 0xE6h 0x01, N/A
CIO16 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal function
1 : Output function as I^2C CLK (Note2).

Index 0xE7h 0x01, N/A
CIO17 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted
1 : inverted

Bit 2, 7-4 read as 0

Bit 3 0 : Normal function.
1 : Select I^2C DAT function (Note2).

Index 0xE8 0x01, N/A
CIO20 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted

Bit 7-2 read as 0.

Index 0xE9h 0x01, N/A
CIO21 function definition.

Bit 0 0 : output.
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted

Bit 7-2 read as 0.

Index 0xEAh 0x01, N/A
CIO22 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted.

Bit 7-2 read as 0.

Index 0xEBh 0x01, N/A
CIO23 function definition.

Bit 0 0 : output
1 : input.

Bit 1 Input/Output signal polarity.
0 : non-inverted
1 : inverted.

Bit 7-2 read as 0

Index 0xECh 0x01, N/A
CIO24 function definition

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity
0 : non-inverted
1 : inverted.

Bit 7-2 read as 0.

Index 0xEDh 0x01, N/A
CIO25 function definition.

Bit 0 0 : output
1 : input.

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal function.
1 : Select KEYLOCK function

Index 0xEEh 0x00, N/A

Bit 5-0 Address line[13-8] of CS0J.

Bit 7-6 CS0J decoding range.
00 : A[3-0]=0000b
01 : A[3-0]=00xxb
10 : A[3-0]=0xxxb
11 : A[3-0]=xxxxb

Index 0xEFh 0x00, N/A

Bit 3-0 read as 0.

Bit 7-4 Address line[7-4] of CS0J.

Index 0xF5h 0x01, N/A
CIO30 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted
1 : inverted.

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal.
1 : Input function as the new KBC clock source

Index 0xF6h 0x01, N/A
CIO31 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal function.
1 : Output function as CS0J

Index 0xF7h 0x01, N/A
CIO32 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted
1 : inverted

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal function.
1 : Output function as CS1J

Index 0xF8h 0x01, N/A
CIO33 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted

Bit 7-2 read as 0.

Index 0xF9h 0x01, N/A
CIO34 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted
1 : inverted

Bit 7-2 read as 0.

Index 0xFAh 0x01, N/A
CIO35 function definition.

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity.
0 : non-inverted.
1 : inverted

Bit 7-2 read as 0

Index 0xFBh 0x01, N/A
CIO36 function definition

Bit 0 0 : output
1 : input

Bit 1 Input/Output signal polarity
0 : non-inverted
1 : inverted

Bit 7-2 read as 0

Index 0xFCh 0x01, N/A
CIO37 function definition.

Bit 0 0 : output.
1 : input

Bit 1 Input/Output signal polarity
0 : non-inverted
1 : inverted

Bit 2, 7-4 read as 0.

Bit 3 0 : Normal function
1 : enable the secondary KBC signal source.
CIO33 functions as ALT_KCLK
CIO34 functions as ALT_KDAT
CIO35 functions as ALT_MCLK
CIO36 functions as ALT_MDAT
CIO37 input functions as the switch control of the traditional and secondary KBC signal source. When CIO37 is 1, the traditional one is selected. When 0, the secondary is selected.

Index 0xFDh 0x00, N/A

Bit 5-0 Address line[13-8] of CS1J.

Bit 7-6 CS1J decoding range.
00 : A[3-0]=0000b
01 : A[3-0]=00xxb
10 : A[3-0]=0xxxb
11 : A[3-0]=xxxxb

Index 0xFEh 0x00, N/A

Bit 3-0 read as 0.

Bit 7-4 Address line[7-4] of CS1J.

Index 0xFFh 0x00, N/A

Bit 0 CS0J assertion on write cycle.
0 : disable
1 : enable

Bit 1 CS0J assertion on read cycle.
0 : disable
1 : enable

Bit 2 CS1J assertion on write cycle.
0 : disable
1 : enable

Bit 3 CS1J assertion on read cycle.
0 : disable
1 : enable

Note 1 : IRQ8 is reserved for use by RTC only.

Note 2 : The access port address of the I^2C device is determined by CS0J. The signals on XSD[0] and XSD[1] will reflect on I^2C_CLK and I^2C_DAT individually.

Note 3 : During direct powerdown, access to I/O ports are denied. To wake up the device, setting 1 to corresponding bit is required.

Note 4 : The disable function of the device has the same behavior as direct powerdown function except the device remains at reset state.

Table 3-2 M512x Hardware Setting Configuration

Pin Name	Function
RTS1J 0 1	CFG_PORT 0x3F0 0x370
RTS2J 0 1	KBC_EN disable enable
DTR1J 0 1	RTC_EN disable enable
DTR2J 0 1	PS2_ATJ (KBC) AT mode PS2 mode

Table 3-3 Drive Option 1 and 2

Data Rate	Register Settings (3F7)		FDC 0xF4[4:3]*		Densel	Drate	
KB/sec	Drate Sel 1	Drate Sel 0	Drate Opt1	Drate Opt0	(1)	Drate1	Drate0
1000	1	1	0	0	1	1	1
500	0	0	0	0	1	0	0
300	0	1	0	0	0	0	1
250	1	0	0	0	0	1	0
1000	1	1	0	1	1	1	1
500	0	0	0	1	1	1	0
500	0	1	0	1	0	0	1
250	1	0	0	1	0	0	0

Note : *Drive Table 00 = Regular drives and 2.88MB
01 = 3-mode drive

Table 3-4 Drvden Output Mapping for Drive Type Table

0xF4 [1:0]		Drvden Signal Definition	
DT1	**DT0**	**DRVDEN1**	**DRVDEN0**
0	0	DRATE0	DENSEL
1	0	DRATE0	DRATE1
0	1	DRATE0	nDENSEL
1	1	DRATE1	DRATE0

3.2 Power Management Features

The M512x contains power management features that makes it ideal for design of notebook and desktop personal computers. These features can be classified into power management of the part and the internal oscillator. The powerdown of the part is done independently of the internal oscillator in the M512x.

3.2.1 Oscillator Power Management

The M512x supports a built-in crystal oscillator that can be programmed to be either powered down or active, independent of the power state of the chip. This capability is implemented by the OSC-OFF bit in the 0x22. When OSC-OFF is set high, the internal oscillator is off.

When the external oscillator is used, power can be saved by turning off the internal oscillator. If the internal oscillator is used, the oscillator may be powered up (even when the rest of the chip is powered off) allowing the chip to wake up quickly and be in a stable state. It is recommended to keep the internal oscillator on even at the powerdown state. The main reason for this is that the recovery time of the oscillator during wake-up may take tens of milli-seconds under the worst case, which may create problems with any sensitive application software. In a typical application, the internal oscillator should be on unless the system goes into a power saving or standby mode. Such a mode request would be made by a system time-out or by a user. In this case, the system software would take over and must turn on the oscillator sufficiently ahead of awakening the part.

In the case of the external oscillators, the power-up characteristics are similar. If the external source remains active during the time the M512x is powered down, then the recovery time effect is minimized.

3.2.2 Part Power Management

This section deals with the power management of the rest of the chip excluding the oscillator. This part shows how powerdown modes and wake up modes are activated.

3.2.2.1 Powerdown Modes of FDC

The rest of the chip is powered down in two ways: direct powerdown and automatic powerdown. Direct powerdown results in immediate shutdown of the part without regard to the current state of the part. Automatic powerdown results when certain conditions become true within the part.

A. Direct Powerdown

Direct powerdown is conducted via the powerdown bit in the DSR register (bit 6) or FDC_PWD bit in 0X22. Programming this bit high will powerdown M512x after the part is internally reset. All current status is lost if this type of powerdown mode is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown will override the automatic powerdown. If the part is in automatic powerdown when the DSR powerdown is issued, then all the previous status of the part will be lost, and the M512x will be reset to its default values.

B. Auto Powerdown

Automatic powerdown is conducted via a "Set Powerdown Mode" command. There are four conditions required before the part will enter powerdown. All these conditions must be true for the part to initiate the powerdown sequence. These conditions are listed as follows:

1. The motor enable pins ME[0:3] must be inactive,
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt),
3. The head unload timer must have expired, and
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the AUTOPD bit in the command to high. The command also provides a capability of programming a minimum power-up time via the MIN DLY bit in the command. The minimum power-up time refers to a minimum amount of time the part will remain powered-up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down provided all the remaining conditions are met. Any software reset will reinitialize the timer. Changing of data rate extends the auto powerdown timer by up to 10 ms, but only if the data rate is changed during the countdown.

Disabling the auto powerdown mode cancels the timers and holds the M512x out of auto powerdown.

3.2.2.2 Powerdown Mode of UART and Printer

UART1, UART2 and printer can enter direct powerdown or auto powerdown respectively by setting their relative powerdown bit in the 0X22 and 0x23.

3.2.2.3 WAKE UP MODES of FDC

This section describes the conditions for awakening the part from both direct and automatic powerdown. Power conservation of battery life is the main reason power management is required. This means that the M512x must be kept in powerdown state as long as possible and should be powered up as late as possible without compromising software transparency.

To keep the part in powerdown mode as late as possible implies that the part should wake-up as fast as possible. However, some amount of time is required for the part to exit powerdown state and prepare the internal microcontroller to accept commands. Application software is very sensitive to such a delay and in order to maintain software transparency, the recovery time of the wake-up process must be carefully controlled by the system software.

A. Wake Up from DSR Powerdown

If the M512x enters powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will serve, although DSR is recommended. No other register access will wake up the part, including writing to the DOR's motor enable (ME[0:3]) bits.

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.

After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command is not blocking it. Finally, after a delay, the polling interrupt will be issued.

B. Wake Up from Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used, then the part goes through the normal reset sequence. If the access is through the selected registers, then the M512x resumes operation as though it was never in powerdown. Besides activating the RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake-up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not wake-up the part)
2. A read from the MSR register
3. A read or write to the FIFO register

Any of these actions will wake-up the part. Once awake, M512x will initiate the auto powerdown time for 10 ms or 0.5 sec. (Depending on the MIN DLY bit the auto powerdown command). The part will powerdown again when all the powerdown conditions stated in the *Auto Powerdown* section are satisfied.

Section 4 : Floppy Disk Controller

4.1 Register Overview

The integrated FDC of the M512x part is register- and hardware-level compatible with the industry standard 765A and 82077SL standards. Table 4-1 lists the I/O address map of the FDC controller. Table 4-2 is the summary of FDC register hardware reset.

Table 4-1 FDC Controller I/O Address Map

A2	A1	A0	R/W	Register
0	0	0	R	SRA (PS/2 mode only)
0	0	1	R	SRB (PS/2 mode only)
0	1	0	R/W	Digital Output Register DOR
0	1	1	R/W	Tape Drive Register TDR
1	0	0	R	Main Status Register MSR
1	0	0	W	Data Rate Select Register DSR
1	0	1	R/W	Data (First In First Out) FIFO
1	1	0	-	reserved
1	1	1	R	Digital Input Register DIR
1	1	1	W	Configuration Control Register CCR

* When this location is accessed, only bit 7 is driving, all other bits are held tristate.

Table 4-2 Summary of FDC Register Hardware Reset and Powerdown State

Register	Bits State	7	6	5	4	3	2	1	0	I/O Address Map
DOR(R/W)	H/W Reset State	0	0	0	0	0	0	0	0	3F2
TDR(R/W)	H/W Reset State	_	_	_	_	_	_	0	0	3F3
MSR(R)	H/W Reset State	0	X	X	X	X	X	X	X	3F4
DSR(W)	H/W Reset State	0	0	0	0	0	0	1	0	3F4
DIR(R)	H/W Reset State	na	_	_	_	_	_	_	_	3F7
CCR(W)	H/W Reset State	_	_	_	_	_	_	1	0	3F7
SRA(R)	H/W Reset State	0	na	0	na	0	na	na	0	3F0
SRB(R)	H/W Reset State	1	1	0	0	0	0	0	0	3F1

4.2 Register Description

This section describes the register bits for all the registers that are directly accessible to the CPU.

4.2.1 Status Register A (SRA)

Address 3F0 Read only

This register is read-only and monitors the state of the IRQ6 pin and several disk interface pins in PS/2 modes. The SRA can be accessed any time when it is in PS/2 mode. In AT mode, the data bus pins D0-D7 are held in a high impedance state for a read of address 3F0h.

PS/2 mode

Bit	**Name**
7	Int Pending
6	DRV2J
5	STEP
4	TRK0J
3	HDSEL
2	INDXJ
1	WPJ
0	DIR

Bit 7 **Interrupt Pending** : The state of the Floppy Disk Interrupt output (active high).

Bit 6 **DRV2J** : DRV2 disk interface input pin, indicates that a second drive has been installed.

Bit 5 **Step** : Step output disk interface output pin (active high)

Bit 4 **Track 0** : TRK0 disk interface input (active low)

Bit 3 **Head Select** : HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

Bit 2 **Index** : Index disk interface input (active low)

Bit 1 **Write Protect** : Write protect disk interface input. A logic "0" indicates that the disk is write protected.

Bit 0 **Direction** : Head movement direction (active high). A logic "1" indicates inward direction a logic "0" outward.

4.2.2 Status Register B (SRB)

Address 3F1 Read only

This register is read-only and monitors the state of several disk interface pins, in PS/2 modes. The SRB can be accessed at any time during PS/2 mode. In AT mode, the data bus pins D0-D7 are held in a high impedance state for a read of address 3F1h.

PS/2 mode

Bit	**Name**
7	1
6	1
5	Drive Sel0
4	Wdata Toggle
3	Rdata Toggle
2	Wgate
1	MOTEN1
0	MOTEN0

Bit 7 **Reserved** : Always read as a logic "1"

Bit 6 **Reserved** : Always read as a logic "1"

Bit 5 **Drive Select 0** : Reflects the status of the Drive Select bit 0 of DOR (address 3F2 bit 0). This bit is cleared after a hardware reset, it is unaffected by a software reset

Bit 4 **Write Data Toggle** : This bit changes

Bit 3 **Read Data Toggle** : Every inactive edge of the RDATA input causes this bit to change state.
state at every inactive edge of the WDATA

Bit 2 **Write Gate** : The WGATE disk interface output (active high)

Bit 1 **Motor Enable 1** : The MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

Bit 0 **Motor Enable 0** : The MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

4.2.3 Digital Output Register (R/W)

Address 3F2 R/W

Table 4-3 Digital Output Register Description

Bit	Description
D7	**Motor Enable 3:** This controls the Motor for drive 3, MTR3. The output is high when it is inactive, and low when it is active. This bit and DOR bit 6 provide information that control the MTR1 and 0 pins, respectively when bit 7 of the configuration register is set.
D6	**Motor Enable 2:** Same function as D7 except for drive 2's motor. Note that this signal is not brought out to a pin.
D5	**Motor Enable 1:** This bit controls the Motor for drive 1's motor. When this bit is 0, the MTR1 output is high.
D4	**Motor Enable 0:** Same as D5 except for drive 0's motor.
D3	**DMA Enable:** When set to a 1, this enables the DRQ, DAK, and INT pins. A zero disables these signals.
D2	**Reset Controller:** This bit resets the controller when 0 and enables normal operation when it is a 1. It does not affect the drive control or data rate registers which are reset only by a hardware reset.
D1~D0	**Drive Select:** These two pins are encoded for the four drive select, and are gated with the motor enable lines, so that only one drive is selected when its motor enable is active.

Table 4-4 Internal 4 Drive Decode - Normal

Digital Output Register						Drive Select Outputs		Motor on Outputs	
D7	D6	D5	D4	D1	D0	DS1J	DS0J	MTR1J	MTR0J
x	x	x	1	0	0	1	0	/D5	/D4
x	x	1	x	0	1	0	1	/D5	/D4
x	1	x	x	1	0	1	1	/D5	/D4
1	x	x	x	1	1	1	1	/D5	/D4
0	0	0	0	x	x	1	1	/D5	/D4

Table 4-5 Internal 4 Drive Decode - Drives 0 and 1 Swapped

Digital Output Register						Drive Select Outputs		Motor on Outputs	
D7	D6	D5	D4	D1	D0	DS1J	DS0J	MTR1J	MTR0J
x	x	x	1	0	0	0	1	/D4	/D5
x	x	1	x	0	1	1	0	/D4	/D5
x	1	x	x	1	0	1	1	/D4	/D5
1	x	x	x	1	1	1	1	/D4	/D5
0	0	0	0	x	x	1	1	/D4	/D5

4.2.4 Tape Drive Register (TDR)

Address 3F3 R/W

This register is included for 82077 software compatibility. The robust data separator used in the M512x does not require its characteristics modified for tape support. The contents of this register are not used internally to the device. The TDR is unaffected by a software reset. Bits 2-7 are tri-stated when read in this mode.

Normal Floppy mode

Normal mode. Register 3F3h contains only bits 0 and 1. When this register is read, bits 2- 7 are at high impedance.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tapesel1	tapesel0

Enhanced Floppy mode 2 (OS2)

Register 3F3 for Enhanced Floppy mode 2 operation

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Media ID1	Media ID0	Drive type ID		Floppy boot drive		tapesel1	tapesel0

For this mode, DRATE0 and DRATE1 pins are inputs and these inputs are gated into bits 6 and 7 of the 3F3 register. These two bits are not affected by any reset.

Bit 7 **Media ID 1** Read only (pin 19) see table next page

Bit 6 **Media ID 0** Read only (pin 20) see table next page

Bits 5 and 4 **Drive Type ID** - These bits reflect two of FDC 0XF2 configuration register bits. (please see next page).

Bits 3 and 2 **Floppy boot Drive**. These bits show the value of FDC 0xF1 configuration register bits.

Bits 1 and 0 - **Tape Drive select** (R/W). Same as in Normal and Enhanced Floppy mode 1.

Media ID1

Drate1	Media ID1	
pin 19	FDC 0xF1-db5=0	FDC 0xF1--db5=1
0	0	1
1	1	0

Media ID0

Drate0	Media ID0	
pin 20	FDC 0xF1-db4=0	FDC 0xF1-db4=1
0	0	1
1	1	0

Drive type ID

Digital Output Register		Register 3F3 - drive type ID	
bit 1	bit 0	bit 5	bit 4
0	0	FDC 0xF2 - bit 1	FDC 0xF2 - bit 0
0	1	FDC 0xF2 - bit 3	FDC 0xF2 - bit 2
1	0	FDC 0xF2 - bit 5	FDC 0xF2 - bit 4
1	1	FDC 0xF2 - bit 7	FDC 0xF2 - bit 6

4.2.5 Main Status Register

Address 3F4h Read only

The read-only main status register indicates the current status of the disk controller. It is always available to be read. One of its functions is to control the flow of data to and from the data register. It also indicates when the disk controller is ready to send or receive data. It should be read before each byte is transferred to or from the data register except during a DMA transfer. No delay is required when reading this register after a data transfer.

Table 4-8 Main Status Register Description

Bit	Description
D7	**Request for Master:** Indicates that the data register is ready to send or receive data from the CPU. This bit is cleared immediately after a byte transfer, and is set again as soon as the M512x is ready for the next byte.
D6	**Data Direction:** Indicates whether the controller is expecting a byte to be written to (0) or read from (1) the data register.
D5	**Non-DMA Execution:** Bit is set only during the execution phase of a command if it is in the non-DMA mode. In other words, if this bit is set, the multiple byte data transfer (in the execution phase) must be monitored by the CPU either through interrupts, or software polling as described in the processor software interface section.
D4	**Command in Progress:** Bit is set after the first byte of the command phase is written. Bit is cleared after the last byte of the result phase is read. If there is no result phase in a command, the bit is cleared after the last byte of the command phase is written.
D3~D0	**Drives 3~0 Seeking:** Set after the last byte of the command phase of a seek or recalibrate command is issued for drives 3~0, respectively. Cleared after reading the first byte in the result phase of the sense interrupt command for this drive.

4.2.6 Data Rate Select Register (DSR)

Address 3F4 Write only

Table 4-9 Datarate Select Register Description

Bit	Description
D7	**S/W RESET** behaves the same as DOR RESET except that this reset is self clearing.
D6	**POWERDOWN** bit implements direct powerdown. Setting this bit high puts the FDC into the powerdown state regardless of the state of the part. The part is reset internally and then goes into powerdown. No status is saved and any operation in progress is aborted. This powerdown mode does not turn off the internal oscillator. Any hardware or software reset will exit the M512x from this powerdown state.
D5	**reserved**
D4~D2	**PRECOMP 0-2** adjusts the WRDATA output to the and disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the M512x offsets the data pattern as it is written to the disk. The amount of precompensation depends upon the drive and media but in most cases the default value is acceptable. The M512x starts precompensating the data pattern starting on Track 0. The CONFIGURE command can change the starting track for precompensation. Table 4-10 lists the precompensation values that can be selected and Table 4-11 lists the default precompensation values. The default value is selected if the three bits are zeros.
D1~D0	**DRATE 0-1** select one of the four data rates as listed in Table 4-12. The default value is 250 Kbps upon a chip ("Hardware") reset. Other ("Software") Resets do not affect the DRATE or PRECOMP bits.

Table 4-10 Precompensation Delay Values

PRECOMP 432 bits	Precompensation Delay--DISABLED
111	0.00ns
001	41.67ns
010	83.34ns
011	125.00ns
100	166.67ns
101	208.33ns
110	250.00ns
000	DEFAULT

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Table 4-11 Default Precompensation Delay Values

Data Rate	Precompensation Delay
1 Mbps	41.67ns
500 Kbps	125ns
300 Kbps	125ns
250 Kbps	125ns

Table 4-12 Data Rates

DRATESEL		Data Rate	
		MFM	FM
1	1	1 Mbps	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

4.2.7 Data Register (R/W)

Address 3F5 R/W

This is the location through which all commands, data, and status flow between the CPU and the FDC. During the command phase, the CPU loads the controller's commands into this register based on the status register request for master and data direction bits. The result phase transfers the status registers and header information to the CPU in the same fashion.

All command parameter information and disk data transfers go through the FIFO. The 16-byte FIFO has programmable threshold values. Data transfers are generated by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to an M5105 compatible mode after a "Hardware" reset (Reset via pin 1). "Software" Resets (Reset via DOR or DSR register) can also place the M512x into M5105-A3/A4-compatible mode if the LOCK bit is set to "0" This maintains PC-AT hardware compatibility.

The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk error. Table 4-13 gives several examples of the delays with a FIFO. The data is based upon the following formula:

Threshold# * 1/DATA RATE * 8 - 1.5_{us} = DELAY

Table 4-13 FIFO Service Delay

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	$1 * 8_{us} - 1.5_{us} = 6.5_{us}$
2 bytes	$2 * 8_{us} - 1.5_{us} = 14.5_{us}$
8 bytes	$8 * 8_{us} - 1.5_{us} = 62.5_{us}$
15 bytes	$15 * 8_{us} - 1.5_{us} = 118.5_{us}$
FIFO Threshold Examples	**Maximum Delay to Servicing at 500 Mbps Data Rate**
1 byte	$1 * 16_{us} - 1.5_{us} = 14.5_{us}$
2 bytes	$2 * 16_{us} - 1.5_{us} = 30.5_{us}$
8 bytes	$8 * 16_{us} - 1.5_{us} = 126.5_{us}$
15 bytes	$15 * 16_{us} - 1.5_{us} = 238.5_{us}$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the M512x enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred.
An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

4.2.8 Configuration Control Register (CCR, PC-AT Modes)

Address 3F7 Write only

Table 4-14 Configuration Control Register Description

Bit	Description
D7~D2	Not used.
D1, D0	**Data Rate Select:** These bits set the data-rate and write-precompensation values for the disk controller. After a hardware reset, these bits are set to 1, 0 (250 Kbps). (please refer to table 4-12)

4.2.9 Digital Input Register (DIR, Read)

Address 3F7 Read only

Table 4-15 Digital Input Register Description (PC/AT mode)

Bit	Description
D7	DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable, regardless of the value of /INVERT/. The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits remain tri-stated.
D6~D0	These bits are reserved for use by the hard disk controller, thus during a read of this register, these bits are in high impedance state.

Table 4-15b Digital Input Register (PS/2 mode)

Bit	Description
D7	DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable.
D6~D3	undefined, always read as logic "1".
D2~D1	Data rate select. These bits control the data rate of the floppy controller. These bits are unaffected by a software reset, and are set to 250 kbps after a hardware reset.
D0	High density. This bit is low whenever the 500 kbps or 1 Mbps data rates are selected, and high when 250 kbps and 300 kbps are selected.

4.3 Result Phase Status Registers

The result phase of a command contains bytes that hold status information. The format of these bytes are described in the following sections. Do not confuse these register bytes with the main status register which is a read-only register that is always available. The result phase status registers are read from the data register only during the result phase.

4.3.1 Status Register 0 (ST0)

Table 4-16 Status Register 0 Description

Bit	Description
D7~D6	**Interrupt Code :** 00 = Normal termination of command. 01 = Abnormal termination of command. Command was executed, but not successfully completed. 10 = Invalid command issue. Command issued was not recognized as a valid command. 11 = Ready changed state during the polling mode.
D5	**Seek End:** This bit is set after a seek or recalibrate command is completed by the controller. Used during sense interrupt command.
D4	**Equipment Check:** This bit is set after a recalibrate command track 0 signal failed to occur. Used during sense interrupt command.
D3	**Not Used:** 0
D2	**Head Number:** At end of execution phase.
D1, D0	**Drive Select:** At end of execution phase. 00 = Drive 0 selected 01 = Drive 1 selected 10 = Drive 2 selected 11 = Drive 3 selected

4.3.2 Status Register 1 (ST1)

Table 4-17 Status Register 1 Description

Bit	Description
D7	**End of Track:** This bit is set when the controller has transferred the last byte of the last sector without the TC pin becoming active. The last sector is the end-of-track sector number programmed in the command phase.
D6, D3	**Not Used:** 0
D5	**CRC Error:** If this bit is set and bit 5 of ST2 is clear, then there was a CRC error in the address field of the correct sector. If bit 5 of ST2 is set, then there was a CRC error in the data field.
D4	**Over Run:** This bit is set when the controller was not serviced by the CPU soon enough during a data transfer in the execution phase. Table 4-18 shows the time values.
D2	**No Data:** This bit is set for any three possible problems: 1. Controller cannot find the sector specified in the command phase during the execution of a read, write, or scan command. An address mark was found even if it is not a blank disk. 2. Controller cannot read any address fields without a CRC error during read ID command. 3. Controller cannot find the starting sector during execution of read a track command.
D1	**Not Writable:** Set if the write protect pin is active when a write or format command is issued.
D0	**Missing Address Mark:** If this bit is set and bit 0 of ST2 is clear then the disk controller cannot detect any address field address mark after two disk revolutions. If bit 0 of ST2 is set, then the disk controller cannot detect the data field address mark.

Table 4-18 Maximum Time Allowed to Service an Interrupt or Acknowledge a DMA Request in Execution Phase

Data Rate	Time to Service
125	62.0 us
250	30.0 us
500	14.0 us
125	6.0 us

4.3.3 Status Register 2 (ST2)

Table 4-19 Status Register 2 Description

Bit	Description
D7	**Not Used:** 0
D6	**Control Mark:** This bit is set if the controller tries to read a sector which contained a deleted data address mark during execution of read-data or scan commands. Or, if a read-deleted-data command was executed, a regular address mark is detected.
D5	**CRC Error in Data Field:** This bit is set if the controller detects a CRC error in the data field. Bit 5 of ST1 is also set.
D4	**Wrong Track:** This bit is only set if the desired sector is not found, and the track number recorded on any sector of the current track is different from that stored in the track register.
D3	**Scan Equal Hit:** This bit is only set if the equal condition is satisfied during any scan command.
D2	**Scan Not Satisfied:** This bit is set if the controller cannot find a sector on the track number recorded on any sector on the track which meets the desired condition during scan commands.
D1	**Bad Track:** This bit is only set if the desired sector is not found, and the track number recorded on any sector on the track is different from that stored in the track register and the recorded track number is FF.
D0	**Missing Address Mark in Data Field:** This bit is set if the controller cannot find the data field address mark during read/scan command. Bit 0 of ST1 is also set.

4.3.4 Status Register 3 (ST3)

Table 4-20 Status Register 3 Description

Bit	Description
D7	**Not Used:** 0
D6	**Write Protect Status:** This bit is the complement of the associated FDC interface pin for the drive selected in DCR.
D5	**Not Used:** 1
D4	**Track 0 Status:** This bit is the complement of the associated FDC interface pin for the drive selected in the DCR.
D3	**Not Used:** 0
D2	**Head Select Status:** This bit shows the status of the associated bit in the sense-drive-status command phase.
D1, D0	**Drive Selected:** These bits show the status of the associated bits in the sense-drive-status command phase. These bits show the same status as ST0 bits 1, 0. 00 = Drive 0 selected 01 = Drive 1 selected 10 = Drive 2 selected 11 = Drive 3 selected

4.4 Controller Functional Description

4.4.1 Controller Phases

The FDC handles commands in three phases–command, execution and result. Each phase is described below.

4.4.1.1 Command Phase

The CPU writes a series of bytes to the data register. These bytes indicate the command desired and the particular parameters required for the command. All the bytes must be written in the order specified in the command description table. The execution phase starts immediately after the last byte in the command phase is written.
The Main Status Register controls the flow of command bytes, and must be polled by the software before writing each Command Phase byte to the Data Register. Prior to writing a command byte, the bit 7 must be set and bit 6 must be cleared in the MSR. After the first command byte is written to the Data Register, the bit 4 in MSR is also set and remain set until the last Result Phase byte is read. If there is no Result Phase, it is cleared after the last command byte is written. A new command may be initiated after reading all the result bytes from the previous command.

4.4.1.2 Execution Phase

The disk controller performs the desired command. Some commands require the CPU to read or write data to or from the data register during this phase. Some commands such as Seek control the read/write head movement on the disk drive. Some commands does not involve any action by the uP or disk drive, and consists of an internal operation by the controller.
If there is data to be transferred between the uP and the controller, there are three methods that can be used, DMA mode, interrupt mode, and software polling mode. All of these data transfer modes work with the FIFO enabled or disabled.

4.4.1.2.1 DMA Mode

If the DMA mode is selected, a DMA request is generated in the execution phase when each byte is ready to be transferred. To enable DMA operations during the execution phase, the DMA mode bit in the Specify command must be enabled, and the DMA signals must be enabled in the Drive Control Register. The DMA controller responds to the DMA request with a DMA-acknowledge and a read- or write-strobe. The DMA request is cleared by the active edge of the DMA-acknowledge. After the last byte is transferred, an interrupt is generated, indicating the beginning of the result phase. TC is asserted to terminate an operation. Due to internal gating, TC is only recognized when the -DAK input is low.

4.4.1.2.2 Interrupt Mode

If the non-DMA mode is selected, an interrupt is generated in the execution phase when each byte is ready to be transferred. The Main Status Register should be read to verify that the interrupt is for a data transfer. Bits 5 and 7 of the Main Status Register is set. The interrupt is cleared when the byte is transferred to or from the data register. The CPU should transfer the byte within the allotted time. If the byte is not transferred within the time allotted, an overrun error is indicated in the result phase when the command terminates at the end of the current sector.

An interrupt is also generated after the last byte is transferred. This indicates the beginning of the Result Phase.

4.4.1.2.3 Software Polling

If the non-DMA mode is selected and interrupts are not suitable, the CPU can poll the Main Status Register during the execution phase to determine when a byte is ready to be transferred. The bit 7 of the Main Status Register reflects the state of the interrupt pin. Otherwise, the data transfer is similar to the interrupt mode described above.

4.4.1.3 Result Phase

During the Result Phase, the uP reads a series of bytes from the data register. These bytes indicate the status of the command. This status may indicate whether the command executed properly, or contain some control information. The bit 7 and bit 6 in the MSR must both be set before each result byte can be read. After the last result byte is read, the bit 4 in the MSR is cleared, and the controller is ready for the next command.

Table 4-21 M512x FDC Command Set

READ DATA

Command Phase

MT	MFM	SK	0	0	1	1	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ DELETED DATA

Command Phase

MT	MFM	SK	0	1	1	0	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ A TRACK

Command Phase

0	MFM	0	0	0	0	1	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ ID

Command Phase

0	MFM	0	0	1	0	1	0
0	0	0	0	0	HD	DR1	DR0

Execution Phase: Controller reads first ID Field header bytes it can find and reports these bytes to the system in the result bytes

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

WRITE DATA

Command Phase

MT	MFM	0	0	0	1	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

WRITE DELETED DATA

Command Phase

MT	MFM	0	0	1	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

FORMAT A TRACK

Command Phase

0	MFM	0	0	1	1	0	1
0	0	0	0	0	HD	DR1	DR0
Bytes per Sector							
Sector per Track							
Format Gap							
Data Pattern							

Execution Phase: System transfers four ID bytes per sector to the floppy controller via DMA or Non-DMA modes. The entire track is formatted. The data block in the Data Field of each sector is filled with the data pattern byte

Result Phase

Status Register 0
Status Register 1
Status Register 2
Undefined
Undefined
Undefined
Undefined

SCAN EQUAL

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SCAN HIGH OR EQUAL

Command Phase

MT	MFM	SK	1	1	1	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SCAN LOW OR EQUAL

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

VERIFY

Command Phase

MT	MFM	SK	1	0	1	1	0
0	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is read from disk but not transferred to the system.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

DUMPREG

Command Phase

0	0	0	0	1	1	1	0

Execution Phase: Internal registers read

Result Phase

Present Track Number on Drive 0							
Present Track Number on Drive 1							
Present Track Number on Drive 2							
Present Track Number on Drive 3							
Step Rate Time				Motor Off Time			
Motor On Time							DMA
Sector per Track/End of Track							
LOCK	0	D3	D2	D1	D0	GAP	WG
0	EIS	FIFO	POLL	FIFOTHR			
PRETRK							

PERPENDICULAR MODE

Command Phase

0	0	0	1	0	0	1	0
OW	0	D3	D2	D1	D0	GAP	WG

Execution Phase: Internal registers are written.

No Result Phase.

CONFIGURE

Command Phase

0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0
0	EIS	FIFO	POLL	FIFOTHR			
PRETRK							

Execution Phase: Internal registers are written.

No Result Phase

RECALIBRATE

Command Phase

0	0	0	0	0	1	1	1
0	0	0	0	0	0	DR1	DR0

Execution Phase: Disk drive head is stepped out to Track 0.

No Result Phase

RELATIVE SEEK

Command Phase

1	DIR	0	0	1	1	1	1
0	0	0	0	0	HD	DR1	DR0
Relative Track Number							

Execution Phase: Disk drive head stepped in or out a programmable number of tracks.

No Result Phase

SEEK

Command Phase

0	0	0	0	1	1	1	1
0	0	0	0	0	HD	DR1	DR0
New Track Number							

Execution Phase: Disk drive head is stepped in or out to a desired track.

No Result Phase

SENSE DRIVE STATUS

Command Phase

0	0	0	0	0	1	0	0
0	0	0	0	0	HD	DR1	DR0

Execution Phase: Disk drive status information is detected and reported.

Result Phase

Status Register 3

SENSE INTERRUPT

Command Phase

0	0	0	0	1	0	0	0

Execution Phase: Status of interrupt is reported

Result Phase

Status Register 0
Present Track Number

SPECIFY

Command Phase

0	0	0	0	0	0	1	1
Step Rate Time				Motor Off Time			
Motor On Time							DMA

Execution Phase: Internal registers are written.

No Result Phase

POWERDOWN MODE

Command Phase

0	0	0	1	0	1	1	1
0	0	0	0	0	0	DLY	APD

Execution Phase: Internal registers are written

Result Phase

0	0	0	0	0	0	DLY	APD

VERSION

Command Phase

0	0	0	1	0	0	0	0

Result Phase

1	0	0	1	0	0	0	0

LOCK

Command Phase

LOCK	0	0	1	0	1	0	0

Execution Phase: Internal registers are written.

Result Phase

0	0	0	LOCK	0	0	0	0

INVALID

Command Phase

Invalid Codes

Result Phase

Status Register 0 (80H)

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4.6 Command Description

4.6.1 Read Data

The read data op-code is written to the data register followed by 8 bytes as specified in the command description table. After the last byte is written, the controller starts looking for the correct sector header. Once the controller is found, the controller sends data to the CPU. After one sector is finished, the sector number is incremented by one and this new sector is searched for. If MT (multi-track) is set, both sides of one track can be read. Starting on side zero, the sectors are read until the sector number specified by end of track sector number is reached. Then, side one is read by starting with sector number one.

In DMA mode, the read-data command continues to read until the TC pin is set. This means that the DMA controller should be programmed to transfer the correct number of bytes. TC should be controlled by the CPU and be asserted when enough bytes are received. An alternative to these methods of stopping the read-data command is to program the end of track sector number as the last sector number that to be read. The controller stops reading the disk with an error message indicating that it tried to access a sector number beyond the end of the track.

The number of data bytes per sector parameter is defined in Table 4-27. If this is set to zero, the data length parameter defines the number of bytes that the controller transfers to the CPU. If the data length specified is smaller than 128, the controller still reads the entire 128 byte sector and checks the CRC, though only the number of bytes specified by the data length parameter are transferred to the CPU. Data length parameter should not be set to zero. If the number of bytes per sector parameter is not zero, the data length parameter has no meaning and should be set to FFh.

Table 4-27 Sector Size Selection

Bytes/Sector Code	Number of Bytes in Data Field
0	128
1	256
2	512
3	1024
4	2048
5	4096
6	8192

If the implied seek mode is enabled by both the mode command and the IPS bit in this command, a seek is performed to the track number specified in the command phase. The controller also waits for the head-settle-time if the implied seek is enabled. After all these conditions are met, the controller searches for the specified sector by comparing the track number, head number, sector number, and number of bytes/sector given in the command phase with the appropriate bytes read off the disk in the address fields.

If the correct sector is found, but there is a CRC error in the address field, bit 5 of ST1 (CRC error) is set and an abnormal termination is indicated. If the correct sector is not found, bit 2 of ST1 (no data) is set and an abnormal termination is indicated. In addition to this, if any address field track number is FF, bit 1 of ST2 (bad track) is set or, if any address field track number is different from that specified in the command phase, bit 4 of ST2 (wrong track) is set.

After finding the correct sector, the controller reads that data field. If a deleted data mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (control mark) is set, and the next sector is searched for. If a deleted data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (control mark) is set, and the read terminates with a normal termination. If a CRC error is detected in the data field, bit 5 is set to both ST1 and ST2 (CRC error) and an abnormal termination is indicated.

If no problems occur in the read command, the read continues from one sector to the next in logical order (not physical order) until either TC is set or an error occurs. If a disk has not been inserted into the disk drive, there are many opportunities for the controller to hang. It does this if it is waiting for a certain number of disk revolutions. If this occurs, the controller can be forced to abort the command by writing a byte to the data register.

An interrupt is generated when an execution phase of the read data command terminates. Table 4-28 shows the values that are read back in the result phase. If an error occurs, the result bytes indicate the sector being read when the error occurred.

Table 4-24 Result Phase Termination Values with No Error

Last	ID Information at Result Phase					
MT	**HD**	**Sector**	**Track**	**Head**	**Sector**	**B/S**
0	0	< EOT	NC	NC	S + 1	NC
0	0	= EOT	T + 1	NC	1	NC
0	1	< EOT	NC	NC	S + 1	NC
0	1	= EOT	T + 1	NC	1	NC
1	0	< EOT	NC	NC	S + 1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S + 1	NC
1	1	= EOT	T + 1	0	1	NC

EOT = End of track sector number from command phase NC = No change in value
S = Sector number last operated on by controller T = Track number programmed in command phase

4.6.2 Read-Deleted-Data

This command is the same as the read-data command except for how it handles a deleted data mark. If a deleted data mark is read, the sector is read normally. If a regular data mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (control mark) is set, and the next sector is searched for. If a regular data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (control mark) is set, and the read terminates with a normal termination.

4.6.3 Write-Data

The write-data command is very similar to the read-data command except that data is transferred from the CPU to the disk rather than the other way around. If the controller detects the write-protect signal, bit 1 of ST1 (not writable) is set and an abnormal termination is indicated.

4.6.4 Write-Deleted-Data

This command is the same as the write-data command except that a deleted-data mark is written at the beginning of the data field instead of the normal data mark.

4.6.5 Read a Track

This command is similar to the read-data command except for the following: the controller starts at the index hole and reads the sectors in their physical order, not their logical order.

Even though the controller reads sectors in their physical order, it still compares the header ID bytes with the data programmed in the command phase. The exception to this is the sector number. Internally, this is set to one, then incremented for each successive sector read. Whether or not the programmed address field matches that read from the disk, the sectors are still read in their physical order. If a header ID comparison fails, bit 2 of ST1 (No data) is set, but the operation continues. If there is a CRC error in the address or data field, the read also continues. The command terminates when it has read the number of sectors programmed in the EOT parameter.

4.6.6 Read ID

This command causes the controller to read the first address field it finds. The result phase contains the header bytes that are read. There is no data transfer during the execution phase of this command. An interrupt is generated when the execution phase is completed.

4.6.7 Format-a-Track

This command formats one track on the disk. After the index hole is detected, data patterns are written on the disk including all gaps, address marks, address fields, and data fields. The exact details of the number of bytes for each field is controlled by the parameters given in the format-a-track command, and the IAF (Index Address Field) bit in the mode command. The data field consists of the fill-byte specified in the command, repeated to fill the entire sector. To allow for floppy formatting, the CPU must supply the four address field bytes (track, head, sector, number of bytes) for each sector formatted during the execution phase. In other words, as the controller formats each sector, it requests four bytes through either DMA requests or interrupts. This allows for non-sequential sector interleaving. Table 4-29 shows some typical values for the programmable gap size.

The format command terminates when the index hole is detected a second time, at which point an interrupt is generated. Only the first three status bytes in the result phase are significant.

Table 4-25A Gap Length for Various Sector Sizes and Disk Types

Mode	Sector Size (Dec)	Sector Code (Dec)	EOT (Hex)	Sector Gap (Hex)	Format* Gap (Hex)
8-inch Drives (360 RPM, 500 kb/s)					
FM	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM	256	01	0F	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5.25-inch Drives (300 RPM, 250 kb/s)					
FM	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3.5-inch Drives (300 RPM, 250 kb/s)					
FM	128	00	0F	07	1B
	256	01	09	0E	2A
	512	02	05	1B	3A
MFM	256	01	0F	0E	36
	512	02	09	1B	54
	1024	03	05	35	74

Table 4-25B Format Table for PC-Compatible Diskette Media

Media Type	Sector Size (Dec)	Sector Code (Hex)	EOT (Hex)	Sector Gap (Hex)	Format* Gap (Hex)
360 K	512	02	09	2A	50
1.2 M	512	02	0F	1B	54
720 M	512	02	09	1B	50
1.44 M	512	02	12	1B	6C
2.88 M	512	02	24	1b	54

* Format gap is the gap length used only for the format command.

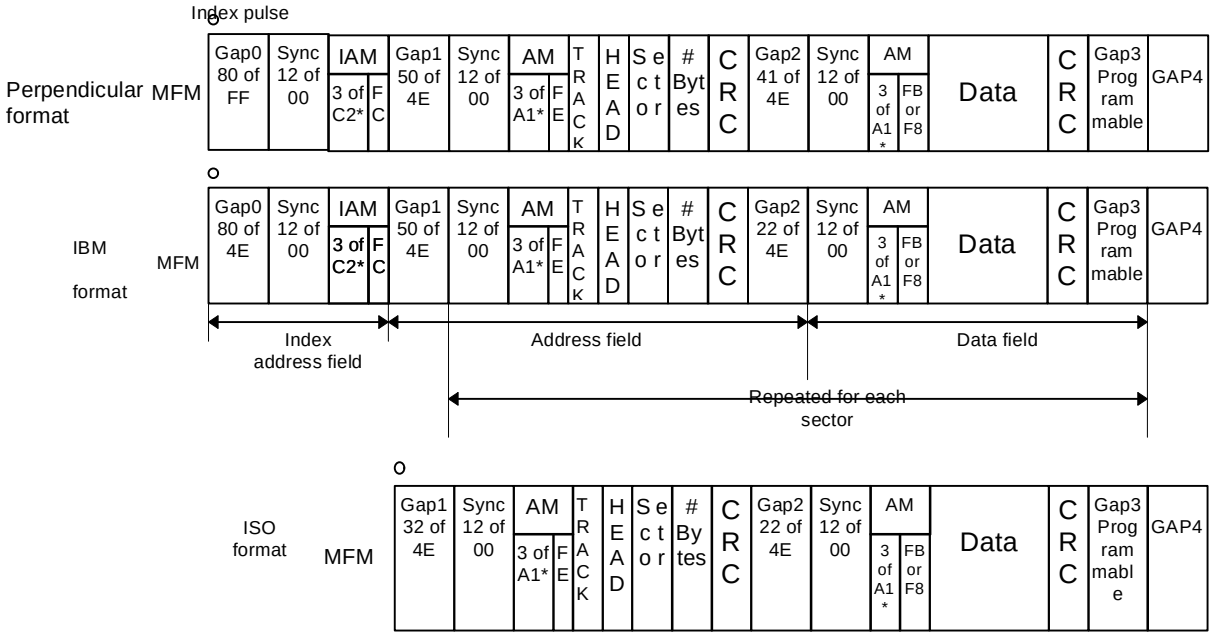


Figure 4-4 IBM, Perpendicular, and ISO Formats Supported by the Format Command

4.6.8 Scan Commands

The scan commands allow data read from the disk to be compared against data sent from the CPU. There are three scan commands to choose from:

Scan equal	Disk data = CPU data
Scan less than or equal	Disk data ≤ CPU data
Scan greater than or equal	Disk data ≥ CPU data

Each sector is interpreted with the most significant byte first. If the wildcard mode is enabled from the mode command, an FFh from either the disk or CPU is used as a "don't care" byte that always matches equal. If each sector is read, the desired condition has not been met, and the next sector is read. The next sector is defined as the current sector number plus the sector step-size specified.

The scan command continues until the scan condition has been met, or the end of track sector number has been reached, or if TC is asserted. If the SK bit is set, sectors with deleted data marks are ignored. If all sectors read are skipped, the command terminates with D3 of ST2 set (scan equal hit). Table 4-30 shows the result phase of the command.

Table 4-30 Scan Command Termination Values

Status Register Command	D2	D3	Conditions
Scan equal	0	1	Disk = CPU
	1	0	Disk <> CPU
Scan low or equal	0	1	Disk = CPU
	0	0	Disk < CPU
	1	0	Disk > CPU
Scan high or equal	0	1	Disk = CPU
	0	0	Disk < CPU
	1	0	Disk > CPU

4.6.9 Seek

There are two ways to move the disk drive head to the desired track number. The first method is to enable the implied seek mode. This way, each individual read or write command automatically moves the head to the track specified in the command.

The second method is by using the seek command. During the execution phase of the seek command, the track number to seek for is compared with the present track number, and a step pulse is produced to move the head one track closer to the desired track number. This is repeated at the rate specified by the specify command until the head reaches the correct track. At this point, an interrupt is generated and a sense-interrupt command is required to clear the interrupt.

During the execution phase of the seek command, the only indication via software that a seek command is in progress is bits 0~3 (drive busy) of the main status register. Bit 4 of the main status register (command in progress) is not set. While the internal micro-engine is capable of multiple seeks on two or more drives at the same time since the drives are selected via the drive-control register in software, software should ensure that only one drive performs the seek command at one time. No other command except the sense-interrupt command is issued while a seek command is in progress.

If the extended track range mode is enabled, write a fourth byte in the command phase to indicate the four most significant bits of the desired track number. Otherwise, write only three bytes.

4.6.10 Relative Seek

The Relative Seek command steps the selected drive in or out a given number of steps. This command will step the read/write head an incremental number of tracks from the current track number, contrasting to step it to the desired track number as Seek command. The Relative Seek parameters are defined as follows:

DIR: Read/Write Head Step Direction Control
0=Step Head Out, 1=Step Head In

RTN: Relative Track Number. This value will determine how many incremental tracks to step the head in or out from the current track number.

4.6.11 Recalibrate

The recalibrate command is very similar to the seek command. It is used to step a drive head out to track zero. Step pulses are produced until the track zero signal from the drive becomes true. If the track zero signal does not go before 77 step pulses are issued, an error is generated. If the extended track range mode is enabled, an error is not generated until 3,917 pulses are issued.

Recalibrations on more than one drive at a time should not be issued for the same reason as explained in the seek command. No other command except the sense-interrupt command should be issued while a recalibrate command is in progress.

4.6.12 Sense-Interrupt Status

An interrupt is generated by the controller when any of the following conditions occur:

1. Upon entering the result phase of:
   a. Read-data command
   b. Read-deleted-data command
   c. Write-data command
   d. Write-deleted-data command
   e. Read-a-track command
   f. Read-ID command
   g. Format command
   h. Scan commands

2. During data transfers in the execution phase while in the non-DMA mode

3. Internal ready signal changes state (only occurs immediately after a hardware or software reset).

4. Seek or recalibrate command termination

An interrupt generated for reasons 1 and 2 above occurs during normal command operations and are easily recognized by the CPU. During an execution phase in non-DMA mode, bit 5 (execution mode) in the MSR is set to 1. Upon entering result phase, this bit is set to 0.

Reasons 1 and 2 do not require the sense interrupt status command. The interrupt is cleared by reading or writing information to the data register. Interrupts caused by reasons 3 and 4 are identified with the aid of the sense interrupt status command. This command resets the interrupt when the command byte is written.

Table 4-31 shows how to identify the cause of the interrupt by using bits 5, 6 and 7 of ST0.

Issuing a sense-interrupt status command without an interrupt pending is treated as an invalid command. If the extended track range mode is enabled, a third byte should be read in the result phase which indicates the four most significant bits of the present track number. Otherwise, only two bytes should be read.

4.6.13 Specify

The specify command sets the initial values for each of the three internal timers. Table 4-32 shows the timer programming values.

The head-load and head-unload timers are artifacts of the UPD765A. These timers determine the delay from loading the head until a read or write command is started, and unloading the head sometime after the command was completed. Since the M512x head-load signal is now the software-controlled motor lines in the drive-control register, these timers only provide some delay from the initialization of a command until it is actually started. Similar to the DP8474, extend these timers setting the TMR bit in the mode command.

The step-rate time defines the time interval between adjacent step pulses during a seek, implied-seek, or recalibrate command. The times stated in Table 4-32 are affected by the data rate. These values are for 500 kb/s MFM (250 Kb/s FM) and 1 Mb/s MFM (500 Kb/s FM). For 300 kb/s MFM data rate (150 Kb/s FM), these values, multiply by 1.6667, and for 250 Kb/s MFM (125 Kb/s FM) double these values.

The choice of DMA or non-DMA operation is made by the non-DMA bit. When this bit is 1, the non-DMA mode is selected, and when this bit is 0, DMA mode is selected. This command does not generate an interrupt.

Table 4-31 Status Register 0 Termination Codes

Interrupt Code D7	D6	D5	Seek End Cause
1	1	0	Internal ready went true
0	0	1	Normal seek termination
0	1	1	Abnormal seek termination

Table 4-32 Step, Head, Load and Unload Timer Definitions (500 kb/s MFM)

Timer	Mode 1 Value	Range	Mode 2 Value	Range	Unit
Step Rate	(16 - N)	1~16	(16 - N)	1~16	ms
Head Unload	N x 16	0~240	N x 512	0~7680	ms
Head Load	N x 2	0~254	N x 32	0~4064	ms

4.6.14 Sense Drive Status

This two-byte command obtains the status of a disk drive. Status register 3 is returned in the result phase and contains the drive status. This command does not generate an interrupt.

4.6.15 Verify

The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously stored value.

4.6.16 Version

The Version command can be used to determine the floppy controller being used. The result phase uniquely identifies the floppy controller version. The FDC returns a value of 90h in order to be compatible with the 82077. For older version compatible with NEC765 controller, a value of 80h (invalid command) will return.

4.6.17 Dumpreg

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. The command returns important information regarding the status of many of the programmed field in the FDC. This can be used to verify the values initialized in the FDC.

4.6.18 Configure

The Configure command controls some operation modes of the controller. It should be issued during the initialization of the FDC after power up. These bits are set to their default values after a hardware reset.
EIS: Enable implied seek. When EIS=1, the FDC will perform a SEEK operation before executing a read/write command. The default value is 0 (no implied seek).

EFIFO: Enable FIFO. When EFIFO=1, the FIFO is disabled (NEC765A compatible mode). This means data is transferred on a byte by byte basis. The default value is 1 (FIFO disable).
POLL: Disable Polling. When POLL=1, polling of the drives is disabled. POLL defaults to 0 (polling enable). When enabled, a single interrupt is generated after reset.
FIFOTHR: The FIFO threshold in the execution phase of a read/write command. This is programmable from 1 to 16 bytes. FIFOTHR defaults to 00. A 00h selects one byte and 0Fh selects 16 bytes.
PRETRK: Precompensation start track number. Programmable from track 0 to 255. PRETRK defaults to track 0. A 00h selects track 0 and a FFh selects track 255.

4.6.19. Powerdown Mode

The Powerdown mode command allows the automatic power management. The use of the command can extend the battery life in portable PC applications. To enable auto powerdown the command may be issued during the BIOS power on self test (POST).
DLY: Minimum powerup timer. This bit is active only if APD bit is enabled. Set this bit to 0 assigns a 10msec timer, and to 1 assigns a 0.5sec timer. The timer will be re-initialized after a command execution is finished (idle state) and start to countdown. When the timer is expired, the FDC will enter the powerdown state automatically.
APD: Enable auto powerdown. When set to 1, the auto powerdown is enabled.

4.6.20 Lock

The Lock command allows the user full control of the FIFO parameters after a software reset. If the LOCK bit is set to 1, then the EFIFO, FIFOTHR and PRETRK bits in the Configure command are not affected by a software reset.
After the command byte is written, the result byte must be read before continuing to the next command.

4.6.21 Invalid

If an invalid command (illegal Opcode byte in the command phase) is received by the controller, the controller responds with ST0 in the Result Phase. The controller does not generate an interrupt during this condition. The system reads an 80h from ST0 indicating an invalid command was received.

4.6.22 Perpendicular Mode

The Perpendicular Mode command is designed to support the Perpendicular Recording disk drives (4Mbytes unformatted capacity). The Perpendicular Mode command configures each of the four logical drives as a perpendicular or conventional disk drive. Configuration of the four logical disk drives is done via the D3-D0 bits, or with the GAP and WG control bits. This command should be issued during the initialization of the floppy controller.
A 0 written to Dn sets drive n to conventional mode, and a 1 sets drive n to perpendicular mode. Also, the OW bit offers additional control. When OW=1, changing the values of D3-D0 is enabled. When OW=0, the internal values of D3-D0 are unaffected, regardless of what is written to D3-D0.
The function of the Dn bits must also be qualified by setting both WG and GAP to 0. If WG and GAP are not set to 00, they overrides whatever is programmed in the Dn bits. Table 4-4 below indicates the operation of the FDC based on the values of GAP and WG. D3-D0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset. A hardware reset resets all the bits to zero.

Table 4-4 Effects of WG and GAP bits

GAP	WG	Mode	GAP2 Length during Format	Portion of GAP2 re-written by Write Data Command
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1Mbps)	41 Bytes	38 Bytes

4.7 Parallel Port Mode FDC

In this mode, the floppy disk control signals are available on the parallel port pins. When this mode is selected, the parallel port is not available. There are four modes of operation. These modes can be selected in index 0xF1 of FDC configuration space. The FDC signals are multiplexed onto the Parallel port pins as shown in table below.

0xF1[1:0]		Parallel port function
0	0	Printer
0	1	Printer
1	0	FDC(drive 0 or 1)
1	1	FDC(drive 1)

The FDC signals are multiplexed onto the Parallel port pins as shown in table below.

Conn Pin no.	Chip pin no.	SPP mode	Type	FDC mode	Pin direction
1	144	STBJ	I/O	DS0J	O
2	138	PD0	I/O	INDEXJ	I
3	137	PD1	I/O	TRK0J	I
4	136	PD2	I/O	WPJ	I
5	135	PD3	I/O	RDATAJ	I
6	134	PD4	I/O	DSKCHGJ	I
7	133	PD5	I/O		
8	132	PD6	I/O	MTR0J	O
9	131	PD7	I/O		
10	129	ACKJ	I	DS1J	O
11	128	BUSY	I	MTR1J	O
12	127	PE	I	WDATAJ	O
13	126	SLCT	I	WGATEJ	O
14	143	AFDJ	I/O	DENSEL	O
15	142	ERRJ	I	HDSELJ	O
16	141	INITJ	I/O	DIRJ	O
17	140	SLINJ	I/O	STEPJ	O

Section 5 : Serial Port Registers

Each of the serial ports function as data input/output interface in a microcomputer system. The system software determines the functional configuration of the UARTs via a tri-state 8-bit bi-directional data bus.

The UARTs are completely independent and perform serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of any of the UARTs at any time during the functional operation. Status information reported includes the type and condition of the transfer operations performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UARTs have programmable baud rate generator capable of dividing the timing reference clock input by divisors of 1 to (2^{16} - 1), and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. The UARTs have complete modem-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle communications link.

Table 5-1 lists the register addresses A2 ~ A0 (AEN is equal to zero). DLAB is the divisor latch access bit.

Table 5-1 Serial Port Registers

Register Address	Access (AEN=0)	Abbreviation	Register Name	Access
Base +	DLAB			
0h	0	THR	Transmit Holding Register	W
0h	0	RBR	Receiver Buffer Register	R
0h	1	DLL	Divisor Latch LSB	R/W
1h	1	DLM	Divisor Latch MSB	R/W
1h	0	IER	Interrupt Enable Register	R/W
2h	-	IIR	Interrupt Identification Register	R
2h	-	FCR	FIFO Control Register	W
3h	-	LCR	Line Control Register	R/W
4h	-	MCR	Modem Control Register	R/W
5h	-	LSR	Line Status Register	R
6h	-	MSR	Modem Status Register	R
7h	-	SCR	Scratch Pad Register	R/W

Table 5-2 Register Summary for Each UART Channel

Bit no.			0	1	2	3	4	5	6	7
0 DLAB=0	Receiver Buffer Register (Read only)	RBR	Data bit 0 (note 1)	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
0 DLAB=0	Transmitter Holding Register (Write only)	THR	Data bit 0	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
1 DLAB=0	Interrupt Enable Register	IER	Enable received data available interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Modem Status Interrupt (EMSI)	0	0	0	0
2	Interrupt Ident. Register (Read only)	IIR	' 0' if interrupt pending	Interrupt ID bit	Interrupt ID bit	0	0	0	FIFO enable	FIFO enable
2	FIFO control register (write only)	FCR	FIFO enable	RCVR FIFO Reset	Xmit FIFO reset	reserved	reserved	reserved	RCVR Trigger (LSB)	RCVR Trigger (MSB)
3	Line control register	LCR	Word length select bit 0 (WLS0)	Word Length Select bit 1 (WLS1)	Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
4	Modem control register	MCR	Data Terminal ready (DTR)	Request to send (RTS)	Out 1 (Note 3)	IRQ Enable (Note 3)	Loop	0	0	0
5	Line status register	LSR	Data ready (DR)	Overrun error (OE)	Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) note 2	Error in RCVR FIFO
6	Modem status register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)	Trailing Edge ring indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
7	Scratch register (note 4)	SCR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0 DLAB=1	Divisor latch (LS)	DLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 DLAB=1	Divisor latch (MS)	DLM	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note : 1. Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
2. When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.
3. This bit no longer has a pin associated with it.
4. When operating in the XT mode, this register is not available.

5.1 Line Control Register (LCR)

The system programmer uses this read/write register to specify the format of the asynchronous data communications exchange and set the divisor latch access bit.

Table 5-3 LCR Registers

Bit	Function
7	Divisor latch access bit (DLAB). 1 = To access divisor latches of the baud generator or the alternate function register during a read or write operation. 0 = To access any other register.
6	Break control bit. This bit causes a break condition to be transmitted to the receiving UART. 1 = Serial output (SOUT) is forced to the spacing logic 0 = Break is disabled This bit acts only on SOUT and has no effect on transmitter logic. This enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters are transmitted because of the break : 1. Load all 0s, pad character in response to THRE. 2. Set break after the next THRE. 3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored. During the break, the transmitter can be used as a character timer to accurately establish the break duration.
5	Stick parity bit. When parity is enabled, it is used in conjunction with bit 4 to select, mark or space parity. 1 = Enable stick parity 0 = Disable stick parity
4	Parity select bit. Selects either an odd or even number of 1's to be transmitted/checked in the data word bit and parity bit. 0 = Odd number of 1's (parity bit is a logic 1, mark parity) 1 = Even number of 1's (parity bit is a logic 0, space parity)
3	Parity enable bit. The parity bit is used to produce an even or odd number of 1's when the data bits and the parity bit are added. A parity bit is generated (transmit data) or checked (received data) between the last data bit and the stop bit of the serial data. 0 = Parity bit is not generated/checked 1 = Parity bit is generated/checked
2	Specifies the number of stop bits transmitted with each serial character. The receiver checks the first stop bit only, regardless of the number of stop bits selected. 0 = 1 stop bit 1 = 1.5 stop bits, when a 5-bit data length is selected 1 = 2 stop bits, when 6-, 7-, or 8-bit data length is selected
0-1	Specify the number of data bits (data length) in each transmitted or received serial character. The following are the bit values: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

5.2 Programmable Baud Generator

The UART contains two independently programmable baud generators. The 24-MHz crystal oscillator frequency input is divided by 13, resulting in a frequency of 1.8462-MHz. This is sent to each baud generator and divided by the divisor for the associated UART. The output frequency of the baud generator is 16 X the baud rate, [divisor # = (frequency input) / (baud rate x 16)]. The output of each baud generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either of the divisor latches, a 16-bit baud counter is loaded.

Table 5-5 provides decimal divisors to use with crystal frequencies of 24-MHz. The oscillator input to the chip should always be 24-MHz to ensure that the FDC timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

5.3 Line Status Register (LSR)

This register provides status information to the CPU concerning the data transfer. LSR is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

Table 5-4 Line Status Register Function Definition

Bit	Function
7	In 16450 mode, this bit is set to 0. In FIFO, LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.
6	This bit changes its function depending on whether the device is operating in XT/AT mode. When in the AT mode, this bit is the transmitter empty (TEMT) indicator. It is set to 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to 0 whenever either the THR or TSR contains a data character.
5	Transmitter holding register empty (THRE) indicator. It indicates that the UART is ready to accept a new character for transmission. It also causes the UART to issue an interrupt to the CPU when the THRE interrupt enable is set high. It is set to 1 when a character is transferred from the THRE into TSR. It is reset to 0 whenever the CPU loads the THRE.
4	Break interrupt (BI) indicator. It is set to 1 when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of start bit data bits parity stop bits). It is reset whenever the CPU reads the contents of the LSR. Restarting after a break is received requires the SIN pin to be logical 1 for at least 1/2-bit time.
3	Framing error (FE) indicator. This bit indicates that the received character did not have a valid stop bit. It is set to 1 whenever the stop bit following the last data bit or parity bit is a logic 0 (spacing level). The FE indicator is reset whenever the CPU reads the contents of LSR. The UART tries to resynchronize after a framing error. To do this, it assumes that the FE was due at the next start bit, so it samples this start bit twice and then takes in the data.
2	Parity error (PE) indicator. This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. It is set to 1 upon detection of a parity error and reset to 0 whenever the CPU reads the contents of the LSR.
1	Overrun error (OE) indicator. It indicates that data in the RBR was not read by the CPU before the next data was transferred into the RBR, thereby destroying the previous data. It is set to 1 upon detection of an overrun condition and reset to 0 whenever the CPU reads the contents of the LSR.
0	Receive data ready (DR) indicator. It is set to 1 whenever a complete incoming character has been received and transferred into the RBR. It is reset to 0 by reading the data in the RBR.

Table 5-5 Baud rates using 1.8462 MHz Clock (24 MHz/13)

Desired baud rate	Divisor used to generate 16x clock	C	Bit 5 in CR8 or 9
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note : C refers to % Error Difference between desired and actual, except where shown otherwise, is 0.2 %.

5.4 Interrupt Identification Register (IIR)

This register keeps a record of the four interrupts prioritized by the UART to reduce software overhead during data transfers. The four levels of interrupt conditions in order of priority are: receiver-line-status, received-data-ready, transmitter-holding-register-empty, and modem-status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete.

Table 5-6 Interrupt Identification Register

Bit	Function
6~7	These two bits are set when the FIFO control register bit 0 equals 1.
4~5	Always '0'.
3	In non-FIFO mode, this bit is a logic 0. In FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.
1~2	Identifies the highest interrupt pending.
0	Used in an interrupt environment to indicate whether an interrupt condition is pending. If yes, the IIR contents may be used as a pointer to the appropriate interrupt service routine. 0 = Interrupt pending 1 = No interrupt pending

Table 5-6 Interrupt Control Table

FIFO mode only	Interrupt ID. register	Interrupt Set and Reset Functions			
D3	D2-D1-D0	**Priority level**	**Interrupt type**	**Interrupt source**	**Interrupt Reset control**
0	0- 0- 1	-	None	None	-
0	1- 1- 0	highest	Receiver line status	Overrun error, Parity error, Framing error Break interrupt	Reading the line status register
0	1- 0- 0	second	Received data available	Received data available	Read receiver buffer or the FIFO drops below the trigger level
1	1- 0- 0	second	Character timeout Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 char times and there is at least 1 char in it during this time.	Reading the Receiver Buffer Register
0	0- 1- 0	third	Transmitter holding register empty	Transmitter Holding Register Empty	Reading the IIR Register or writing the transmitter holding register
0	0- 0- 0	fourth	MODEM status	Clear to send or data set ready	Reading the Modem status register

5.5 Interrupt Enable Register (IER)

This register enables the four types of UART interrupts. Each interrupt can individually activate the UR2IRQA or UR1IRQA output signal. Resetting bits 0 ~ 3 of the IER disables the interrupt system. Similarly, setting bits of this register to 1 enables the selected interrupts. Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the interrupt output signal. All other system functions operate in their normal manner, including the setting of the line status and modem status registers.

Table 5-8 Interrupt Enable Register

Bit	Function
0	Enables the received-data-available interrupt
1	Enables the THRE interrupt
2	Enables the receiver-line-status interrupt
3	Enables the modem-status interrupt
4-7	Always 0

5.6 FIFO Control Register

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from FIFO mode to NS16450 mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0 = 1

Bit 4, 5: FCR4 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

5.7 Modem Control Register (MCR)

This register controls the interface with the modem or data set (or a peripheral emulating a modem).

Table 5-9 Modem Control Register

Bit	Function
7-5	Set to logic 0.
4	This bit provides a local loopback feature for the UART diagnostic testing. When set to 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is looped back into the receiver shift register input; the four modem control inputs (DSRJ, CTSJ, RIJ, and DCDJ) are disconnected; and the DTRJ, RTSJ, OUT1, IRQ enable bits in MCR respectively. When operating in AT mode, the modem control output pins are forced to their high (inactive) states. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-receive data paths of the serial port. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem status interrupts are also operational, but the interrupt's sources are the lower four bits of MCR instead of the four modem control inputs. Writing a 1 to any of them causes an interrupt. The interrupts are still controlled by the IER.
3	This bit enables the interrupt when set. In local loopback mode, this bit controls bit 7 of the MSR.
2	This is the OUT1 bit. It does not have an output pin associated with it. It can be written to and read by the CPU. In local loopback mode, this bit controls bit 6 of the MSR.
1	Controls the RTSJ output. In local loopback mode, this bit controls bit 4 of the MSR.
0	Controls the DTRJ output. In local loopback mode, this bit controls bit 5 of the MSR. 1 = DTRJ output is forced to 0 0 = DTRJ output is forced to 1

5.8 Modem Status Register (MSR)

This register gives the current state of the control lines from the modem to the CPU. The bits are set to 1 whenever a control input from the modem changes state, and set to 0 when CPU reads the MSR.

Table 5-10 Modem Status Register

Bit	Function
7	Complement of the DCDJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to IRQ enable in the MCR.
6	Complement of the RIJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.
5	Complement of the DSRJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to DTR in the MCR.
4	Complement of the CTSJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.
3	Delta data carrier detect (DDCD) indicates that the DCDJ input to the chip has changed state. Whenever bit 0, 1, 2 or 3 is set to 1, a modem status interrupt is generated.
2	Trailing edge of ring indicator (TERI) detector indicates that the RIJ input of the chip has changed from a low to high state.
1	Delta data set ready (DDSR) indicates that the DSRJ input to the chip has changed its state since the last time it was read by the CPU.
0	Delta clear to send (DCTS) indicates that CTSJ input to the chip has changed its state since the last time it was read by CPU.

5.9 Scratchpad Register (SCR)

The 8-bit read/write register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

5.10 Infrared Interface

5.10.1 Sharp-IR Mode

This mode supports bidirectional data communication with a remote device using infrared radiation as the transmission medium. Sharp-IR uses Amplitude Shift Key (ASK) and allows serial communication at baud rates up to 38.4K Baud. The format of the serial data is similar to the UART data format, a zero value start bit, followed by up to 8 data bits, an optional parity bit, and ending with at least one stop bit with a binary value of one. A zero is signalled by sending a 500KHz continuous pulse train of infrared radiation. A one is signalled by the absence of any infrared signal.
The device operation in Sharp-IR mode is similar to the operation in UART. The main difference is that the data transfer is normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of this mode is controlled by the IR mode bits in the UART' s configuration space. Both UART1 and UART2 can be programmed in this mode. The transfer signals will rout to SIN1/SIN2 and SOUT1/SOUT2. Two additional pins, IRRX and IRTX, are also provided.

5.10.2 IrDA SIR Mode

This is an operation mode similar to Sharp-IR. The IrDA 1.0 SIR allows serial communication at baud rates up to 115.2K Baud. The data format is the same as Sharp-IR mode except no parity bit is needed. A zero is signalled by sending a single infrared pulse. A one is signalled by not sending any pulse. The width of each pulse is 3/16ths of a single bit time.
The device operation in IrDA 1.0 SIR mode is similar to the operation in UART. The main difference is that the data transfer is normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of this mode is controlled by the IR mode bits in the UART' s configuration space. Both UART1 and UART2 can be programmed in this mode. The transfer signals will rout to SIN1/SIN2 and SOUT1/SOUT2. Two additional pins, IRRX and IRTX, are also provided.

Section 6 : Keyboard Controller and Real Time Clock Functional Description

6.1 Keyboard and RTC ISA Interface

The M512x ISA interface is functionally compatible with the M8042 style host interface. It consists of the D0-D7 data bus; the IORJ, IOWJ and the Status register, Input Data register, and Output Data register. Table below shows how the interface decodes the control signals. In addition to the above signals, the host interface includes keyboard and mouse IRQ' s.

ISA I/O Address Map

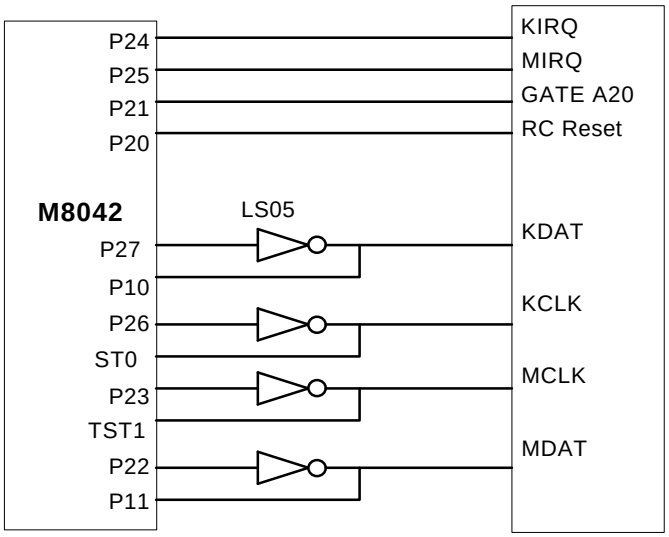
ISA Address	BLOCK	FUNCTION
0x70 (R/W)	RTC	Address Register (70H)
0x71 (R/W)	RTC	Data Register (71H)

ISA Address	nIOW	nIOR	Block	Function (Note 1)
0x60	0	1	KDATA	Keyboard Data Write (C/D=0) (60h)
	1	0	KDATA	Keyboard Data Read (60h)
0x64	0	1	KDCTL	Keyboard Command Write (C/D=1) (64h)
	1	0	KDCTL	Keyboard Status Read (64h)

Note 1 : These registers consist of three separate 8-bit registers. Status, Data/Command write and Data Read.

6.2 Keyboard Controller

The Universal Keyboard Controller uses an M8042 microcontroller CPU cord. This section concentrates on the M512x enhancements to the M8042.



Keyboard and Mouse Interface

KIRQ is the Keyboard IRQ

MIRQ is the Mouse IRQ

P21 is the CIO14 alternate function, can be used for Gate A20.

P20 can be used to optionally RC reset.

Keyboard Data Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

Keyboard Data Read

This is an 8 bit read only register. If enabled by "ENABLE FLAGS", the KIRQ output is cleared and the OBF flag in the status register is cleared. If not enabled, the KIRQ and/or AUXOBF1 must be cleared in software.

Keyboard Command Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

Keyboard Status Read

This is an 8 bit read only register. Refer to the description of the Status Register for more information.

CPU-to-Host Communication

The heart of M512x can write to the Output Data register via register DBB. A write to this register automatically sets Bit 0 (OBF) in the Status register. See table below

Host Interface Flags

M8042 Instruction	FLAG
OUT DBB	Set OBF, and, if enabled, the KIRQ output signal goes high

Host-to-CPU Communication

The host system can send both commands and data to the Input Data register. The CPU differentiates between commands and data by reading the value of Bit 3 of the Status register. When bit 3 is "1", the CPU interprets the register contents as a command. When Bit 3 is "0", the CPU interprets the register contents as data. During a host write operation, bit 3 is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

KIRQ

If "EN FLAGS" has been executed and P24 is set to a one: the OBF flag is gated onto KIRQ. The KIRQ signal can be connected to system interrupt to signify that the M512x CPU has written to the output data register via "OUT DBB, A". If P24 is set to a zero, KIRQ is forced low. At power-up, after a valid reset pulse has been delivered to the device, KIRQ is reset to 0. KIRQ normally reflects the status of "DBB".

If "ENFLAGS has not been executed: KIRQ can be controlled by writing to P24. Writing a zero to P24 forces KIRQ low, a high forces KIRQ high.

MIRQ

If "EN FLAGS" has been executed and P25 is set to a one: IBF is inverted and gated onto MIRQ. The MIRQ signal can be connected to system interrupt to signify that the M512x CPU has read the DBB register. If "ENFLAGS has not been executed : MIRQ and is controlled by P25. Writing a zero to P25 forces MIRQ low, a high forces MIRQ high. (MIRQ is normally selected as IRQ12 for mouse support.)

Gate A20

A general purpose P21 can be routed out to the Common I/O pin CIO14 for use as a software controlled Gate A20 or user defined output.

External Keyboard and Mouse Interface

Industry-standard PC-AT compatible keyboards employ a two-wire, bi-directional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the M512x provides four signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The M512x has four high-drive, open-drain output (1), bidirectional port pins that can be used for external serial interfaces, such as ISA external keyboard and PS/2-type mouse interfaces. They are KCLK, KDAT, MCLK and MDAT.

P26 is inverted and output as KCLK. The KCLK pin is connected to TESTO. P27 is inverted and output as KDAT. The KDAT pin is connected to P70. P23 is inverted and output as MCLK. The MCLK pin is connected to TEST1. P22 is inverted and output as MDAT. The MDAT pin is connected to P11. NOTE : External pull-ups may be required.

Keyboard Power Management

The keyboard provides support for two power saving modes: soft power down mode and hard power down mode. In soft power down mode, the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode, the clock to the M8042 is stopped. Efforts are made to reduce power wherever possible.

Soft Power Down Mode

This mode is entered by executing a HALT instruction. The execution of program code is halted until either RESET is driven active or a data byte is written to the DBBIN register by a master CPU. If this mode is exited using the interrupt, and the IBF interrupt is enabled, then program execution resumes with a CALL to the interrupt routine, otherwise the next instruction is executed. If it is exited using RESET, then a normal reset sequence is initiated and program execution starts from program memory location 0.

Hard Power Down Mode

This mode is entered by executing a STOP instruction. The oscillator is stopped by disabling the oscillator driver cell. When either RESET is driven active or a data byte is written to the DBBIN register by a master CPU, the mode will be exited (as above). However, as the oscillator cell will require an initialization time, either RESET must be held active for sufficient time to allow the oscillator to stabilize. Program execution will resume as above.

Interrupts

The M512x provides the two M8042 interrupts. IBF and the Timer/Counter Overflow.

Memory Configurations

The M512x provides 2K of on-chip ROM and 256 bytes of on-chip RAM.

Register Definitions

Host I/F Data Register

The Input Data register and, Output Data register, are each 8 bits wide. A write to this 8 bit register will load the Keyboard Data Read Buffer, set the OBF flag and set the KIRQ output if enabled. A read of this register will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag. Refer to the KIRQ and Status register descriptions for more information.

Host I/F Status Register

The Status register is 8 bits wide. Table below shows the contents of the Status register.

Status Register

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	UD	UD	C/D	UD	IBF	OBF

This register is cleared on a reset. This register is read-only for the Host and read/write by the M512x.

UD Writable by M512x. These bits are user-definable.

C/D (Command Data) This bit specifies whether the input data register contains data or a command (0 = data, 1 = command). During a host data/command write operation, this bit is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

IBF (Input Buffer Full) This flag is set to 1 whenever the host system writes data into the input data register. Setting this flag activates the M512x' s nIBF (MIRQ) interrupt if enabled. When the M512x reads the input data register (DBB), this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF (Output Buffer Full) This flag is set to 1 whenever the M512x writes to the output data register (DBB). When the host system reads the output data register, this bit is automatically reset.

Default Reset Conditions

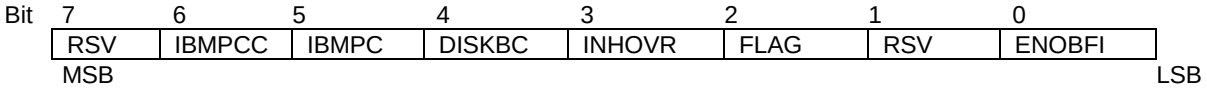
The M512x has one source of reset: an external reset via the RESET pin. Refer to table of Resets below for the effect of each type of reset on the internal registers.

Resets

DESCRIPTION	HARDWARE RESET (RESET)
KCLK	Weak High
KDAT	Weak High
MCLK	Weak High
MDAT	Weak High
Host I/F Data Reg	N/A
Host I/F Status Reg	OOH

NC : No Change
N/A : Not Applicable

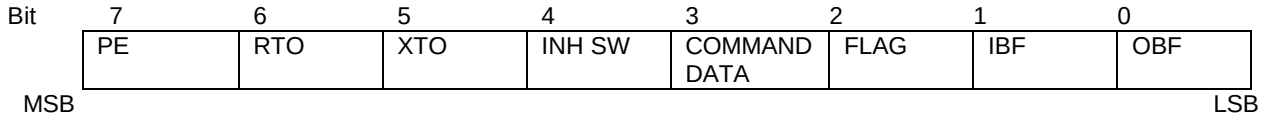
Command Byte Bit Definition



Command Byte Bit Definition

Bit Number	Bit Definition
7	Reserved. This bit should be 0.
6	IBM Personal Computer Compatibility Mode. Writing a 1 to this bit tells the keyboard controller that it needs to convert the scan codes received from the keyboard to those used by the IBM PC.
5	IBM Personal Computer Mode. Writing a 1 to this bit signals the keyboard controller not to check parity, or convert scan codes.
4	Disable Keyboard. Writing a 1 to this bit disables Keyboard I/F by driving the clock-line low.
3	Inhibit Override. Writing a 1 to this bit disables the Keyboard-Inhibit function.
2	System Flag. The M8042 places the value written to this bit in the system flag bit of its status register.
1	Reserved. This bit should be 0.
0	Enable Output-Buffer-Full interrupt. Writing a 1 to this bit causes the controller to generate an interrupt when it places data into its output buffer.

Status Register Bit Definition



Status Register Bit Definition

Bit Number	Bit Definition
7	Parity Error. 0 : The last byte of received data had odd parity. 1 : The last byte of received data had even parity.
6	Receive Time-Out. 0 : No error 1 : The keyboard started a transmission but did not finish within a specific receive time-out-delay.
5	Transmit Time-Out 0 : No error 1 : The keyboard started a transmission but was not properly completed.
4	Inhibit Switch 0 : Keyboard is inhibited 1 : Keyboard is not inhibited
3	Command/Data Byte Select 0 : Data byte 1 : Command byte
2	System Flag. This bit is set to 0 during power-on
1	Input Buffer Full 0 : Keyboard controller input buffer is empty 1 : Data has been written into the buffer
0	Output Buffer Full 0 : Keyboard controller output buffer is empty 1 : Keyboard controller output buffer has placed data into

Commands' Description

Command	Description
20H	**Read keyboard controller's command byte**. The keyboard controller puts the command byte in its output buffer, available at I/O port 60H.
60H	**Write keyboard controller's command byte**. The next byte from the system at I/O port 60H is placed as the controller command.
A1H	**Output controller version number**. A single byte of the controller's version comes at I/O port 60H.
AAH	**Self test**. This commands the controller to do internal diagnostics tests. A Hex 55 is placed in the output buffer if no errors are detected.
ABH	**Interface test**. This command checks the clocks and data lines of the keyboard. 00: no errors detected 01: clock is stuck low 02: clock is stuck high 03: data is stuck low 04: data is stuck high
ADH	**Disable keyboard**. It disables the keyboard clock line, and also sets the corresponding bit in the command byte. It resumes after giving any keyboard command.
AEH	**Enables keyboard**. It enables the keyboard clock line, and also resets the corresponding bit in the command byte.
D0H	**Read output port**. This command places the output port (P2) status of the controller at I/O port 60H.
D1H	**Write output port**. Data following this command is loaded onto the controller's output port.
E0H	**Read test inputs**. This makes the current status of the test inputs of the controller's KBC and KBD available to the system at I/O port 60H as bit 0 and bit 1, respectively.
F0H ~ FFH	**Pulse output port**. Bits 0 ~ 3 of the controller's output port may be pulsed low for a period of approximately 6 seconds. The same bits of the command itself indicate the bits to be pulsed. A 0 indicates that the bits should be pulsed, a 1 indicates that the bits should not be modified.

6.3 Real Time Clock

This RTC Super Cell is a complete time of day clock with alarm and one hundred year calendar, a programmable periodic interrupt and a programmable square wave generator.

■ Time of day Register Descriptions

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar and alarm bytes may either be binary or binary-coded decimal. Table below shows the binary and BCD formats of the 10 time, calendar and alarm locations.

Time, Calendar and Alarm Data Modes

Address	Function	Decimal Range	Binary Mode	BCD Mode
00	Seconds	0-59	$0-$3B	$0-$59
01	Seconds Alarm	0-59	$0-$3B	$0-$59
02	Minutes	0-59	$0-$3B	$0-$59
03	Minutes Alarm	0-59	$0-$3B	$0-$59
04	Hours	1-12 0-23	$1-$C(AM) $81-$8C(PM) $0-$17	$1-$12(AM) $81-$92(PM) $0-$23
05	Hours Alarm	1-12 0-23	$1-$C(AM) $81-$8C(PM) $0-$17	$1-$12(AM) $81-$92(PM) $0-$23
06	Day of Week	1-7	$1-$7	$1-$7
07	Date	1-31	$1-$1F	$1-$31
08	Month	1-12	$1-$C	$1-$12
09	Year	0-99	$0-$63	$0-$99

■ Address Map

The memory consists of 242 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, alarm data, and four control and status bytes. All 256 bytes are directly readable and writable by the processor program except for the following: 1) Registers C and D are read only. 2) bit 7 of Register A is read only and 3) the high order bit of the seconds byte is read only. The contents of four control and status registers (A, B, C, and D) are described in Registers.

■ Set Operation

Before initialization of the internal registers of the M512x, the SET bit in register B should be set to a 1 to prevent RTC from updating. The CPU then initializes the first ten locations in the selected format (binary or BCD). The SET bit should then be cleared to allow updating. After initialization and enabling, the M512x will perform clock calendar updates in the selected data mode.

■ BCD and Binary Format

The 24/12 bit in register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initialization, the 24/12 bit cannot be changed without reinitializing the hour locations. In 12 hour format, the high order bit of the hours byte indicates PM when it is a 1.

■ Alarm Operation

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is in any byte from C0h to FFh. An alarm interrupt each hour is created with "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

■ Interrupts

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt maybe programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt maybe selected for rates from half-a-second to 30.517µs. The update ended interrupt maybe used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in register B enable the three interrupts. Writing a 1 to an interrupt enable bit permits that interrupt to be initiated when the event occurs. A 0 in the interrupt enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enable, the IRQ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

■ Divider Control

The divider control bits have three uses, as shown in Table below. Three usable operating time bases may be selected. The divider chain maybe held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one-half second later.

Divider Configurations

	Divider bits			
OSC1 Frequency	DV2	DV1	DV0	Mode
4.194304 MHz	0	0	0	Operate
1.048576 MHz	0	0	1	Operate
32.768 MHz	0	1	0	Operate
Any	1	1	*	Divider reset

■ Periodic Interrupt Selection

The periodic interrupt allows the IRQJ pin to be triggered from once every 30.517µs. The periodic interrupt is separate from the alarm interrupt which maybe outputted from once-per-second to once-per-day.

Table below shows that the periodic interrupt rate is selected with the same register A bits which select the square-wave frequency.

Periodic Interrupt Rate Table

RS value	4.194304 MHz or 1.048576 MHz Time Base	32.768 KHz Time Base
0h	none	none
1h	30.517 µs	3.90625 ms
2h	61.035 µs	7.8125 ms
3h	122.070 µs	122.070 µs
4h	244.141 µs	244.141 µs
5h	488.281 µs	488.281 µs
6h	976.562 µs	976.562 µs
7h	1.953125 ms	1.953125 ms
8h	3.90625 ms	3.90625 ms
9h	7.8125 ms	7.8125 ms
Ah	15.625 ms	15.625 ms
Bh	31.25 ms	31.25 ms
Ch	62.5 ms	62.5 ms
Dh	125 ms	125 ms
Eh	250 ms	250 ms
Fh	500 ms	500 ms

■ Update Cycle

The RTC executes an update cycle one-per-second, assuming one of the proper time bases is in place, the DV2-DV0 divider is not clear, and the SET bit in register B is clear. The SET bit in the 1 state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the second byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11xxxxxx) is present in all three positions.

With a 4.194304 MHz or 1.048576 MHz time base, the update cycle takes 248µs while a 32.768 KHz time base update cycle takes 1984 µs. During the update cycle, the time, calendar and alarm bytes are not accessible by the processor program. The RTC protects the program from reading transitional data. This protection is provided by switching the time, calendar and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete, the output will be undefined. The update in progress (UIP) status bit is set during the interval.

Three methods of accommodating non-availability during update are usable by the program. In discussing the three methods, it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in register C should be cleared.

The second method uses the update in progress bit (UIP) in register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. After the UIP bit goes high, the update cycle begins 244 µs later. Therefore, if a low is a read in the UIP bit, the user has at least 244µs before the time/calendar data will be changed. If a 1 is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in register A is set high between the setting of the PF bit in register C.

To properly setup the internal counters for daylight savings time operation, the user must set the time at least two seconds before the roll-over will occur. Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

■ **Register Description**

The RTC has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Register 0AH

Index register port : 70H

Data register port : 71H

Index : 0AH

(Read/Write except UIP)

7	6	5	4	3	2	1	0
UIP	DV	DV1	DV0	RS3	RS2	RS1	RS0

Bits 3-0. The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 7 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by RESETJ.

Bits 6-4. Three bits are used to permit the program to select various conditions of the 22 stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 6 shows that time bases of 4.194304 MHz, 1.048576 MHz, and 32.768 KHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed, the first update cycle begins one-half second later. These three read/write bits are not affected by RESET.

Bit 7. The update in progress (UIP) bit is a status flag that maybe monitored by the program. When UIP is a "1", the update cycle is in progress or will begin. When UIP is a "0", the update cycle is not in progress and will not be for at least 244µs (for all time bases). The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero - it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibits any update cycle and then clears the UIP status bit.

Register 0Bh

Index register port : 70H

Data register port : 71H

Index : 0BH

(Read/Write)

7	6	5	4	3	2	1	0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

Bit 0. The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday of April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday of October when the time first reaches 1:59:59 AM, it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or rest.

Bit 1. The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hours mode (a "0"). This is a read/write bit, which is affected only by software.

Bit 2. The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or RESET. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded decimal (BCD) data.

Bit 3. When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero, the SQW pin is held low. The state of SQWE is cleared by the RESETJ pin. SQWE is a read/write bit.

Bit 4. The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert IRQ. The RESETJ pin going low or the SET bit going high clears the UIE bit.

Bit 5. The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) bit in Register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes and the three alarm bytes (including a "don't care" alarm code of binary 11xxxxxx). When the AIE bit is a "0", the AF bit does not initiate an IRQ signal. The RESETJ pin clears AIE to "0". The internal functions do not affect the AIE bit.

Bit 6. The periodic interrupt enable (PIE) bit is read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the IRQ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A zero in PIE blocks IRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal KS82C6818A functions, but is cleared to "0" by a RESETJ.

Bit 7. When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by RESET or internal functions of the M512x.

Register 0Ch

Index register port : 70H

Data register port : 71H

Index : 0CH

(Read only)

7	6	5	4	3	2	1	0
IRQF	PF	AF	UF	0	0	0	0

Bits 3-0. The unused bits of Status Register C are read as 0's and cannot be written.

Bit 4. The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting IRQ, UF is cleared by a Register C read or a RESETJ.

Bit 5. A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the IRQ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A reset or a read of Register C clears AF.

Bit 6. The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates and IRQ signal and sets the IRQF bit when PIE is also a "1". The PF bit is cleared by a /RESET/ or a software read of Register C.

Bit 7. The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true :

PF = PIE = "1"

AF = AID = "1"

UF = AIE = "1"

Any time the IRQF bit is a "1", the IRQ pin is driven low. All flag bits are cleared after Register C is read by the program when the RESET pin is low.

Register 0Dh

Index register port : 70H

Data register port : 71H

Index : 0DH

(Read only)

7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Bits 6-0. The remaining bits of Register D are unused. They cannot be written, but are always read as 0's.

Bit 7. The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the VBAT is satisfactorily connected. A "0" appears in the VRT bit when the VBAT is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read only bit which is not modified by the RESETJ pin. The VRT bit can only be set by reading Register D.

Section 7 : BIOS

7.1 BIOS BUFFER

The M512x contains one 245 type buffer that can be used for a BIOS Buffer. If the BIOS buffer is not used, then ROMCSJ and ROMOEJ must be tied high so as not to interfere with the boot ROM.

This function allows data transmission from the RD bus to the SD bus or from the SD bus to the RD bus. The direction of the transfer is controlled by ROMOEJ. The enable input, ROMCSJ, can be used to disable the transfer and isolate the buses.

ROMCSJ	ROMOEJ	
L	L	RD [0:7] data to SD [0:7] bus
L	H	SD [0:7] data to RD [0:7]
H	X	Isolation

Section 8 : Parallel Port

8.1 Parallel Port Interface

The M512x incorporates one IBM XT/AT compatible parallel port. The M512x supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Please refer to the Configuration Description (Section 3) for information on disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The M512x also incorporates a protective circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below:

DATA PORT	BASE ADDRESS + 00H
STATUS PORT	BASE ADDRESS + 01H
CONTROL PORT	BASE ADDRESS + 02H
EPP ADDR PORT	BASE ADDRESS + 03H
EPP DATA PORT 0	BASE ADDRESS + 04H
EPP DATA PORT 1	BASE ADDRESS + 05H
EPP DATA PORT 2	BASE ADDRESS + 06H
EPP DATA PORT 3	BASE ADDRESS + 07H

The bit map of these registers :

Table 8-1 Bit Mapped Registers

Data Port	D0	D1	D2	D3	D4	D5	D6	D7	Note
	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
Status Port	TMOUT	0	OSLC	ERRJ	SLCT	PE	ACKJ	BUSYJ	1
Control Port	STROBE	AUTOFD	INITJ	SLC	IRQE	PCD	0	0	1
EPP ADDR Port	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2, 3
EPP DATA Port 0	PD0	PD1	PD2	DP3	PD4	PD5	PD6	PD7	2, 3
EPP DATA Port 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2, 3
EPP DATA Port 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2, 3
EPP DATA Port 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2, 3

Note 1: These registers are available in all modes.
2: These registers are only available in EPP mode.
3: For EPP mode, IOCHRDY must be connected to the ISA bus.

Table 8-2 Parallel Port Connector

HOST Connector	Pin No.	STANDARD	EPP	ECP
1	77	StrobeJ	WriteJ	StrobeJ
2-9	71-68, 66-63	PData <0:7>	PData<0:7>	PData<0:7>
10	62	AckJ	Intr	Ack
11	61	Busy	WaitJ	Busy,PeriphAck(3)
12	60	PE	(NU)	PError, nAckReverse(3)
13	59	Select	(NU)	Select
14	76	AutofdJ	DSTRBJ	AutoFd, HostAck(3)
15	75	ErrorJ	(NU)	Fault(1) PeriphRequest(3)
16	74	InitJ	(NU)	Init(1) ReverseRqst(3)
17	73	SelectinJ	AstrbJ	Selectin(1,3)

(1) = compatible Mode
(3) = High Speed Mode

Note : For the cable interconnection required for ECP support and the Slave Connector pin numbers, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.09, Jan. 7, 1993. This document is available from Microsoft.

8.2 IBM XT/AT Compatible, Bi-Directional and EPP Modes

DATA PORT Address Offset = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus with the rising edge of the IOWJ input. The contents of this register are buffered (non inverting) and output onto the PD0 -PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

STATUS PORT Address Offset = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of an IORJ read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT
This bit is valid in EPP mode only and indicates that a 10 µsec time out has occurred on the EPP bus. A logic 0 means that no time out error has occured; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a zero. Writing a zero to this bit has no effect.

BITS 1, 2 - are not implemented as register bits. During a read of the Printer Status Register, these bits are at low level.

BIT 3 ERRJ - ERRORJ
The level on the ERRORJ input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 ACKJ - ACKNOWLEDGEJ
The level on the ACKJ input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the Printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 BUSYJ - BUSYJ
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

CONTROL PORT Address Offset = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the STROBEJ output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the AUTOFDJ output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 INITJ - INITIATE OUTPUTJ
This bit is output onto the INITJ output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the SLCTINJ output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enalbe interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going ACKJ input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is valid in extended mode only (CRC<7> = 0). In printer mode, the direction is always out regardless of the state of this bit. In bi-directional mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

EPP ADDRESS PORT Address Offset = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PDO - PD7 ports, the leading edge of IOWJ causes an EPP Address WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP Write cycle. During a READ operation, PDO -PD7 ports are read, the leading edge of IOR causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the Pdata for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 0 Address Offset = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non-inverting) and output onto the PD0 - PD7 ports, the leading edge of IOWJ causes an EPP DATA WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0- PD7 ports are read, the leading edge of IOR causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the Pdata for the duration of the IOR cycle. This register is only available in EPP mode. To maintain compatibility with Intel' s 82360SL device that has 32-bit Host bus interface, four consecutive byte address locations (data port 0~4) are provided for transferring data.

EPP DATA PORT 1 Address Offset = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Please refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 2 Address Offset = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Please refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 3 Address Offset = 07H

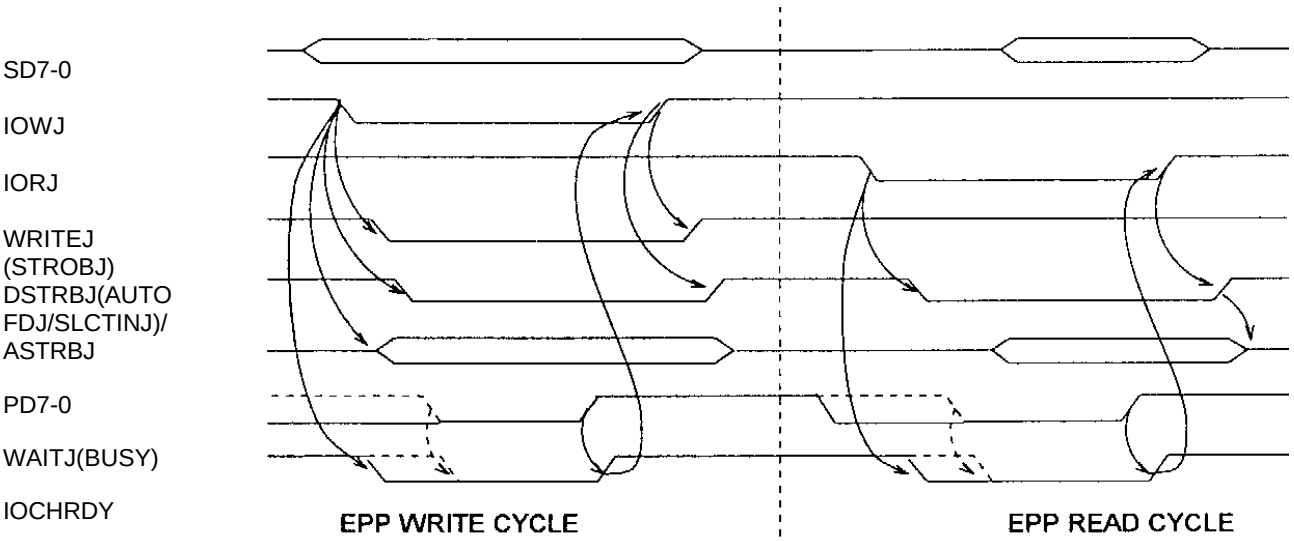
The EPP Data Port 3 is located at an offset of '07H' from the base address. Please refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10 usec have elapsed from the start of the EPP cycle (IORJ or IOWJ asserted) WAITJ will be deasserted. If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

EPP mode version 1.7 Timing



The timing for a Write/Read EPP 1.7 operation is shown in timing diagram above
The sequence of operation is :

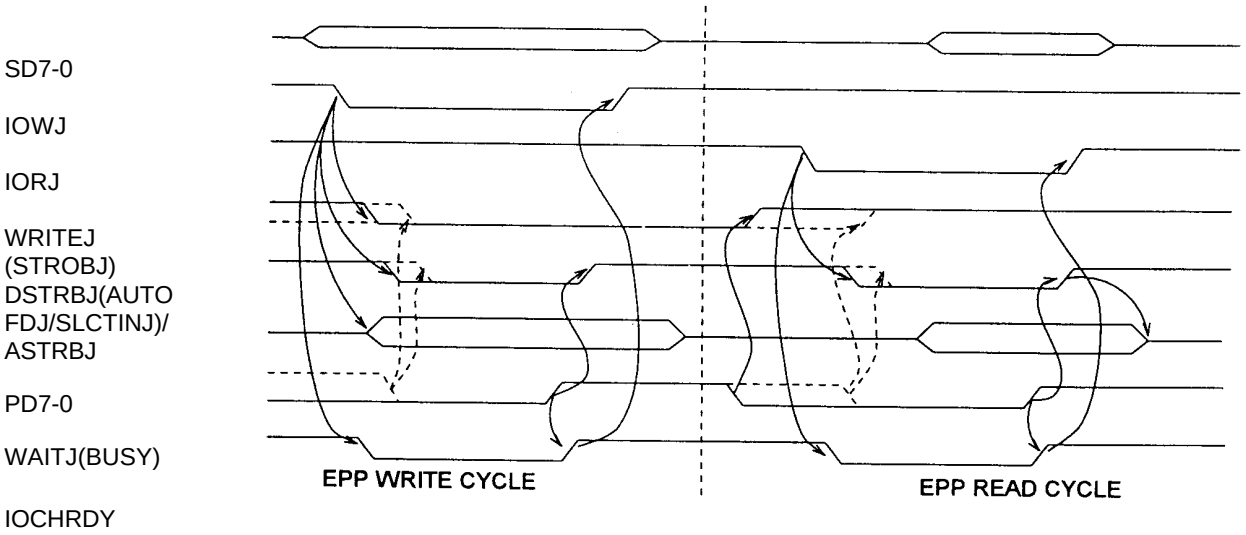
EPP 1.7 Data/Address Write

1. The host writes a byte to Data (Address) port. IOWJ goes low to drive data to PD7-0.
2. The EPP pulls WRITEJ low to indicate it' s a write cycle.
3. The EPP pulls DSTRBJ (ASTRBJ) low to signal that data is valid.
4. If WAITJ goes low during the cycle, IOCHRDY is pulled low.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then IOWJ will go high
6. When IOWJ goes high, it pulls WRITEJ & DSTRBJ(ASTRBJ) high, and then the EPP can change PD7-0

EPP 1.7 Data/Address Read

1. The host reads a byte from Data (Address) port. IORJ goes low to input data from PD7-0.
2. The EPP keeps WRITEJ high to indicate it' s a read cycle.
3. The EPP pulls DSTRBJ (ASTRBJ) low to indicate that peripheral have to start sending data.
4. If WAITJ is low during the cycle, IOCHRDY is pulled low.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then IORJ will go high
6. When IORJ goes high, it pulls WRITEJ & DSTRBJ(ASTRBJ) high, and then the peripheral can tri-state PD7-0

EPP mode version 1.9 Timing



EPP WRITE CYCLE EPP READ CYCLE

The timing for a Write/Read EPP 1.9 operation is shown in timing diagram above
The sequence of Write/Read operation is :

EPP 1.9 Data/Address Write

1. The host writes a byte to Data (Address) port. IOWJ goes low to drive data to PD7-0.
2. IOCHRDY goes low and waits for WAITJ to go low.
3. If WAITJ goes low or already low, the EPP pulls or keeps WRITEJ low to show being a write cycle.
4. The EPP pulls DSTRBJ (ASTRBJ) low to indicate that data is ready and waits for WAITJ to go high.
5. When WAITJ goes high, it pulls IOCHRDY and DSTRBJ (ASTRBJ) high, and then IOWJ will go high to turn off this cycle.

EPP 1.9 Data/Address Read

1. The host reads a byte from Data (Address) port. IORJ goes low to input data from PD7-0.
2. IOCHRDY goes low and waits for WAITJ to go low.
3. If WAITJ goes low or was already low, the EPP pulls or keeps WRITEJ high to indicate being a read cycle.
4. The EPP pulls DSTRBJ (ASTRBJ) low to signal the peripheral to start sending data and waits for WAITJ to go high.
5. When WAITJ goes high, it pulls IOCHRDY and DSTRBJ (ASTRBJ) high, and then IORJ will go high to turn off this cycle.

Table 8-3 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
WRITEJ	WriteJ	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/ Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP.)
WAIT	WaitJ	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	DATA StrobeJ	O	This signal is active low. It is used to denote data read or write operation.
RESET	ResetJ	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	Address StrobeJ	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Select Status	I	Same as SPP mode.
ERRJ	Error	I	Same as SPP mode.
PDIR	Parallel Port Direction	O	This output shows the direction of the data transfer on the parallel port bus. A low means an output /write condition and a high means an input/read condition. This signal is normally a low (output/write) uniess PCD of the control register is set or if an EPP read cycle is in progress.

Note 1: SPP and EPP can use 1 common register.
Note 2: WriteJ is the only EPP output that can be over-ridden by SPP control port during an EPP cycle.
For correct EPP read cycles, PCD is required to be a low.

Extended Capabilities Parallel Port

ECP provides a number of advantages, some of which are listed below.

- High performance half-duplex forward and reverse channel
- Interlocked handshake, for fast reliable transfer
- Optional single byte RLE compression for improved throughput (64:1)
- Channel addressing for low-cost peripherals
- Maintains link and data layer separation
- Permits the use of active output drivers
- Permits the use of adaptive signal timing
- Peer-to-peer capability

PWord A port word; equal in size to the width of the ISA interface. For this implementation, PWord is always 8 bits.
1 A high level.
0 A low level.

These terms may be considered synonymous:

- PeriphClk, AckJ
- HostAck, AutoFdJ
- PeriphAck, Busy
- PeriphRequestJ, FaultJ
- ReverseRequestJ, InitJ
- AckReverseJ, PError
- Xflag, Select
- ECPMode, SelectinJ
- HostClk, StrobeJ

Vocabulary
The following terms are used in this document:
assert When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
forward Host to Peripheral communication.
reverse Peripheral to Hose communication.

Reference Document
IEEE 1284 Extended Capabilities Port Protocol
and ISA Interface Standard, Rev 1.09, Jan 7, 1993. This document is available from Microsoft.
The bit map of the Extended Parallel Port registers is :

	D7	D6	D5	D4	D3	D2	D1	D0	Note
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/ RLE	Address or RLE field							2
dsr	BusyJ	AckJ	PError	Select	FaultJ	0	0	0	1
dcr	0	0	Direction	ackIntEn	Selectin	InitJ	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	0	0	0	0	0	0	
ecr	MODE			ErrintrEnJ	DmaEn	Service Intr	full	empty	

Note 1: These registers are available in all modes.
Note 2: All FIFOs use one common 16 byte FIFO.

ISA IMPLEMENTATION STANDARD

This specification describes the standard ISA interface to the Extended Capabilities Port (ECP). All ISA devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.09, Jan. 7, 1993. This document is available from Microsoft.

Description

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Decompression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 8-4 ECP Pin Descriptions

Name	Type	Description
StrobeJ	O	During write operations StrobeJ registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
AckJ	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with AutoFdJ in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with StrobeJ in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with StrobeJ. PeriphAck also provides command information in the reverse direction.
PError (Ack ReverseJ)	I	Used to acknowledge a change in the direction of the transfer (asserted= forward). The peripheral drives this signal low to acknowledge ReverseRequestJ. It is an "interlocked" handshake with ReverseRequestJ. The host relies upon AckReverseJ to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
AutoFdJ (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with AckJ in the reverse direction. This signal indicates whether the data lines contain ECP address or data, the host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with AckJ. HostAck also provides command information in the forward phase.
FaultJ (Periph RequestJ)	I	Generates an error interrupt when asserted. This signal provides a mechanism or peer-to-peer communication. This signal is valid only in the forward direction. During ECP mode, the peripheral is permitted (but not required) to level this pin to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
InitJ	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and SelectInJ is high.
SelectInJ	O	Always deasserted in ECP mode.

Register Definitions

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ECR. The table below lists these dependencies. Operation of the devices in modes other than those specified is undefined.

Table 8-5 ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.
Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 8-6 Mode Descriptions

Mode	Description*
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	(Reserved)
110	Test mode
111	Configuration mode

* Refer to ECR Register Description

DATA and ECPAFIFO PORT Address Offset = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus on the rising edge of the IOWJ input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO- Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet.

Device Status Register (DSR) Address Offset = 01H

The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status port are defined as follows:

BIT 3 FaultJ
The level on the Fault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select
The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError
The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 AckJ
The level on the AckJ input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 BusyJ
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

Device Control Register (DCR) Address Offset = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 being affected; bits 6-7 are read as 0.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the STROBEJ output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the AUTOFDJ output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 INITJ - INITIATE OUTPUT
This bit is output onto the INITJ output without inversion.

BIT 3 SELECTIN
This bit is inverted and output onto the SLCTINJ output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 acklntEn - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the ACKJ input. Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION
If mode = 000 or mode = 010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

CFIFO (Parallel Port Data FIFO) Address Offset = 400h

Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ECPDFIFO (ECP Data FIFO) Address Offset = 400h

Mode = 011
Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

TFIFO (Test FIFO Mode) Address Offset =400H

Mode = 110
Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.

Data in the tFIFO will not be transmitted to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and servicelntr bits.

The writelntr Threshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until servicelntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readlntr Threshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until servicelntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

CNFGA (Configuration Register A) Address Offset = 400H

Mode = 111
This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (Pword = 1 byte)

CNFGB (Configuration Register B) Address Offset = 401H

Mode = 111
BIT 7 compress
This bit is read only. During a read, it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression.

BIT 6 IntrValue
Returns the value on the ISA IRQ line to determine possible conflicts.

BITS 5~0 : The ECP Parallel port Configuration register B must reflect the IRQ and DRQ selected by the Configuration registers

IRQ selected	Config.Reg. B Bits 5: 3
14	110
13	101
11	100
10	011
9	010
7	001
5	111
Others	000

DMA selected	Config.Reg. B Bits 5: 3
3	011
2	010
1	001
Others	000

ECR (Extended Control Register) Address Offset = 402H

Mode = all
This register controls the extended ECP parallel port functions.

BITS 7, 6, 5
These bits are Read/Write and select the Mode.

BIT 4 ErrlntrEnJ
Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of FaultJ.
0: Enables an interrupt pulse on the high to low edge of FaultJ. Note that an interrupt will be generated if Fault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write

1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disable DMA unconditionally.

BIT 2 serviceIntr
Read/Write
1: Disable DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred, serviceIntr bit shall be set to a 1 by hardware, it must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.
case dmaEn = 1:
During DMA (this bit is set to a 1 when terminal count is reached).
case dmaEn = 0 direction = 0:
This bit shall be set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.
case dmaEn = 0 direction = 1:
This bit shall be set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

BIT 1 full
Read only
1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

BIT 0 empty
Read only
1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

Table 8-7 - Extended Control Register

R/W	Mode
000	Standard Parallel Port mode. In this mode, the FIFO is reset and common collector drivers are used on the control lines (StrobeJ, AutoFdJ, InitJ and SelectInJ). Setting the direction bit will not tri-state the output drivers in this mode.
001	PS/2 Parallel Port mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010	Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011	ECP Parallel Port Mode. In the forward direction(0), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (1), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register CR4. All drivers have active pull-ups (push-pull)
101	Reserved
110	Test Mode. In this mode, the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

OPERATION

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001) hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched to mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode, the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO, it may have acquired loose data that will be eliminated. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert AutoFdJ independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:
. Set Direction = 0, enabling the drivers.
. Set strobe = 0, causing the StrobeJ signal to default to the deasserted state.
. Set autoFd = 0, causing the AutoFdJ signal to default to the deasserted state.
. Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ECPAFIFO or ECPDFIFO respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

Termination from ECP Mode

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be changed into the forward direction.

Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8-bit data or 8-bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8-bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low.
The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 8-8

Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0x00 only)
1	Channel Address (0-127)

Data Compression

The M512x supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. a run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition

The drivers for StrobeJ, AutoFdJ, InitJ and SelectlnJ are open-collector in mode 000 and are push-pull in all other modes.

ISA Connections

The interface can never stall causing the host to hang. The width of data transfers if strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section.) Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

Interrupts

The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.

An interrupt is generated when :

1. For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC is received.

2. For Programmed I/O:
a. When serviceIntr is 0, dmaEn is 0, direction is 0 and ther are writeIntr Threshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntr Threshold or more free bytes in the FIFO.

b. (1) When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntr Threshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntr Threshold or more bytes in the FIFO.

3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.

4. When ackIntEn is 1 and the nAck signal transitions from a low to a high.

FIFO Operation

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Model. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or PDRQ depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e.2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting PDACKJ and addresses need not be valid. PINTR is generated when a TC is received. PDRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until PDACKJ is deasserted for a minimum of 350 nsec. (**Note**: The only way to properly terminate DMA transfers is with a TC.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode - Transfers from the FIFO to the Host

(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it turns out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP activates the PDRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the PDRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by PDACKJ), indicating that no more data is required. PDRQ goes inactive after PDACKJ goes active for the last byte of a data transfer (or on the active edge of IORJ, on the last byte, if no edge is present on PDACKJ). If PDRQ goes inactive due to the FIFO going empty, then PDRQ is active again as soon as there is one byte in the FIFO. If PDRQ goes inactive due to the TC, then PDRQ is active again when there is one byte in the FIFO, and serviceIntr has been re-enabled. (Note: A data underrun may occur if PDRQ is not removed in time to prevent an unwanted cycle.)

Programmed I/O Mode or Non-DMA Mode

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000h or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. to use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the PINTR point. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

Programmed I/O - Transfers from the FIFO to the Host

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntr Threshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntr Threshold bytes may be read from the FIFO in a single burst.

Programmed I/O - Transfers from the Host to the FIFO

In the forward direction, an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit need to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

The FIFO threshold value is selected via <THR> = <CRA bit7-4>

The readIntr Threshold = {
16 data bytes FIFO, if <THR>=0
<THR> data bytes FIFO, if <THR>=1 to 15

For example, if the <THR>=4, then the serviceIntr is set whenever there are 4-16 bytes in the FIFO

The writeIntr Threshold = {
16 free bytes FIFO, if <THR>=0
<THR> free bytes FIFO, if <THR>=1 to 15

For example, if the <THR>=4, then the serviceIntr is set whenever there are 4-16 bytes free in the FIFO.

Section 9 : Common I/O Ports

The M512x has 22 independently programmable common I/O ports (CIO). Each CIO port is represented as a bit in one of three 8-bit registers, CIO1, CIO2 or CIO3. Only 6 bits of CIO2 are implemented. Each CIO port and its alternate function is listed in table below.

CIO Port	Alternate Function	Register Assignment
CIO10	Interrupt Steering	CIO1, bit 0
CIO11	Interrupt Steering	CIO1, bit 1
CIO12	IRRX Input	CIO1, bit 2
CIO13	IRTX Output	CIO1, bit 3
CIO14	GATEA20 Output	CIO1, bit 4
CIO15	RC Reset Output	CIO1, bit 5
CIO16	I^2C Interface CLK Output	CIO1, bit 6
CIO17	I^2C Interface DATA I/O	CIO1, bit 7
CIO20		CIO2, bit 0
CIO21		CIO2, bit 1
CIO22		CIO2, bit 2
CIO23		CIO2, bit 3
CIO24		CIO2, bit 4
CIO25	Keylock Input	CIO2, bit 5
CIO30	KBC clock source Input	CIO3, bit 0
CIO31	CS0J Output	CIO3, bit 1
CIO32	CS1J Output	CIO3, bit 2
CIO33	ALT_KCLK I/O	CIO3, bit 3
CIO34	ALT_KDAT I/O	CIO3, bit 4
CIO35	ALT_MCLK I/O	CIO3, bit 5
CIO36	ALT_MDAT I/O	CIO3, bit 6
CIO37	ALT_KBC select Input	CIO3, bit 7

CIO registers CIO1, CIO2 and CIO3 can be accessed by the host when the chip is in the normal run mode; i.e., not in the configuration mode. The host uses an index and data register to access the CIO registers. The power on default index and data registers are 0xEA and 0xEB respectively. When the chip is in configuration mode, these index and data registers are used to access the internal configuration registers. In configuration mode, the index address may be programmed to reside on address 0xE0, 0xE2, 0xE4 or 0xEA. The data address is automatically set to the index address + 1. Upon exiting the configuration mode, the new Index and Data registers are used to access registers CIO1, CIO2 and CIO3.

To access the CIO1 register the host should first make sure the chip is in the normal (run) mode. Then it should perform an IOW of 0x01 to the Index register (at 0xEX) to select CIO1 and then read or write the Data register (at Index+1) to access the CIO1 register.
To access CIO2 the host should perform an IOW of 0x02 to the Index register and then access CIO2 through the Data register.

To access CIO3 the host should perform an IOW of 0x03 to the Index register and then access CIO3 through the Data register.

Register	Address	Normal (Run) Mode			Config Mode
Index	0xE0,0xE2, 0xE4,0xEA	0x01	0x02	0x03	0x00-0xFF
Data	0xE1,0xE3, 0xE5,0xEB	access to CIO1	access to CIO2	access to CIO3	access to internal Config registers

CIO ports can assume alternate functions such as input-type, output-type or I/O type. The CIO port structure for each type is illustrated in the following figures.

Common I/O Configuration Registers

Assigned to each CIO port is an 8-bit CIO configuration register which is used to independently program each I/O port. The CIO configuration registers are only accessible when the M512x is in the configuration mode. Configuration section of this specification contains more details.

Reading and Writing CIO Ports

When a CIO port is programmed as an input, reading it through the CIO register latches either the inverted or non-inverted logic value present at the CIO pin; writing to it has no effect. When a CIO port is programmed as an output, the logic value written into the CIO register is either output to or inverted to the CIO pin; when read the result will reflect the contents of the CIO register bit. This is summarized in Table 9-1.

Table 9-1 - CIO Read/Write Behavior

Host Operation	CIO Input Port	CIO Output Port
Read	latched value of CIO pin	bit value in CIO register
Write	no effect	bit placed in CIO register

GATEA20

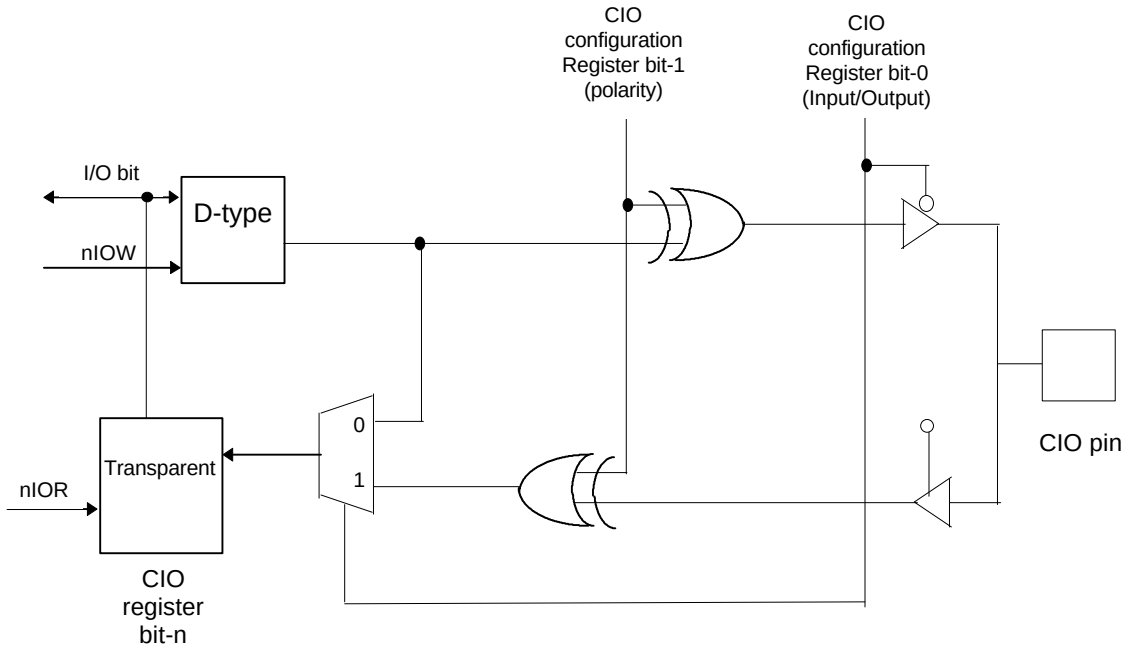
GateA20 is an internal signal from the Keyboard controller (Port 21). The M512x may be configured to drive this signal onto CIO14 by programming its CIO configuration register.

KBC RC Reset

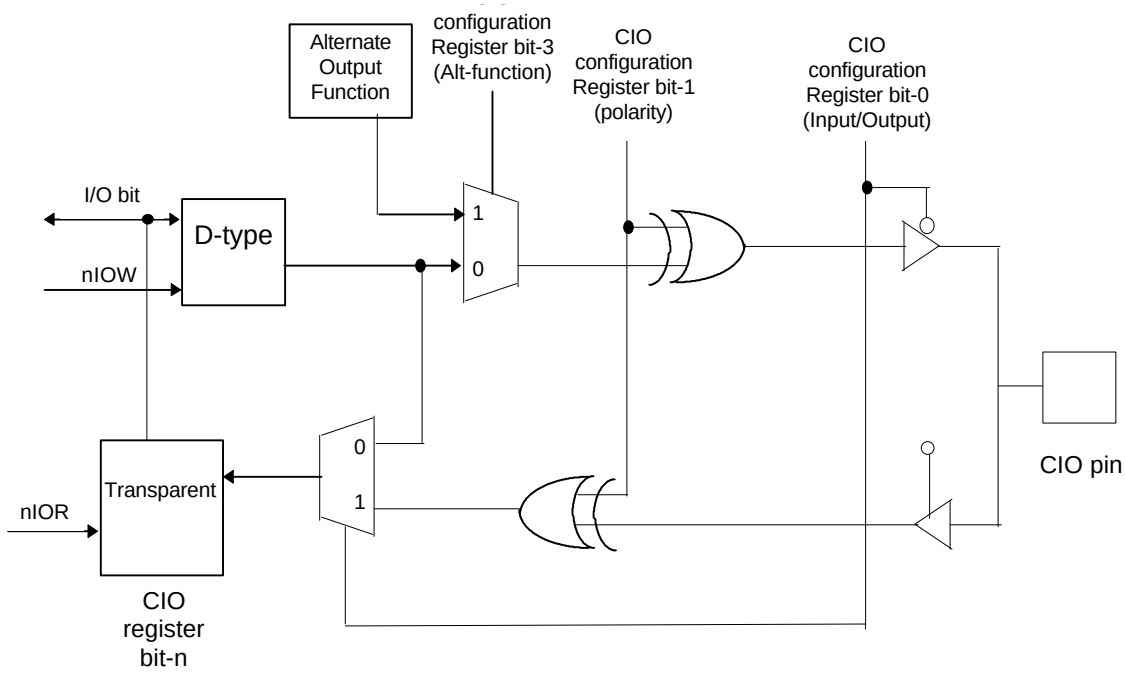
KBC RC is an internal signal from the Keyboard controller (Port 20). The M512x may be configured to drive this signal onto CIO15 by programming its CIO configuration register.

The M512x provides a set of flexible Input/Output control functions to the system designer through a set of Common I/O pins (CIO). These CIO pins may perform simple I/O or may be individually configured to provide a predefined alternate function. Power on reset configures all CIO pins as simple non-inverting inputs.

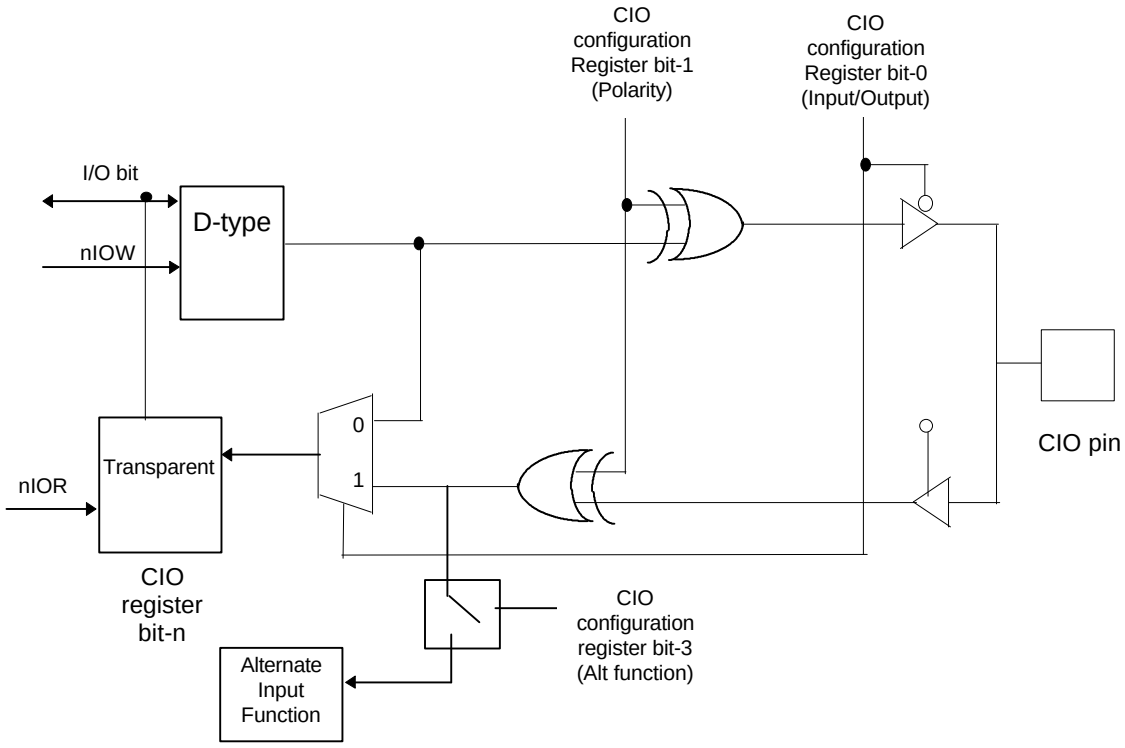
There are four types of CIO ports as shown in following figures :



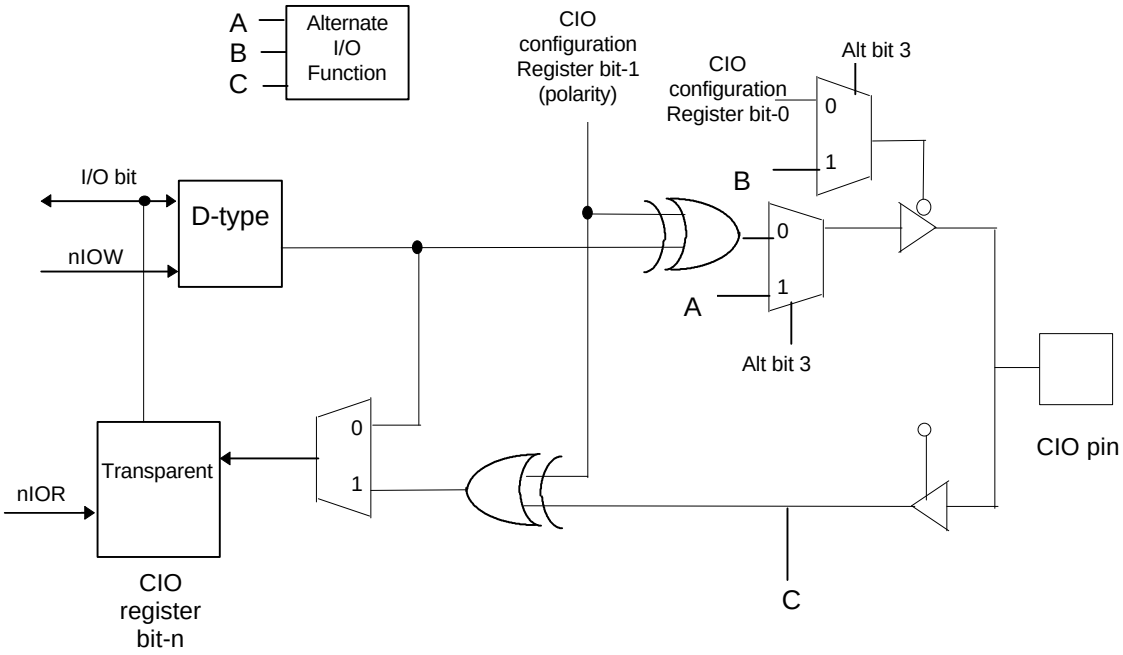
CIO having no alternate function (CIO20-CIO24)



CIO having an output-type alternate function. (CIO13, CIO14, CIO15, CIO16, CIO31, CIO32)



CIO having an input-type alternate function (CIO10, CIO11, CIO12, CIO30, CIO37, CIO25)



CIO having an I/O type alternate function (CIO17, CIO33, CIO34, CIO35, CIO36)

Section 10 : Electrical Characteristics

10.1 Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics. Unless otherwise specified, all voltages are measured with respect to ground.

Table 10-1 Absolute Maximum Ratings

Item	Ratings
Supply voltage VDD Operating supply voltage	-0.5V to +7V 4.5V to 5.5V
All input and output voltages with respect to VSS	-0.5V to VCC +0.5V
Storage temperature range (TSTG)	-65^{o}C to 150^{o}C
Operating temperature (TA)	0^{o}C to 70^{o}C
Package power dissipation (PD)	750 mW
Lead temperature (TL) (soldering, 10 seconds)	260^{o}C
|VCC - VCCA|	0.6V
ESD tolerance (CZAP)	100 pF

10.2 DC Characteristics

V_{DD} = 5.0V ± 5%, V_{SS} = 0V, unless otherwise specified. These values are measured under static conditions, and not under dynamic conditions.

Table 10-2 DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	High level input voltage	Except OSC1/CLK	2.0	VCC	V
VIL	Low level input voltage	Except OSC1/CLK	-0.5	0.8	V
IIN	Input current	Except OSC pins, VIN = VDD or GND		±1.0	uA
ICCA	Average VDDA supply current	VIN = 2.4V or 0.5V, I/O = 0 mA*		10	mA
	Quiescent VDDA supply current in low power mode	VIN = VDD or GND, I/O = 0 mA*		400	uA
ICC	Average VDD supply current	VDD = 5.5V; no loads on the outputs: IORJ, IOWJ, SIN, DSRJ, DCDJ, CTSJ, RIJ = 2V; All other inputs: 0.8V or 2.4V; CLK = 24 MHz; DIVISOR = EFFFh		50	mA
	Quiescent VDD supply current in low power mode	VIN = VDD or GND, I/O = 0 mA*			

Table 10-2 DC Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
Oscillator Pins (OSC1/CLK)					
IOSC	OSC1 input current	(OSC1 = GND), VIN = VDD or GND	±1.6		mA
VIH	OSC1 high level input voltage	OSC2 = GND	2.4		V
VIL	OSC1 low level input voltage	OSC2 = GND		0.4	V
Disk Drive Interface Pins (MTR0~3, DR0~3, WDATA, WGATE, RDATA, DIR, HDSEL, TRK0, WRTPRT, RPM, STEP, DSKCHG, INDEX)					
VH	Input hysteresis		250 typical		mV
VOL	Low level output voltage	IOUT = 36 mA		0.4	V
ILKG	Output high leakage current	VOUT = VDD or GND		±100	uA
VIH	High level input voltage		2.2		V
VIL	Low level input voltage			0.8	V
Microprocessor and Parallel Port Pins					
VOL	Output low voltage	IOL = 24 mA on D0~D7; 16 mA on PD0~PD7; 16 mA on INITJ, AFDJ, STBJ and SLINJ; 4 mA on all other outputs		0.4	V
VOH	Output high voltage	IOH = -12 mA on D0~D7; -16 mA on PD0~PD7; -16 mA on INITJ, AFDJ, STBJ and SLINJ; -4 mA on all other outputs	2.4		V
IIL	Input leakage	VDD = 5.5V, VSS = 0V All other pins floating		±10	uA
IOZ	Output tri-state leakage	VDD = 5.5V, VSS = 0V VOUT = 0V, 5.5V		±20	uA

* I_{CC} is measured with a 0.1 uF supply decoupling capacitor-to-ground.

10.2.1 Capacitance

$T_A = 25^oC$, $V_{DD} = V_{SS} = 0V$)

Table 10-3 Capacitance

Symbol	Parameter	Conditions	Typ	Max	Units
CIN	Input capacitance	fC = 1 MHz; Unmeasured	5	7	pF
COUT	Output capacitance	pins returned to VSS	6	8	pF
CI/O	I/O capacitance		10	12	pF

10.3 AC Characteristics

T_A = 0°C to +70°C, V_{DD} = +5V ± 5%.

All AC timings can be met with current loads that do not exceed 3.2 mA or -8 uA at 100 pF capacitive loading. For capacitive loads that exceed 100 pF, the following typical derating factors should be used:

100 pF < C_L ≤150 pF, t = (0.10 ns/pF) (C_L - 100 pF) typical
150 pF < C_L ≤ 200 pF, t = (0.08 ns/pF) (C_L - 100 pF) and
t = (0.5 ns/mA) (I_{SINK} mA) or t = -(0.5 ns/mA) (I_{SOURCE} mA)
t_{SOURCE} is always negative, I_{SINK} ≤4.8 mA, I_{SOURCE} ≤ -120 uA, C_L ≤ 250 pF.

Table 10-4 lists the AC Characteristics of the M512x.

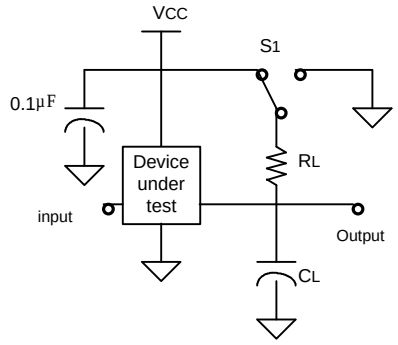
Table 10-4 AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
tAR	Delay from address to IORJ		19		ns
tAW	Delay from address to IOWJ		19		ns
tCH	Duration of clock high pulse	see Note A	16		ns
tCL	Duration of clock low pulse	see Note A	16		ns
tDH	Data hold time		10		ns
tDS	Data setup time		19		ns
tHZ	IORJ to floating data delay	see Note B	13		ns
tRA	Address hold time from IORJ		0		ns
tRC	Read cycle update		36		ns
tRD	IORJ strobe width		60		ns
tTPS	Port setup		13		ns
tRI	Read strobe to clear IRQ6			52	ns
tRVD	Delay from IORJ to data			31	ns
tRW	Reset pulse width		100		ns
tWA	Address hold time from IOWJ		0		ns
tWC	Write cycle update		36		ns
tWI	Write strobe to clear IRQ6			52	ns
tWO	Write to output			41	ns
tWR	IOWJ strobe width		50		ns
RC	Read cycle = tAR + tRD + tRC		115		ns
WC	Write cycle = tAW + tWR + tWC		105		ns

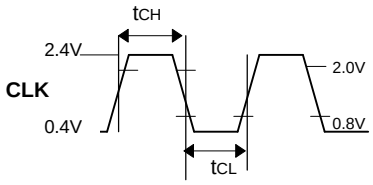
Note: *A. External clock (24 MHz maximum).*
B. Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

10.4 AC Test Conditions

In Table 10-5, C_L = 100 pF. This includes jig and scope capacitance. S1 is open for push-pull outputs. S1 is equal to V_{CC} for high impedance to active low, and active low to high impedance measurements. S1 is equal to GND for high impedance to active high, and active high to high impedance measurements. R_L = 1.0 kohm for CPU interface pins. For the open drain drive interface pins S1 = V_{CC} and R_L = 150 ohms.



External Clock Input (24 MHz)



The 2.4V and 0.4V levels are the voltages tthat tthe inputs are driven to during AC testing

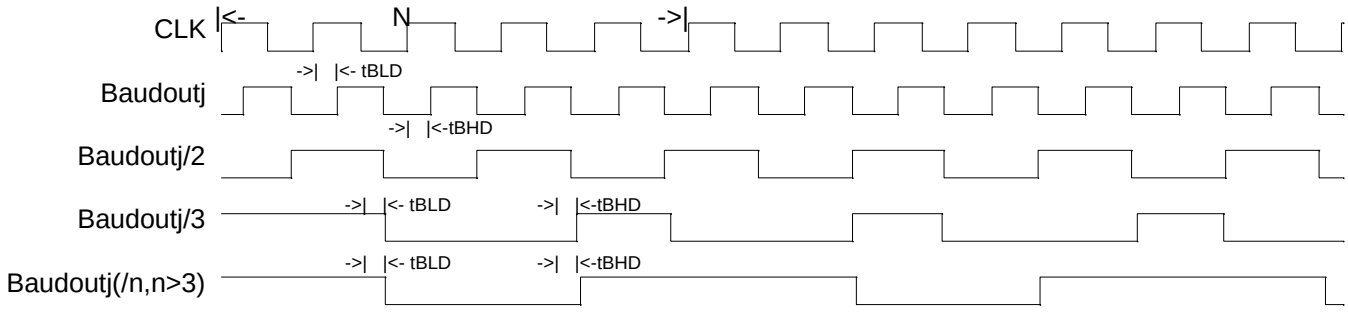
Table 10-5 AC Test Conditions

Input pulse levels	GND to 3.0V
Input rise and fall times	6 ns
I/O reference levels	1.3V
Tri-state reference levels	Active high - 0.5V Active low + 0.5V

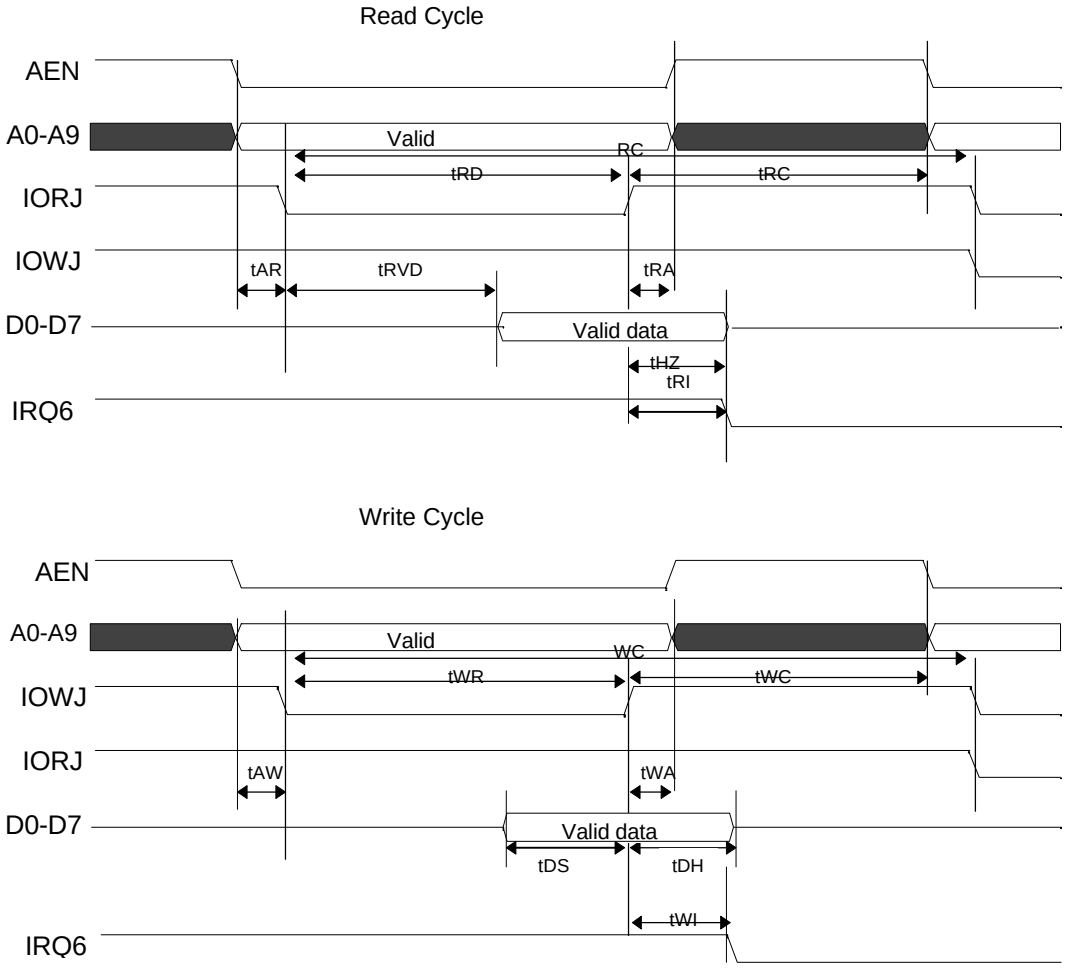
Table 10-6 Serial Interface Baud Generator

Symbol	Parameter	Conditions	Min	Max	Unit
N	Baud Divisor		12^{16} - 1		
t_{BHD}	Baud output positive edge delay	CLK = 24 MHz / 2, 100 pF load		56	ns
t_{BLD}	Baud output negative edge delay	CLK = 24 MHz / 2, 100 pF load		56	ns

BAUDOUTJ Timing



CPU Interface



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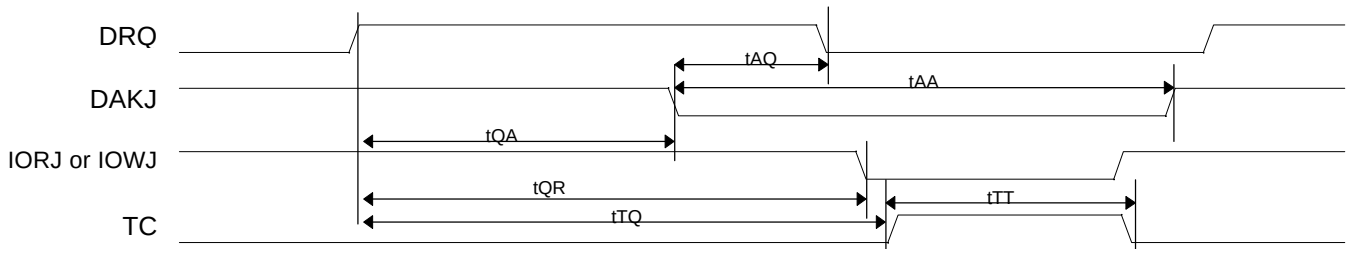
DMA Timing

DMA acknowledge is sufficient to acknowledge a data transfer. Read or write strobes are necessary only if data is presented to the data bus. If read/write strobes are applied, then the read/write strobes and the acknowledge must be removed within 1 *us* of each other.

Table 10-7 DMA Timing

Symbol	Parameter	Min	Max	Unit
t_{AA}	DAK pulse width	60		ns
t_{AQ}	End of DRQ from DAK		92	ns
t_{QA}	DAK assertion from DRQ	8		ns
t_{QR}	DRQ to read or write strobe	8		ns
t_{TQ}	Time after last DRQ that TC must be asserted		Note	ns
t_{TT}	TC strobe width	40		ns

Note: *The terminal count pin (TC) terminates the data transfer operation. There are several constraints placed on the timing of TC. 1) TC is enabled by DAKJ, so TC must be pulsed while DAKJ is low. 2) TC must occur before ((1/data rate x 8) - 1 us). Data rate is the exact data transfer rate being used.*

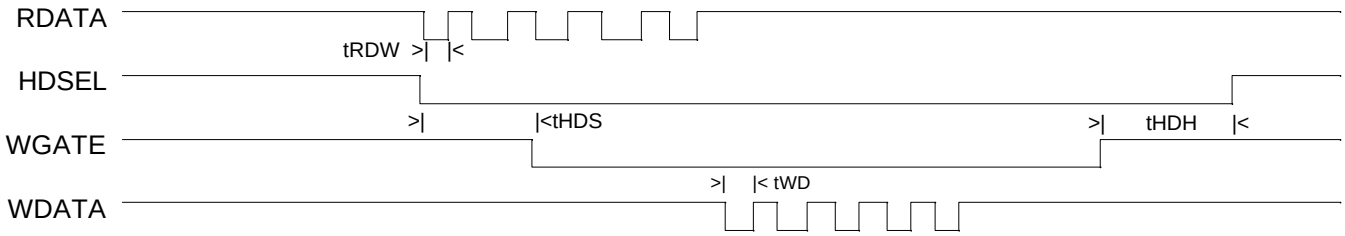


Drive Read and Write Timing

Table 10-8 Drive Read and Write Timing

Symbol	Parameter	Conditions	Min	Unit
t_{RDW}	Read-data pulse-width		25	ns
t_{WD}	Write-data pulse-width	250 kb/s (MFM)	500	ns
t_{HDS}	Head-select setup to write-gate-assertion		40	us
t_{HDH}	Head-select hold from write-gate		12	ns
	300 kb/s (MFM)	416	ns	
	500 kb/s (MFM)	250	ns	
	1000 kb/s (MFM)	225	ns	

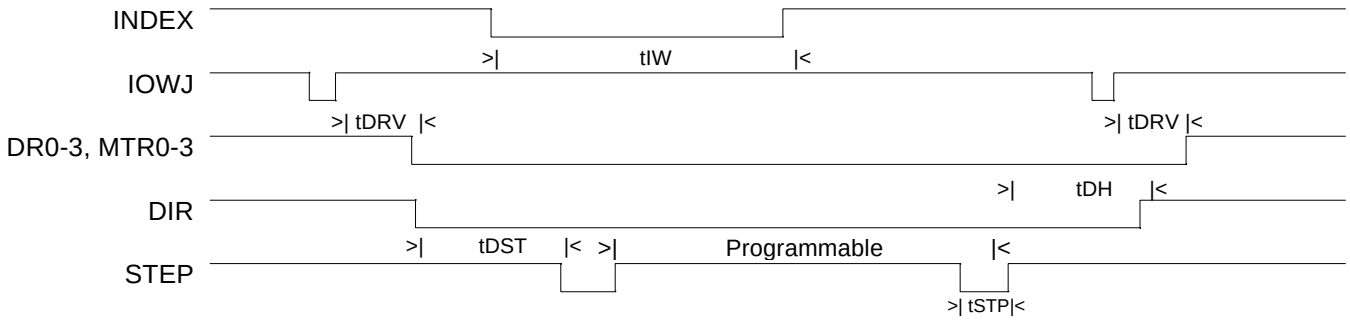
Note : *Whenever WGATE is asserted, the WDATA line is active. At the end of each write, one dummy byte is written before WGATE is deasserted.*



Drive Track Access Timing

Table 10-9 Drive Track Access Timing

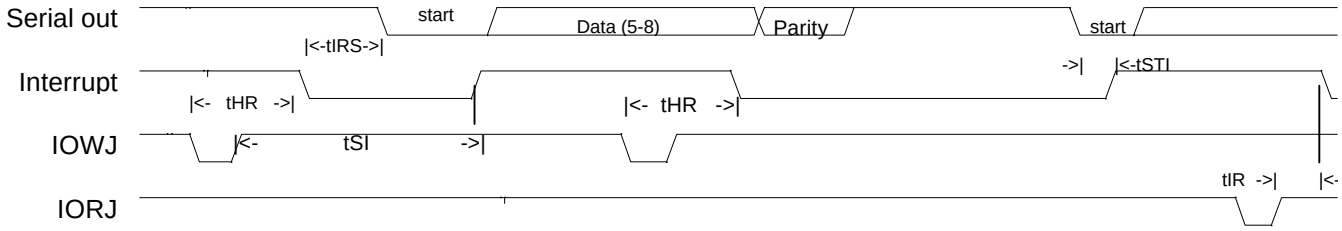
Symbol	Parameter	Min	Max	Unit
t_{DH}	Direction hold from end-of-step	1 step time		
t_{DRV}	Drive-select or motor-time from write-strobe		100	ns
t_{DST}	Direction-setup prior to step	6		us
t_{IW}	Index pulse-width	100		ns
t_{STP}	Step pulse-width	8		us



Transmitter

Table 10-10 Transmitter

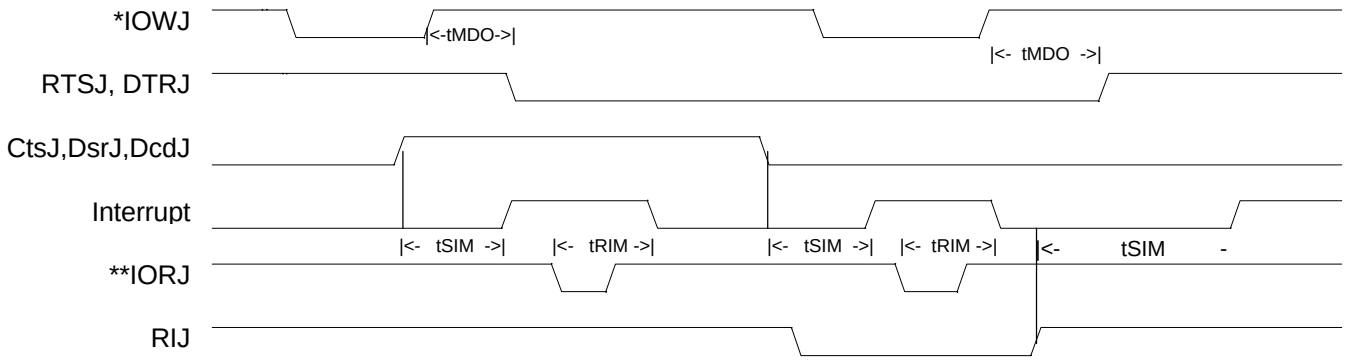
Symbol	Parameter	Min	Max	Unit
t_{HR}	Delay from IOWJ (WR THR) to reset interrupt		50	ns
t_{IR}	Delay from IORJ (RD IIR) to reset interrupt (THRE)		50	ns
t_{IRS}	Delay from initial INTR reset to transmit start	8	24	Baudout cycles
t_{SI}	Delay from initial write to interrupt	16	24	Baudout cycles
t_{STI}	Delay from start to interrupt (THRE)		8	Baudout cycles



Modem Control

Table 10-11 Modem Control

Symbol	Parameter	Max	Unit
t_{MDO}	Delay from IOWJ (WR MCR) to output	50	ns
t_{RIM}	Delay to reset interrupt from IORJ (RD MSR)	98	ns
t_{SIM}	Delay to set interrupt from modem input	50	ns

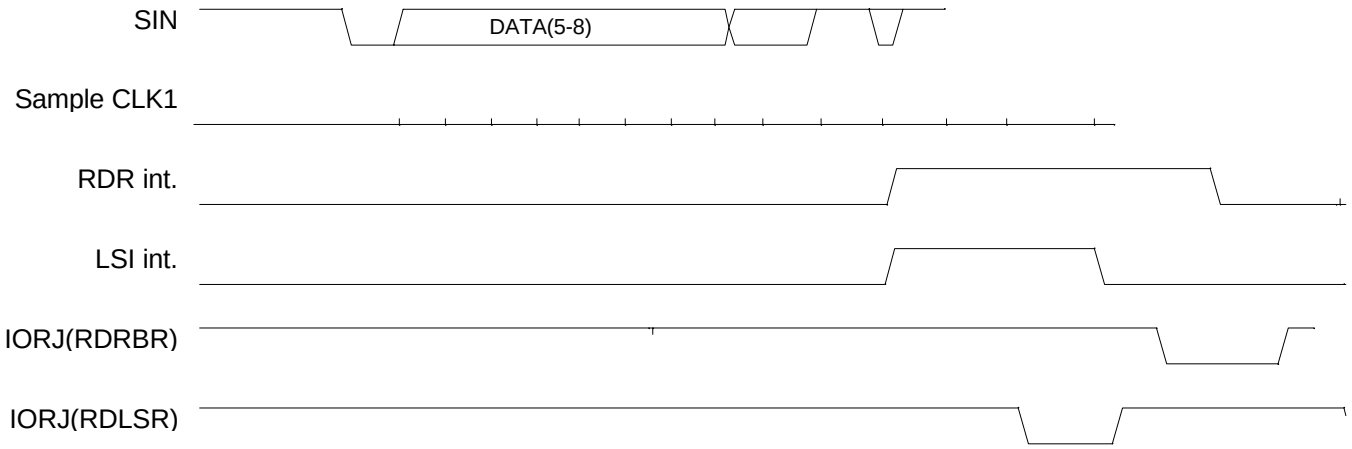


* : See Write Cycle Timing ** : See Read Cycle Timing

Receiver

Table 10-12 Receiver

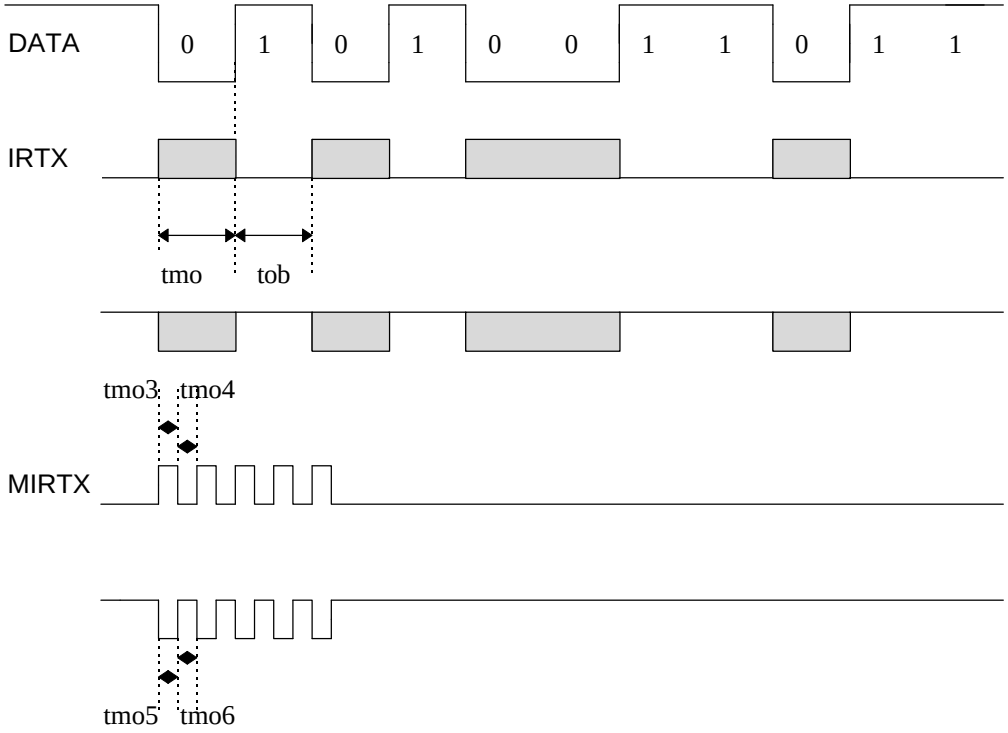
Symbol	Parameter	Max	Unit
t_{RAI}	Delay from active edge of IORJ to reset interrupt	98	ns
t_{RINT}	Delay from inactive edge of IORJ (RD LSR) to reset interrupt	50	ns
t_{SCD}	Delay from R_{CLK} to sample time	41	ns
t_{SINT}	Delay from stop to set interrupt	2	Baudout cycles



Amplitude Shift Keyed IR Transmit Timing

Table 10-13. ASK IR Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
tmo	Modulated output bit time				us
tob	Off bit time				us
tmo3	Modulated output "on"	0.79	1	1.21	us
tmo4	Modulated output "on"	0.79	1	1.21	us
tmo5	Modulated output "on"	0.79	1	1.21	us
tmo6	Modulated output "off"	0.79	1	1.21	us



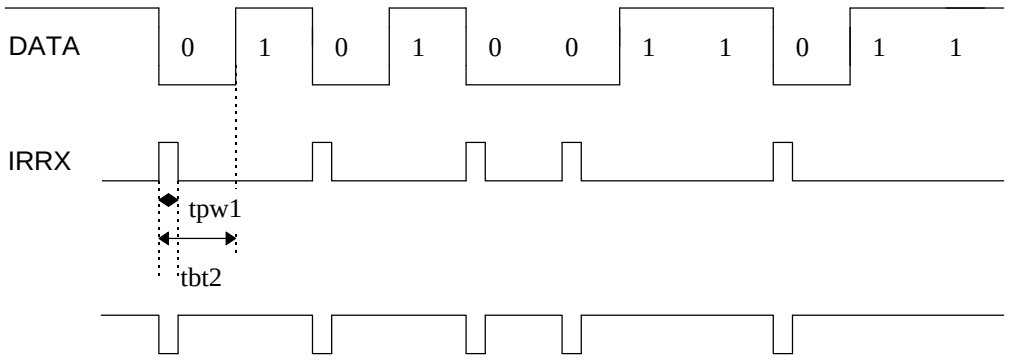
Notes :

1. t1, t2 timing referred to IrDA Transmit Timing @ each baud rate.
2. UART1, UART2 0xF1 bit 1: 1 = receive active low
   0 = receive active high (default)
3. MIRTX are the modulated outputs. (500k)

IrDA Receive Timing

Table 10-14. IrDA Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
tpw1	Pulse width at 115k baud	1.40	1.60	2.71	us
tpw1	Pulse width at 57.6k baud	1.40	3.22	3.69	us
tpw1	Pulse width at 38.4k baud	1.40	4.80	5.53	us
tpw1	Pulse width at 19.2k baud	1.40	9.70	11.07	us
tpw1	Pulse width at 9.6k baud	1.40	19.50	22.13	us
tpw1	Pulse width at 4.8k baud	1.40	39.00	44.27	us
tpw1	Pulse width at 2.4k baud	1.40	78.00	88.55	us
tbt2	Bit time at 115k baud		8.68		us
tbt2	Bit time at 57.6k baud		17.40		us
tbt2	Bit time at 38.4k baud		26.00		us
tbt2	Bit time at 19.2k baud		52.00		us
tbt2	Bit time at 9.6k baud		104.00		us
tbt2	Bit time at 4.8k baud		208.00		us
tbt2	Bit time at 2.4k baud		416.00		us



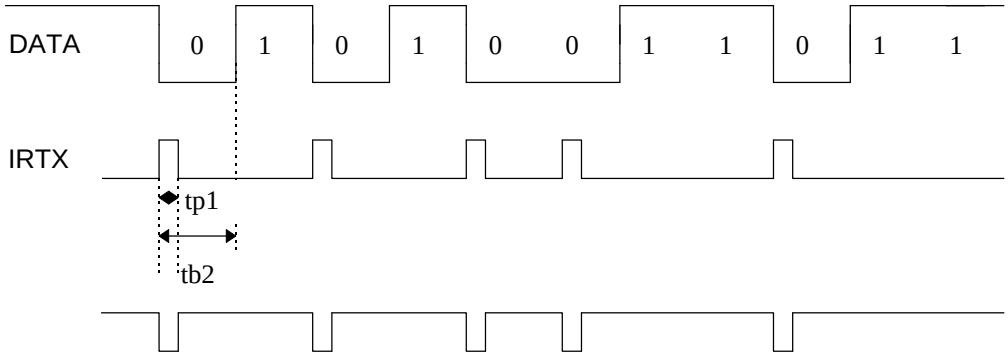
Notes :

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. UART1, UART2 0xF1 bit 0 : 1 = receive active low
   0 = receive active high (default)

IrDA Transmit Timing

Table 10-15. IrDA Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
tp1	Pulse width at 115k baud	1.39	1.60	2.72	µs
tp1	Pulse width at 57.6k baud	1.39	3.22	3.70	µs
tp1	Pulse width at 38.4k baud	1.39	4.80	5.54	µs
tp1	Pulse width at 19.2k baud	1.39	9.70	11.08	µs
tp1	Pulse width at 9.6k baud	1.39	19.50	22.14	µs
tp1	Pulse width at 4.8k baud	1.39	39.00	44.28	µs
tp1	Pulse width at 2.4k baud	1.39	78.00	88.56	µs
tb2	Bit time at 115k baud	-	8.68	-	µs
tb2	Bit time at 57.6k baud	-	17.40	-	µs
tb2	Bit time at 38.4k baud	-	26.00	-	µs
tb2	Bit time at 19.2k baud	-	52.00	-	µs
tb2	Bit time at 9.6k baud	-	104.00	-	µs
tb2	Bit time at 4.8k baud	-	208.00	-	µs
tb2	Bit time at 2.4k baud	-	416.00	-	µs



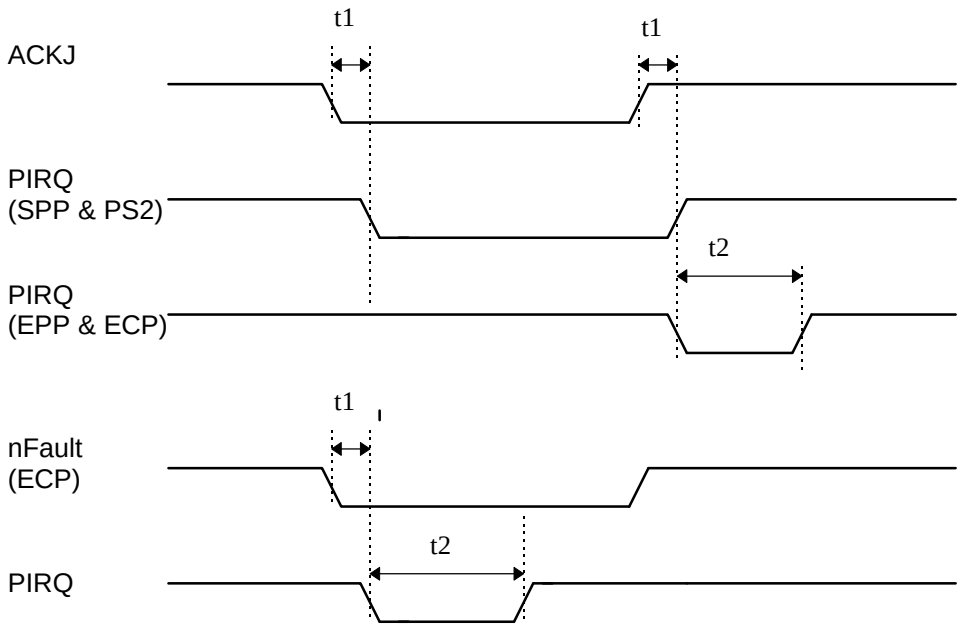
Notes :

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. UART1, UART2 0xF1 bit 1 : 1 = transmit active low
   0 = transmit active high (default)

Parallel Port Interrupt Timing

Table 10-16. Parallel Port Interrupt Timing

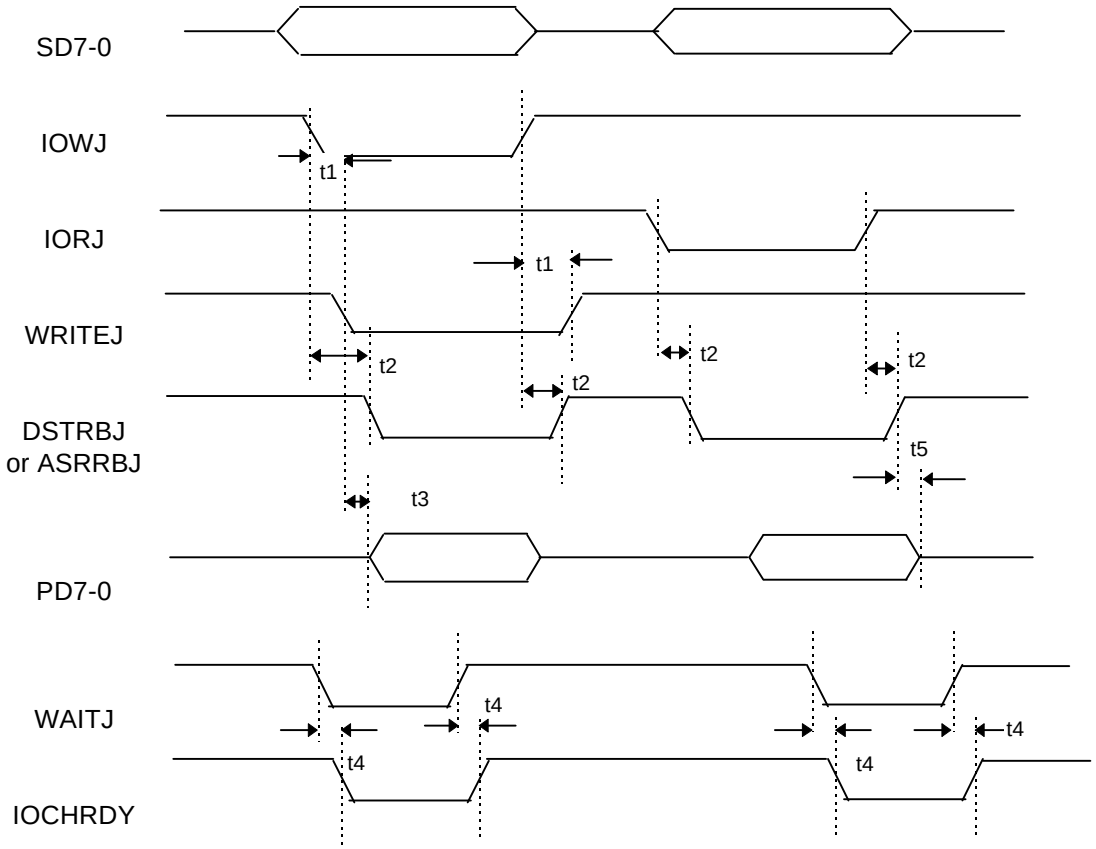
Symbol	Parameter	Min	Typ	Max	Unit
t1	PIRQ delay from ACKJ, nFault			30	ns
t2	PIRQ active in EPP & ECP modes	250		375	ns



EPP Mode Version 1.7 Timing

Table 10-17. EPP Mode Version 1.7 Timing

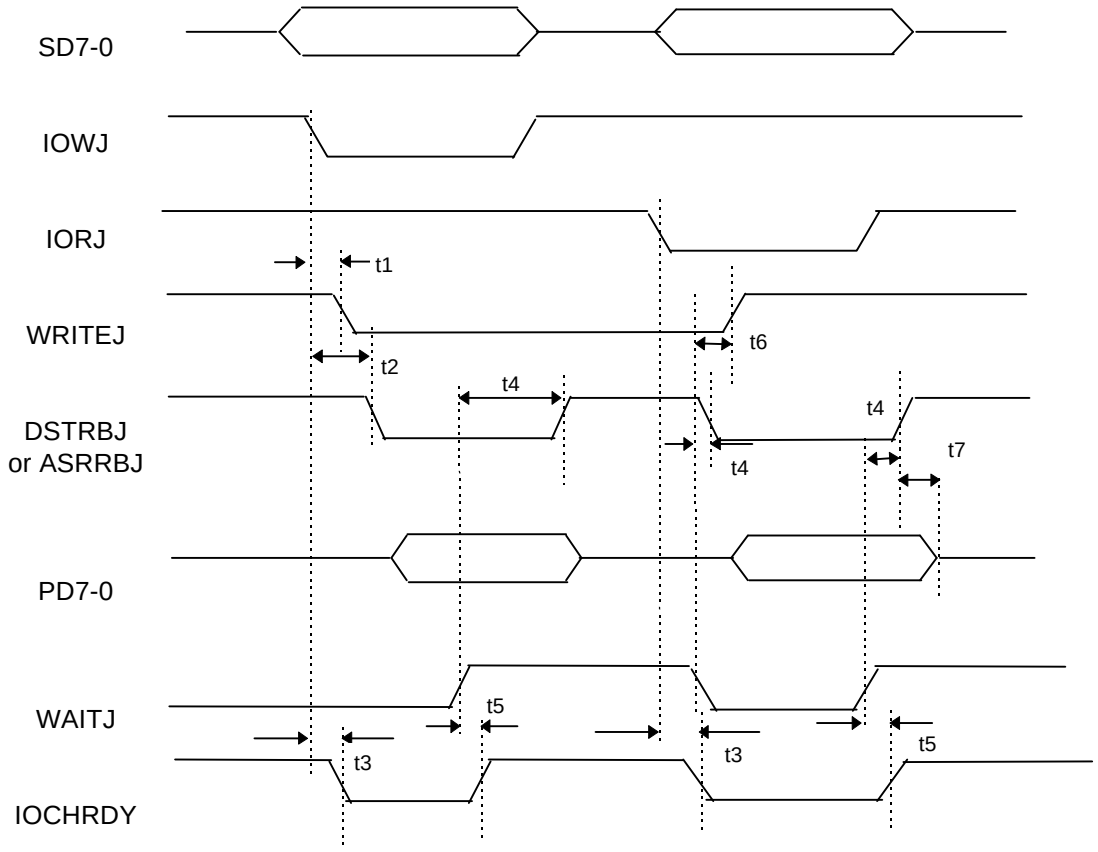
Symbol	Parameter	Min	Typ	Max	Unit
t1	IOWJ active to WRITEJ active			45	ns
t2	IOWJ active to WRITEJ & DSTRBJ/ASTRBJ active			45	ns
t3	WRITEJ active to PD7-0 valid			15	ns
t4	WAITJ active to IOCHRDYJ active			40	ns
t5	DSTRBJ/ASTRBJ inactive to PD7-0 invalid	50			ns



EPP Mode version 1.9 Timing

Table 10-18. EPP Mode version 1.9 Timing

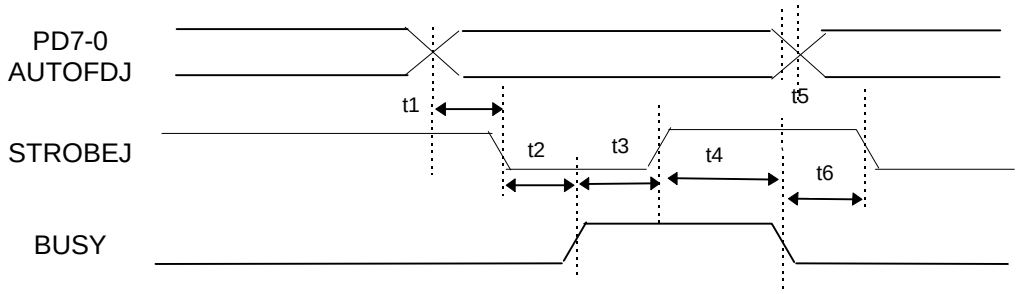
Symbol	Parameter	Min	Typ	Max	Unit
t1	IOWJ active to WRITEJ active			45	ns
t2	IOWJ active to DSTRBJ/ASTRBJ active			65	ns
t3	IOWJ active to IOCHRDY active			40	ns
t4	WAITJ inactive to DSTRBJ/ASTRBJ inactive			105	ns
t5	WAITJ inactive to IOCHRDYJ inactive			40	ns
t6	WAITJ active to WRITEJ inactive			85	ns
t7	DSTRBJ/ASTRBJ inactive to PD7-0 invalid	50			ns



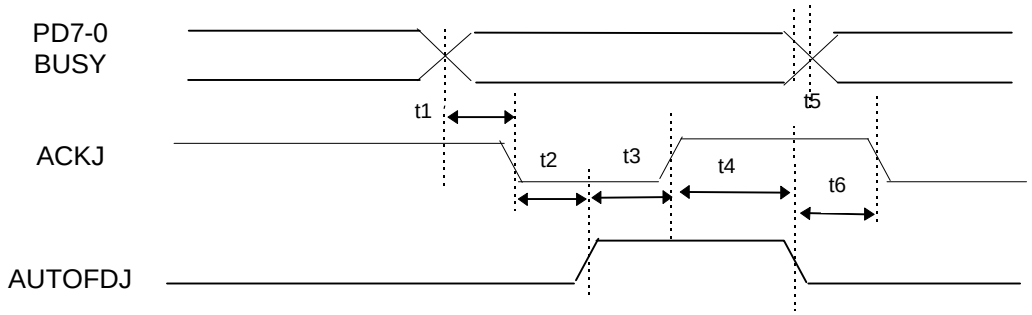
ECP Mode Timing

Table 10-19. ECP Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	DATA valid to STROBEJ active	0			ns
t2	STROBEJ active to BUSY active	0			ns
t3	BUSY active to STROBEJ inactive	75			ns
t4	STROBEJ inactive to BUSY inactive	0		35	ms
t5	BUSY inactive to DATA update	0		1	sec
t6	BUSY inactive to STROBEJ active	0			ns



ECP Forward Timing Diagram

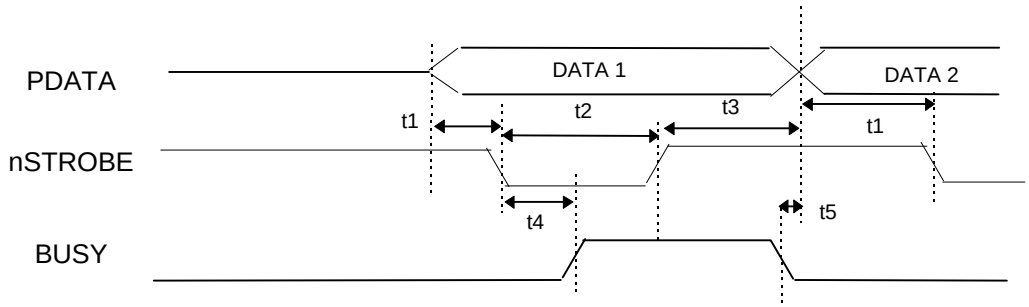


ECP Backward Timing Diagram

Compatible FIFO Mode Timing

Table 10-20. Compatible FIFO Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Data valid to nSTROBE active		500		ns
t2	nSTROBE active pulse width		500		ns
t3	Data hold from nSTROBE inactive		500		ns
t4	nSTROBE active to BUSY active		500		ns
t5	BUSY inactive to PDATA TRANSING	80			ns



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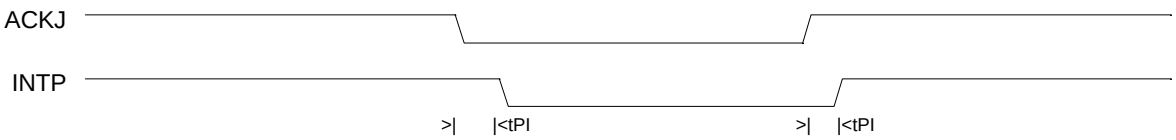
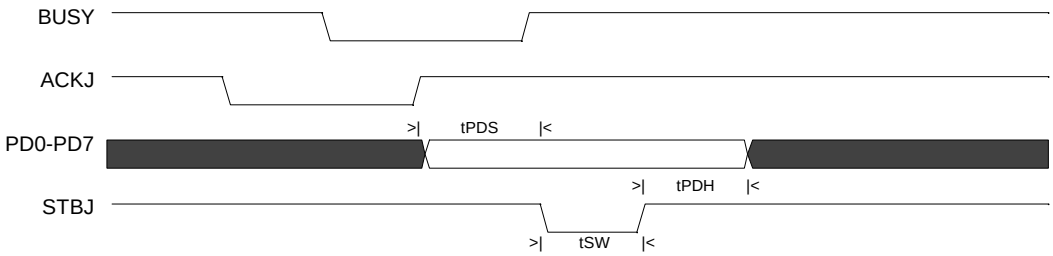
Parallel Interface

Table 10-21. Parallel Interface

Symbol	Parameter Conditions	Min	Max	Unit
t_{PDH}	Port data hold	500		ns
t_{PDS}	Port data setup	500		ns
t_{PI}	Port interrupt	33		ns
t_{SW}	Strobe width	500		ns

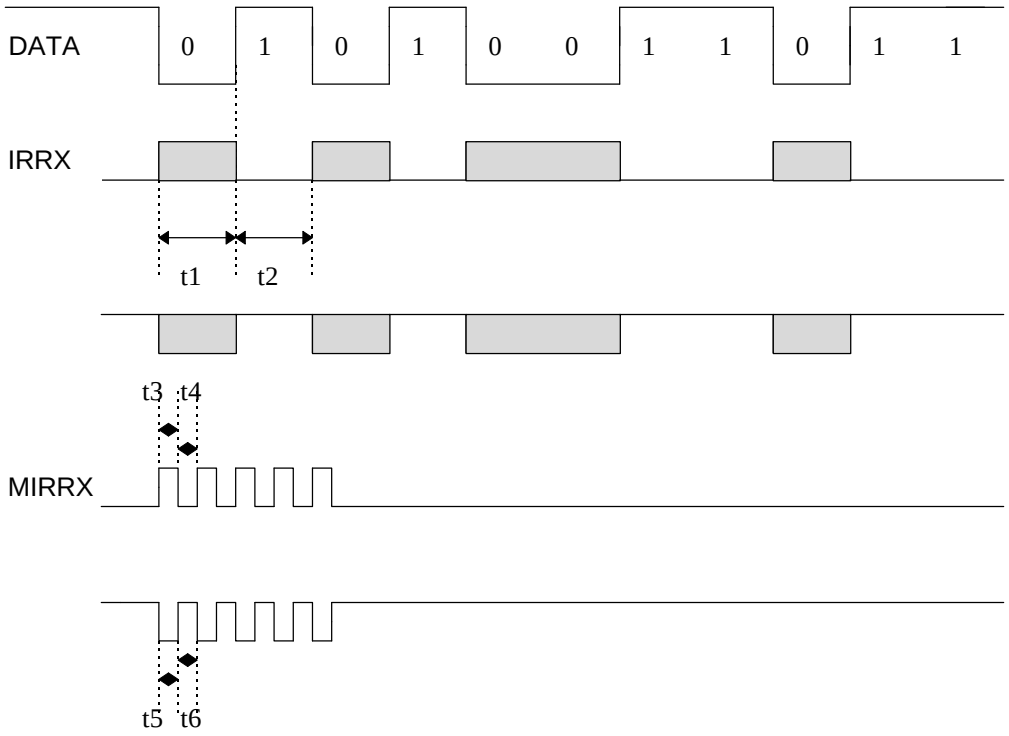


Interrupt Timing



Typical Peripheral Data Exchange

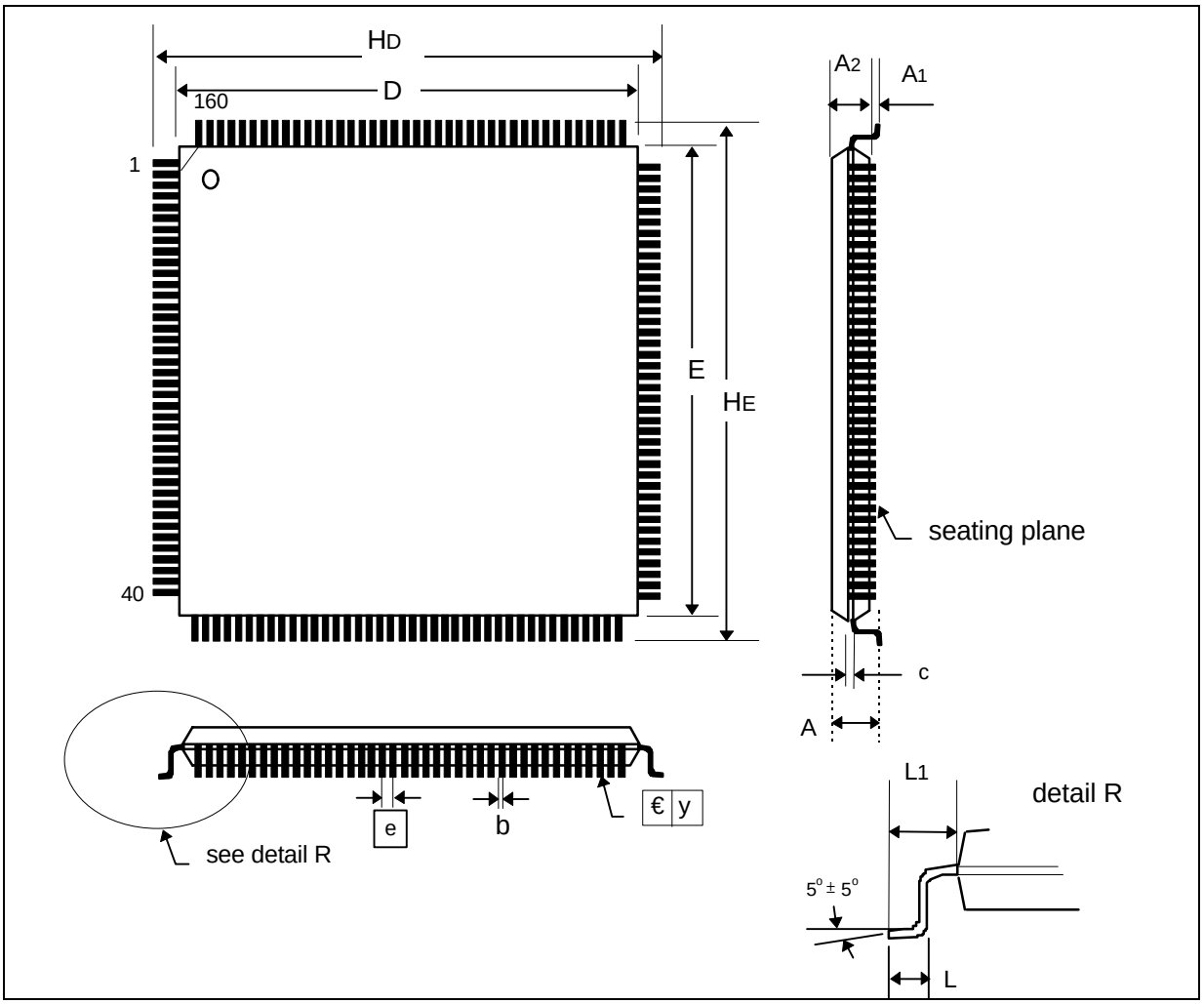
	Parameter	Min	Typ	Max	Unit
t1	Modulated output bit time				µs
t2	Off bit time				µs
t3	Modulated output “on”	0.81	1	1.18	µs
t4	Modulated output “on”	0.81	1	1.18	µs
t5	Modulated output “on”	0.81	1	1.18	µs
t6	Modulated output “off”	0.81	1	1.18	µs



Notes :

1. t1, t2 timing referred to IrDA Receive Timing @ each baud rate.
2. UART1, UART2 0xF1 bit 0 : 1 = receive active low
   0 = receive active high (default)
3. MIRRX are the modulated outputs. (500k)

Section 11 : Packaging Information



Symbol	Dimensions in Millimeters (nom.)	Dimensions in Inches (nom.)
A	3.5 (max)	0.138 (max)
A_1	0.20	0.008
A_2	3.20	0.126
b	0.30	0.012
c	0.15	0.006
D	28.0	1.102
E	28.0	1.102
e	0.65	0.026
H_D	32.0	1.260
H_E	32.0	1.260
L_1	2.01	0.079
L	0.8	0.031
y	0.10	0.004

Section 12 : Ordering Information

Ordering Information

M5123 supports Phoenix KBC

M5125 supports AMI KBC

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Section 13 : Revision History

p.28 **Note** : Drive Table 00 = Regular Drives and 2.88MB
01 = 3-mode drive

p.53 Perpendicular Mode

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