M51272P/FP

NTSC/PAL ENCODER

DESCRIPTION

The M51272P/FP is a semiconductor integrated circuit designed for color signal modulation. It consists of R-Y and B-Y input signal clamp circuits,burst signal mixing,chroma modulator, Y/C mixing amplifier,sync adder and video signal output amplifier.

FEATURES

- Low power dissipation(Vcc=5.0V, Icc=30mA typ.)
- Suitable for both NTSC and PAL.
- Adjustable carrier balance.
- able to mute luminance signal and color individually.
- Built-in 75 ohm load driver.

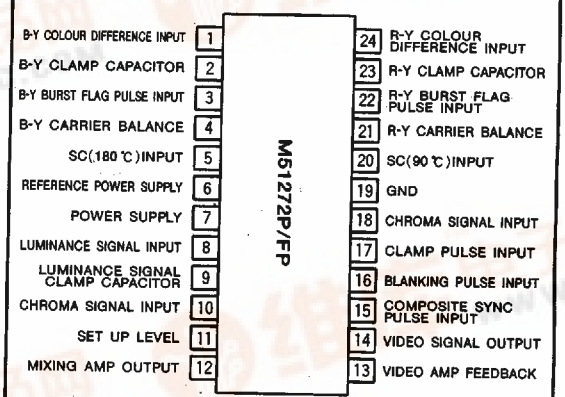
APPLICATION

NTSC/PAL color TV sets and VCR.

RECOMMENDED OPERATING CONDITION

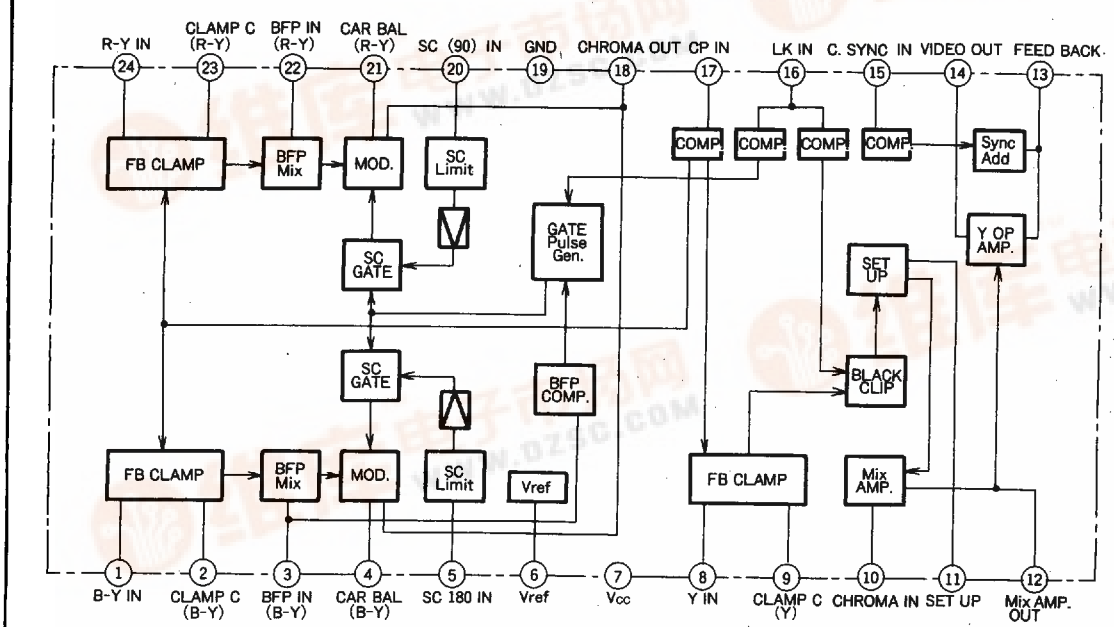
Supply voltage range ..... 4.5~5.5V
Rated supply voltage 5.0V

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D(P)
24P2Q-A(FP)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
Vcc	Supply voltage	6	V
Pd	Power consumption	1000(P)/500(FP)	mW
Topr	Operating temperature	−20~75	℃
Tstg	Storing ambient temperature	−40~125	℃
K_θ	Heat reduction rate	10.0(P)/5(FP)	mW/℃

ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise noted)

DC CHARACTERISTICS

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min.	Typ.	Max.	
Icc	Circuit current	DC bias alone	A	20	30	40	mA
V1	Voltage at terminal 1	DC bias alone		2.1	2.3	2.5	V
V2	Voltage at terminal 2	DC bias alone		1.6	1.8	2.0	V
V3	Voltage at terminal 3	DC bias alone		2.7	2.9	3.1	V
V5	Voltage at terminal 5	DC bias alone		3.4	3.6	3.8	V
V6	Voltage at terminal 6	DC bias alone		2.8	3.0	3.2	V
V8	Voltage at terminal 8	DC bias alone		2.1	2.3	2.5	V
V9	Voltage at terminal 9	DC bias alone		1.6	1.8	2.0	V
V10	Voltage at terminal 10	DC bias alone		2.8	3.0	3.2	V
V12	Voltage at terminal 12	DC bias alone		1.9	2.2	2.5	V
V14	Voltage at terminal 14	DC bias alone		1.7	2.0	2.3	V
V18	Voltage at terminal 18	DC bias alone		2.8	3.1	3.4	V
V20	Voltage at terminal 20	DC bias alone		3.4	3.6	3.8	V
V22	Voltage at terminal 22	DC bias alone		2.7	2.9	3.1	V
V23	Voltage at terminal 23	DC bias alone		1.6	1.8	2.0	V
V24	Voltage at terminal 24	DC bias alone		2.1	2.3	2.5	V

INPUT TERMINAL CHARACTERISTICS

Pin No.	Input from	Internal bias voltage (standard)	Test conditions	Input resistance or current standard value			Unit
				Min.	Typ.	Max.	
①	Resistor	2.3V	—	15	20	25	KΩ
③	Resistor	2.9V	—	1.5	2	2.5	KΩ
④	Open base (NPN)	Not specified	V4=3V	—	1	2	μA
⑤	Resistor	3.6V	—	7.5	10	12.5	KΩ
⑧	Resistor	2.3V	—	15	20	25	KΩ
⑩	Resistor	3.0V	—	4.5	6	7.5	KΩ
⑪	Open base (NPN)	Not specified	V11=5V	—	3	6	μA
⑮	Open base (NPN)	Not specified	V15=5V	—	1	2	μA
⑯	Open base (PNP) (NPN)	Not specified	V16=5V	—	0.5	1	μA
			V16=0V	−4	−2	—	
⑰	Open base (NPN)	Not specified	V17=5V	—	1	2	μA
⑳	Resistor	3.6V	—	7.5	10	12.5	KΩ
㉑	Open base (NPN)	Not specified	V21=3V	—	1	2	μA
㉒	Resistor	2.9V	—	1.5	2	2.5	KΩ
㉔	Resistor	2.3V	—	15	20	25	KΩ

OUTPUT TERMINAL CHARACTERISTICS

Pin No.	Output from	Test conditions	Bias current			Unit
			Min.	Typ.	Max.	
⑫	Emitter follower (NPN)	Ammeter between 12 pin and Vcc	160	200	240	μA
⑱	Emitter follower (NPN)	Ammeter between 18 pin and Vcc	1.3	1.6	1.9	mA

AC CHARACTERISTICS

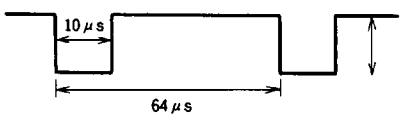
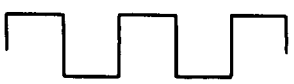
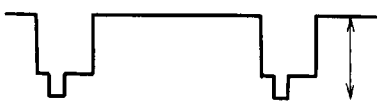
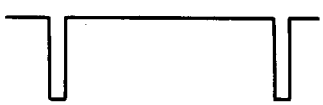
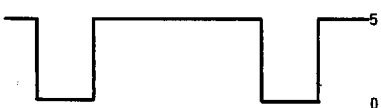
Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min.	Typ.	Max.	
$V_{CC}R$	Operating supply voltage range		There Shall not be any abnormal operation in the standard application circuit		4.0	5.0	6.0	V
CBb	B-Y	Carrier balance DC voltage	Pin4 terminal voltage shall be variable. Carrier leakage shall be minimum.	B	2.9	3.0	3.1	V
Gmb	B-Y	Demodulation output	SG1 200mV$_{P-P}$ input	B	500	600	700	mV$_{P-P}$
Lb	B-Y	Input linearity characteristics.	SG1 200mV$_{p-p}$, 400mV$_{P-P}$	B	−5	0	5	%
Swb	B-Y	Sub-carrier input range	SG2 output level shall be variable.	B	—	—	0.1	V$_{P-P}$
CBr	R-Y	Carrier balance DC voltage	Pin21 terminal voltage shall be variable. Carrier leakage shall be minimum.	B	2.9	3.0	3.1	V
Gmr	R-Y	Demodulation output	SG1 200mV$_{P-P}$ input	B	500	600	700	mV$_{P-P}$
Lr	R-Y	Input linearity characteristics	SG1 200mV$_{P-P}$, 400mV$_{P-P}$	B	−5	0	5	%
Swr	R-Y	Sub-carrier input range	SG2 output level shall be variable.	B	—	—	0.1	V$_{P-P}$
B/R	B-Y, R-Y demodulation gain ratio		—	B	0.8	1	1.2	—
△R	B-Y, R-Y sub-carrier orthogonality		Difference of sub-carrier phase delay	B	—	0	±10	deg
Gbb	Burst mixing	B-Y burst gain	Burst output level when BFP is 1V$_{P-P}$.	B	200	300	400	mV$_{P-P}$
Gbr	Burst mixing	R-Y burst gain	Burst output level when BFP is 1V$_{P-P}$.	B	200	300	400	mV$_{P-P}$
SCth	Burst mixing	B-Y burst input SC GATE threshold	Pin3 voltage shall be variable.	B	—	—	0.7	V
G_Y	Y MIX AMP.	Gain	SG3 APL 100% input 200mV$_{P-P}$	C	7	9	11	dB
L_Y	Y MIX AMP.	Input linearity characteristics	SG3 200mV$_{P-P}$, 400mV$_{p-p}$	C	−5	0	5	%
BW_Y	Y MIX AMP.	Frequency characteristics	Frequency which changes GY to −3dB.	C	10	—	—	MHz
Gc	C MIX AMP.	Gain	SG4 1MHz, 200mV$_{P-P}$	C	7	9	11	dB
Lc	C MIX AMP.	Input linearity characteristics	SG4 1MHz, 200mV$_{P-P}$, 400mV$_{P-P}$	C	−5	0	5	%
BWc	C MIX AMP.	Frequency characteristics	Frequency which changes GC to −3dB.	C	10	—	—	MHz
Gv	Video Op-amp	Gain	SG3 APL 100%, 200mV$_{P-P}$	D	−2	0	2	dB
DLv	Video Op-amp	Output dynamic range	SG3 APL 100% Output level shall be variable.	D	1.0	—	—	V$_{P-P}$
S_L	Set up level		Pin11 terminal voltage shall be variable. APL 100%, 200mV$_{P-P}$	D	2.8	3.0	3.2	V
SYth	Sync, Add	C. SYNC pulse threshold	Pin15 terminal voltage shall be variable. pin14 output	C	2.3	2.5	2.7	V
SY_L	Sync, Add	Synchronizing level	15 Pin synchronizing pulse input	C	450	600	750	mV
SYt1	Sync, Add	Delay time 1	15 Pin synchronizing pulse input	C	—	—	200	ns
SYt2	Sync, Add	Delay time 2	15 Pin synchronizing pulse input	C	—	—	200	ns
BLKyth	Y, C blanking	Blanking pulse Y system threshold	Pin16 terminal voltage shall be variable.	C	1.3	1.5	1.7	V
BLKcth	Y, C blanking	Blanking pulse C system threshold	Pin16 terminal voltage shall be variable.	B	3.3	3.5	3.7	V
△Vcb	Y, C blanking	B-Y blanking carrier leakage	Sub-carrier input, 16pin : 0V, 5V	B	—	—	−25	dB
△Vcr	Y, C blanking	R-Y blanking carrier leakage	Sub-carrier input, 16pin : 0V, 5V	B	—	—	−25	dB
△Vsb	Y, C blanking	B-Y blanking signal leakage	Signal input, 16pin : 0V, 5V	B	—	—	−25	dB
△Vsr	Y, C blanking	R-Y blanking signal leakage	Signal input, 16pin : 0V, 5V	B	—	—	−25	dB
CPth	Clamping pulse threshold		Pin17 terminal voltage shall be variable.	C	1.8	2.0	2.2	V

ELECTRICAL CHARACTERISTICS TEST METHOD

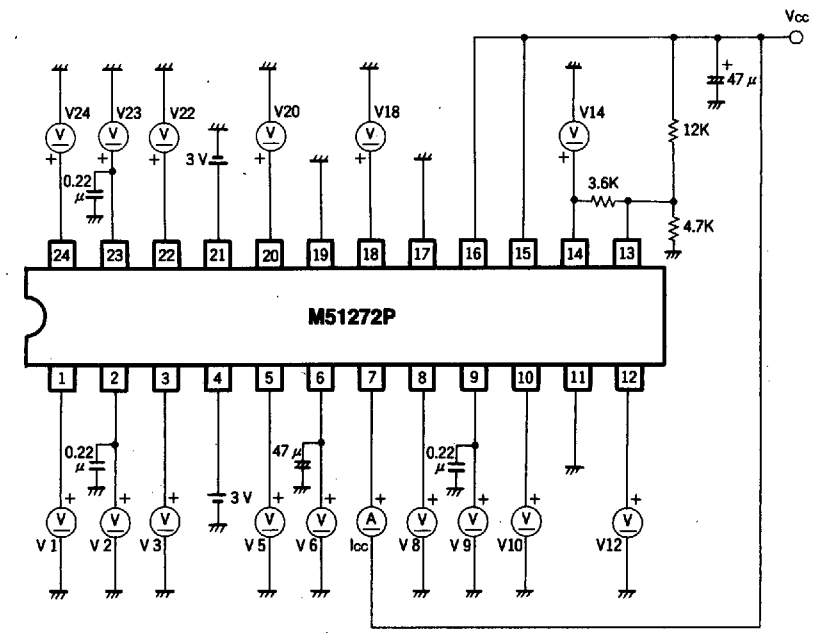
Icc, V_1~V_{24}

Each value read by ammeter or voltmeter is the measured value each measuring point.

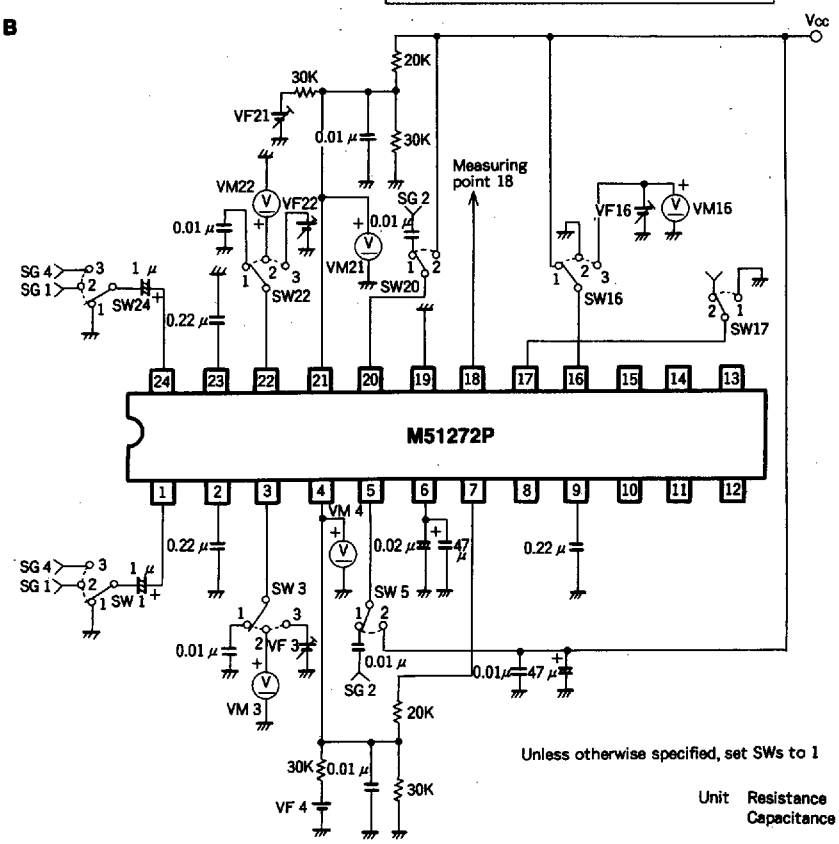
INPUT SIGNAL

SG No.	Waveform	Standard	Remarks
SG1		Level variable	Unless otherwise specified, level shall be 200mV$_{P-P}$.
SG2		4.4336MHz, square wave, duty 50%, output level variable	Unless otherwise specified, output shall be 1V$_{P-P}$.
SG3		APL100% signal, output level variable	
SG4		Sine wave, frequency output level variable	
CP		Shall be synchronous with SG1 and 3.	Shall be close to burst position.
C.SYNC		Shall be synchronous with SG1 and 3.	
BLK		Shall be synchronous with SG1 and 3.	Horizontal blanking interval

TEST CIRCUIT A



TEST CIRCUIT B



B-Y,R-Y CARRIER BALANCE ADJUSTMENT

B-Y: Set SW20 to 2.Adjust VF21 so that VM21 indicates approximately 3V.Input a square wave of 4.4MHz, 1Vp-p and duty 50% from SG2.Adjust VF4 so that 4.4MHz component output at measuring point 18 reads minimum value.

R-Y: Set SW5 to 2. Input a signal from SG2.Adjust VF21 so that 4.4MHz component output at measuring point 18reads minimum value.

CBb and CBr

CBb and CBr represent readings of VM4 and 21 when carrier balance of each B-Y and R-Y is adjusted.

Gmb and Gmr

With carrier balance adjusted, set SW1,17 and 20 to 2.Gmb (mVp-p) represents the output value at measuring point 18 when inputting 200mVp-p from SG1.
Set SW5,17 and 24 to 2. Gmr (mVp-p) represents the output value at measuring point 18 when inputting 200mVp-p from SG1.

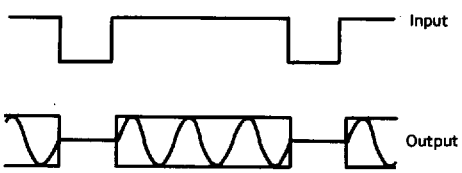
Lb and Lr

With carrier balance adjusted, set SW1,17 and 20 to 2. In the following equation, A (mVp-p) represents output value at measuring point 18 when inputting 200mVp-p from SG-1C (mVp-p)represents output value when inputting 400mV.

$$Lb=(C-2A)/2A(\%)$$

Set SW5,17 and 24 to 2. Determine BmBp-p(input 200mVp-p) and DmVp-p(input 400mV)according to above procedure. The following equation is obtained.

$$Lr=(D-2B)/2B(\%)$$



Swb and Swr

With the conditions as in 2) above,vary input level from SG2. Swb and Swr represent the input level range in which each A and B satisfies the standard.

B/R

From A and B obtained in 2), we get;

$$B/R=A/B$$

ΔR

Set SW20 to 2. Adjust VF4 so that VM4 indicates approximately 3.5V(VM21:approximately 3V).ThusE(deg)represents the phase difference between SG2 input phase and output phase of measuring point 18. Set SW5 to 2(with other SWs at 1). Adjust VF21 so that VM21 indicates approximately 2.5V (VM4:approximately 3V).

In the same manner determine the phase difference F(deg) between input and output.We then get;

$$\Delta R=E-F(deg)$$

Gbb and Gbr

Adjust carrier balance and set SW3 and 20 to 2.V3(V) represents the VM3 voltage reading at pin ③ terminal.Set SW3 to 3.Adjust VF3 so that VM3 reads V3+1V. Gbb(mVp-p)represents output level at measuring point 18.

Set SW5 and 22 to 2. V22(V) represents the voltage reading of VM22 at pin 22 terminal.Set SW 22 to 3. Adjust VF22 so that VM22 reads V22+1V. Follow the same procedure to determine Gbr(mVp-p).

SCth

Adjust carrier balance and set SW3,5,16,17 and 24 to 2. V3(V) represents the voltage reading of VM3 at pin ③ terminal. Set SW3 to 3.

Apply increasing voltage higher than V3 to pin ③. Obseve measuring point 18. In the following equation, V3a(V)represents the voltage at pin ③ when the output level of measuring point 18 satisfies Gmr standard.

$$SCth=V3a-V3(V)$$

BLKcth

Adjust carrier balance and set SW1,17 and 20 to 2.Input 200mVp-p from SG1. Observe output at measuring point 18. Set SW 16 to 3.Decrease terminal voltage at pin ⑯ slowly from 5V. Set SW 16 to 3.BLKcth(V) represents the reading of VM16 when output of measuring point 18 stops.

ΔVcb and ΔVcr

Set SW 20 to 2. Adjust VF4 so that VM4 indicates approximately 2V. (VM21 shall be in a carrier balance state). In the following equation,Vcb_1 represents output level at measuring point 18 when SW16 is set to 1. Vcb_2 represents that of measuring point 18 when SW16 is set to 2.

$$\Delta Vcb=20 \log Vcb_2/Vcb_1(dB)$$

Set SW 5 to 2. Adjust VF21 so that VM21 indicates approximately 2V. (VM4 shall be in a carrier balance state). The resulting equation is;

$$\Delta Vcr=20 \log Vcr_2/Vcr_1(dB)$$

ΔVsb and ΔVsr

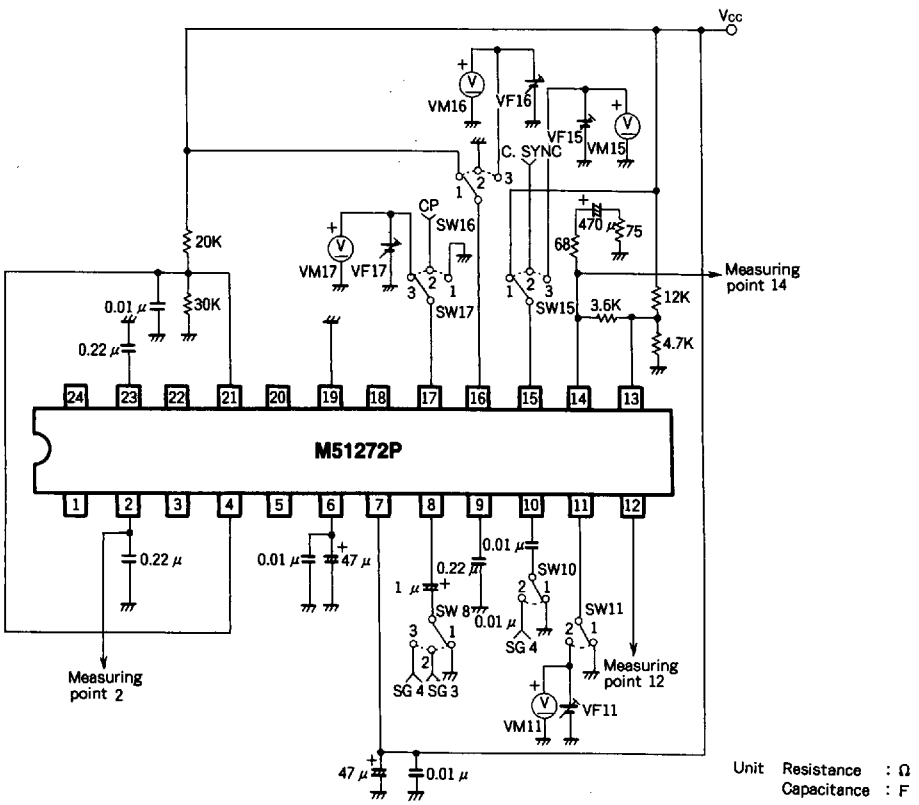
Set SW1 to 3;SW5 and 20 to 2 ,adjusting carrier balance. Input 4.4336MHz, 200mVp-p from SG4.In the following equation,Vsb_1 represents output level at measuring point 18 when SW16 is set to 1.Vsb_2 represents that of measuring point 18 when SW16 is set to 2.

$$\Delta Vsb=20 \log Vsb_2/Vsb_1(dB)$$

Set SW 24 at 3;SW5 and 20 at 2. The resulting equation is;

$$\Delta Vsr=20 \log Vsr_2/Vsr_1(dB)$$

TEST CIRCUIT C



Unless otherwise specified, SWs shall be set to 1.

Gy

Set SW8 and 17 to 2. Input an APL100% signal at SG3. In the following equation,G(mVp-p) represents the output level at measuring point 12.

$$Gy=20 \log G/200(dB)$$

Ly

as in 1),vary input level from SG3 into 400mVp-p. In the following equation, H (mVp-p) represents the output level at measuring point 12.

$$Ly=(H-2G)/2G(\%)$$

BWy

Set SW8 to 3;input 200mVp-p from SG4 and vary frequency. BWr represents the frequency by which gain at measuring point 12 becomes −3dB compared to Gy.

Gc

Set SW10 to 2;input 200mVp-p,1MHz from SG4.In the following equation, I (mVp-p) represents the output level at measuring point 12.

$$Gc=20 \log I/200 (dB)$$

Lc

as in 4),vary input level from SG4 into 400mVp-p. In the following equation, J (mVp-p) represents the output level at measuring point 12.

$$Lc=(J-2I)/2I(\%)$$

BWc

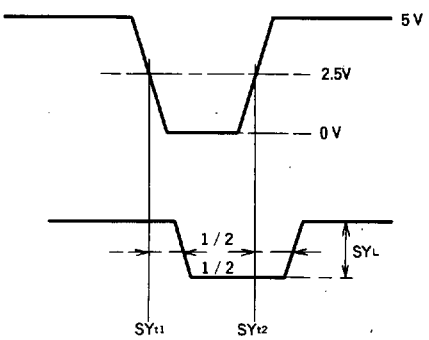
Set SW10 to 2;input 200mVp-p from SG4 and vary frequency. BWc represents the frequency by which gain at measuring point 12 becomes −3dB compared to Gc.

SYth

Set SW15 to 3.Slowly decrease pin ⑮ terminal voltage from 5V by adjusting VF15. Observe measuring point 14.SYth(V) represents the VM15 reading when DC voltage at measuring point 14 decreases from 2V to approximately 1.5V.

SY_L,SY_{t1} and SY_{t2}

Set SW15 to 2.Input C. Sync pulse. Determine SY_L, SY_{t1} and SY_{t2} at measuring point 14 as follows.(SW11 shall be set to 2. VF11=3V)



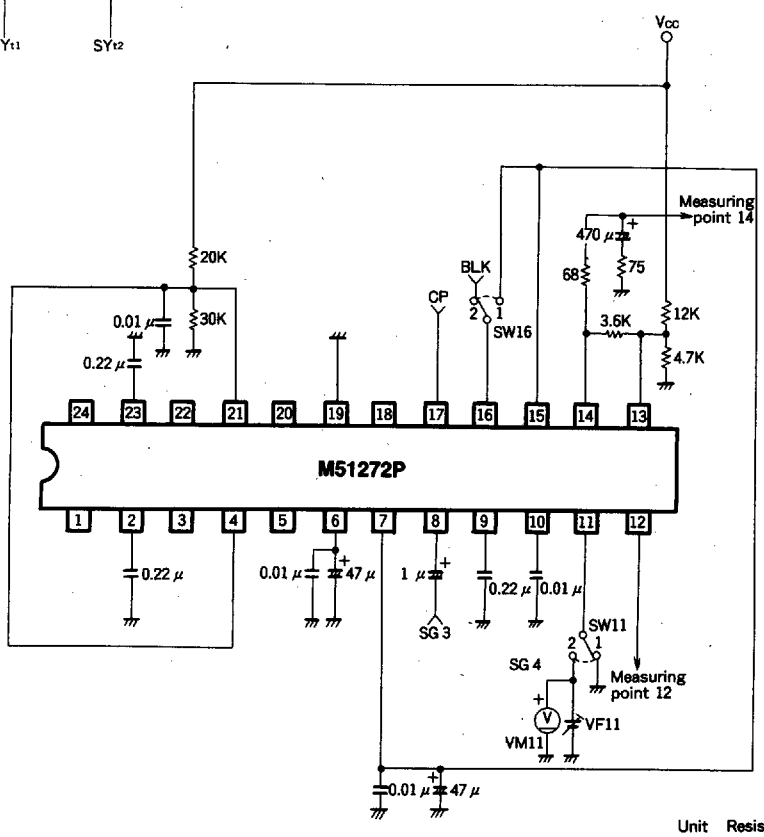
BLKyth

Set SW16 to 3. Slowly decrease pin ⑯ terminal voltage from 5V by adjusting VF16. Observe measuring point 12. BLKyth(V), represents the VM16 reading when pin ⑫ terminal voltage decreases from high (approximately 2.2V) to low (approximately 1V).

CPth

Set SW17 to 3. Slowly decrease pin ⑰ terminal voltage from 5V using VF17. CPth represents the VM17 reading when voltage at measuring point 2 increases from low (approximately 0V) to high (approximately 2V).

TEST CIRCUIT D



Unit Resistance : Ω
Capacitance : F

Unless otherwise specified, SWs shall be set to 1.

Measurement of Gv

Input APL100%, 200mVp-p from SG3.In this state, Gv_1 and Gv_2 represent output levels at measuring points 12 and 14 respectively. The resulting equation is;

$$Gv=20 \log Gv_2/Gv_1(dB)$$

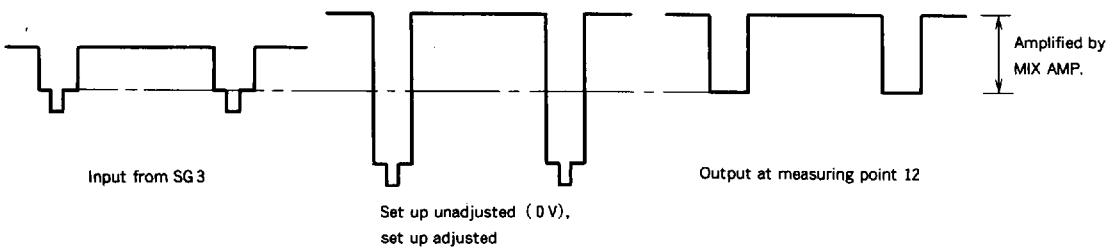
Measurement of DLv

Input APL100% from SG3.Increase the input signal level while observing measuring point 14.

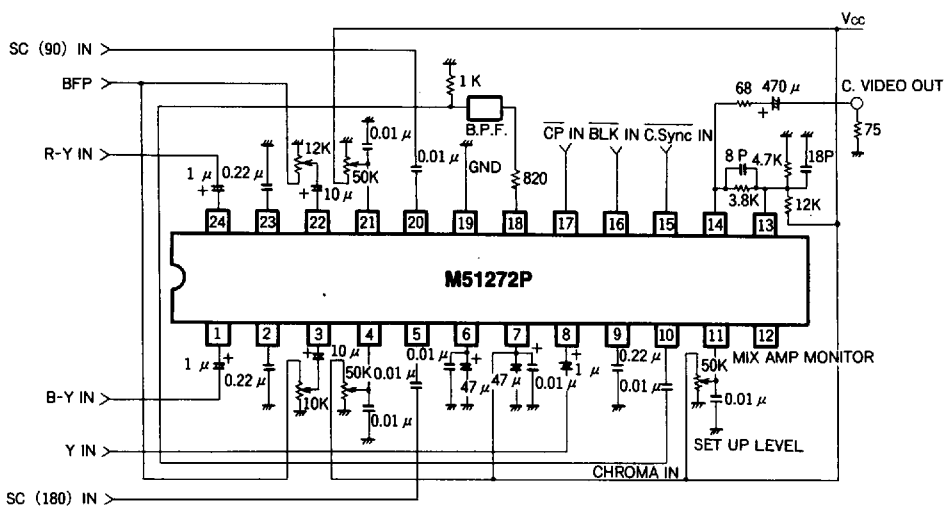
DLv(Vp-p) represents the output level read just before the output signal begins to show non-linear change.

Measurement of SL

Set SW11 and 16 to 2.Input APL100%, 200mVp-p from SG3. Adjust VF11 so that output signal pedestal level becomes equal to the input signal level.In this condition, SL(V) represents the VM11 value.



APPLICATION EXAMPLE



Unit Resistance : Ω
Capacitance : F

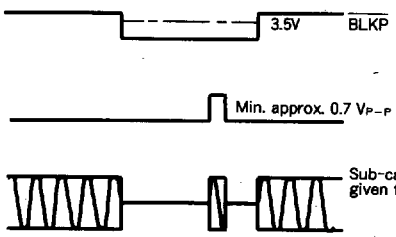
PRECAUTIONS FOR APPLICATION

INPUT PULSE

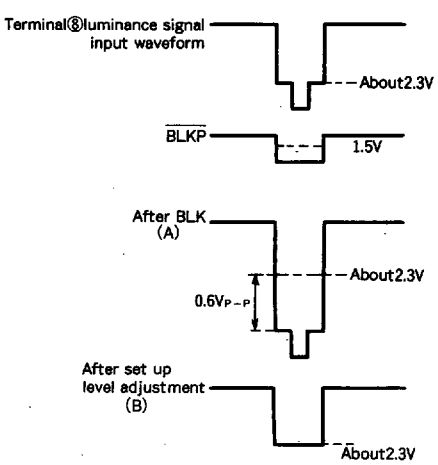
1. Blanking pulse (BLKP)

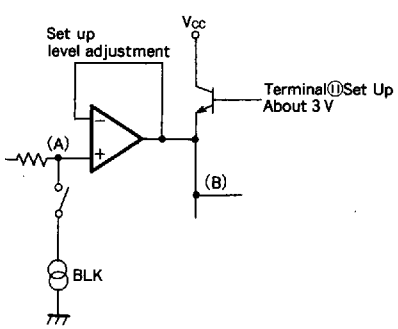
BLKP input is at pin ⑯ with threshold for color signal and luminance signal.

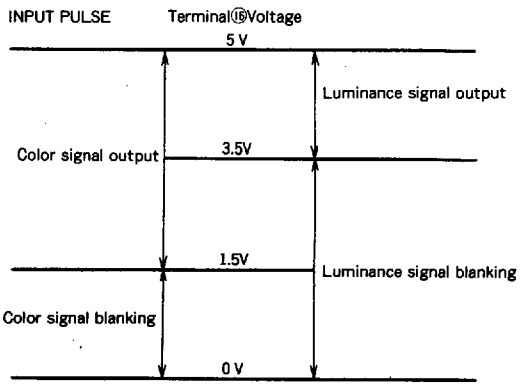
a. For color signal, threshold is 3.5V. When LO is at "3.5 V - GND," sub-carrier supply for R-Y, B-Y demodulator is stopped. When burst flag pulse is inputted at B-Y, subcarrier is supplied during the period.



b. Threshold is about 1.5 V for luminance signal. When LO is at "1.5V - GND," blanking is done to luminance signal.

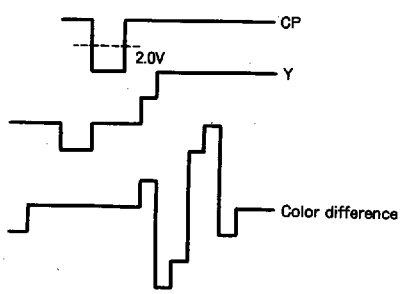






2. Clamping pulse (CP)

CP input is at pin ⑰ with threshold of 2.0V. When LO is at "2.0 - GND," clamping function works. B-Y and R-Y can be set at any part of horizontal retrace line part as long as blanking is conducted to this part. In this case, when luminance signal has sync, set CP at back porch.



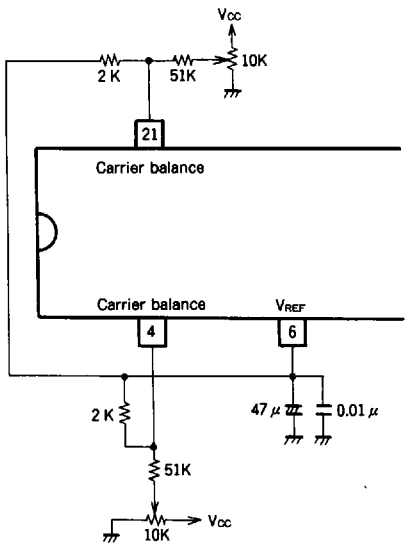
3. Sync pulse (C. Sync)

C. Sync input is at pin ⑮ with threshold of 2.5V. When LO is "2.5V - GND," sync is added to C.VIDEO signal. In case of luminance signal with sync inputted is outputted, set pin áN at "2.5V - VCC." In such case, input luminance signal without blanking, and set Set Up level pin (pin ⑪) to GND.

4. Burst flag pulse (BFP)

BFP input is at pin ③(B-Y) and pin ㉒(R-Y). 1/9 of input level BFP is superimposed on color difference signal in the IC (input impedance 2kΩ). When BFP is encoded to NTSC and into PAL, input only to B-Y (pin③) and to R-Y (pin ㉒) respectively.

CARRIER BALANCE OPTIMUM ADJUSTMENT CIRCUIT



Points 1. To apply adjusting voltage based on ⑥ pin V_{REF} voltage.
2. To allow fine adjustment.

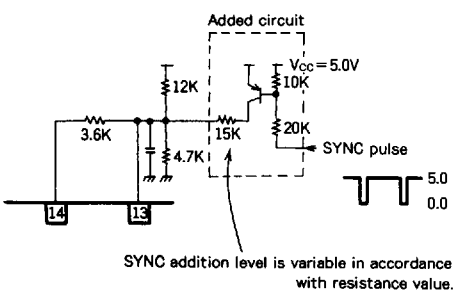
Improvement by the circuit above
1. Carrier balance shift against temperature change is eliminated.
2. Adjustment range is widened allowing easy adjustment.

Carrier balance
Ground pin ⑰, set clamp, set pin ⑯ to Vcc, and then remove blanking.

Input proper burst flag pulse (NTSC→B-Y, PAL→B-Y, R-Y) and sub-carrier. Then, observing pin ⑱ chroma output, adjust pin ④ and ㉑ voltage so that carrier leakage becomes minimum. (Burst is outputted.)

To input sub-carrier (pin ⑤, ⑳), input rectangular wave of 0.2 - 2 V_{P-P} at duty 50%.

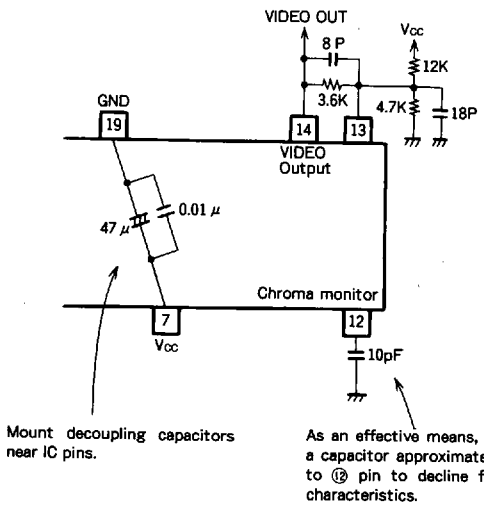
SYNC EXTERNAL ADDITION METHOD



In the circuit above, sync dispersion is only that of external resistance dispersion.

Quantity of sync addition of the IC is uneven because it is determined by the external resistance (3.6kΩ) and the IC internal current.

COUNTERMEASURE FOR OSCILLATION AT OUTPUT STAGE



Depending on conditions of printed board, undesirable oscillation may be generated. In that case, refer to the information above for countermeasures.

BLOCK DIAGRAM OF M51271 and M51272 (ENCODER)