

M52005P

COMB FILTER Y/C PROCESSOR, CORING

DESCRIPTION

The M52005P is a semiconductor integrated circuit containing switching circuits for comb filter selection, noise reduction by coring, and S pin input. This IC can rationalize the design of a TV set with an S pin.

FEATURES

- Produces Y signal with minimum ringing, due to high performance Y/C separation circuit.
- Provides simple comb filter function.
- NR level setting is discretionary.
- NR frequency band is selectable.
- Signal can be output without passing through NR circuit.

APPLICATION

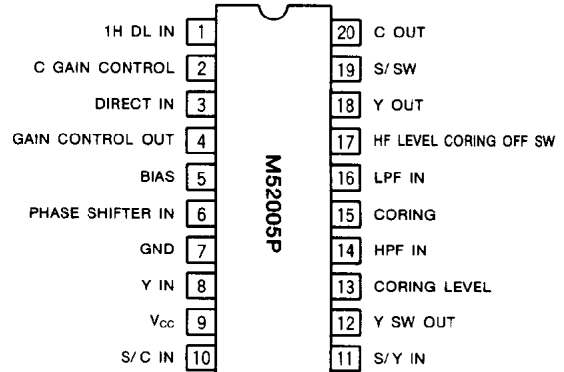
Color TV

RECOMMENDED OPERATING CONDITION

Supply voltage range 11~13V

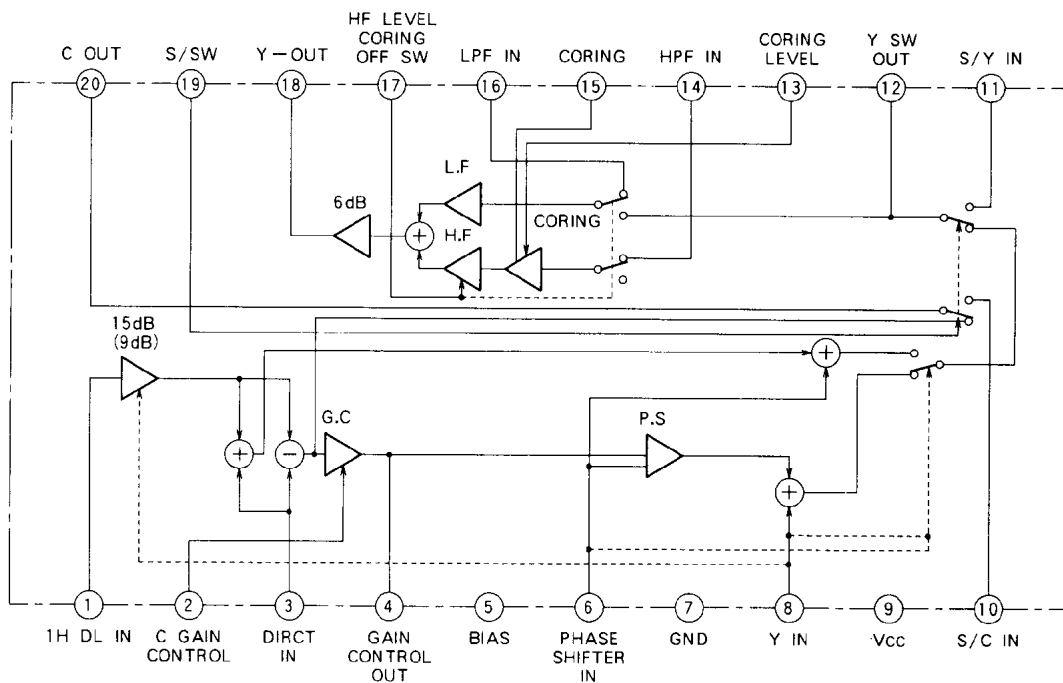
Rated supply voltage 12V

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

BLOCK DIAGRAM



COMB FILTER Y/C PROCESSOR, CORING

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V _{cc}	Supply voltage	14	V
P _d	Power dissipation	1250	mW
T _{opr}	Operating temperature	-20~75	°C
T _{stg}	Storage temperature	-40~125	°C
Surage	Electrostatic discharge	±200	V

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{cc}=12V, unless otherwise noted. Position all switches of test circuit at "a" as initial setting. Each VR setting is shown in test circuit diagram. No signal is input. Only settings different from initial settings are shown in "Test conditions" column.)

Symbol	Parameter	Test Point	Input	Test conditions	Note	Limits			Unit
						Min.	Typ.	Max.	
I _{cc}	Circuit current	Ⓐ	—	SW9 : b	1	24.3	33.3	42.3	mA
G _{VH1}	High-frequency amplifier gain (1)	TP18	SG1	VR13 : 12V	2	15.1	16.1	18.1	dB
G _{VH2}	High-frequency amplifier gain (2)	TP18	SG1	VR13 : 12V	2	8.1	10.1	12.1	dB
G _{VH3}	High-frequency amplifier gain (3)	TP18	SG1	VR17 : 2V, VR13 : 12V	2	-31.1	-28.1	-25.1	dB
G _{VCO1}	Coring amplifier gain (1)	TP18	SG2	VR1 : 12V	3	9.3	12.3	15.3	dB
G _{VCO2}	Coring amplifier gain (2)	TP18	SG2	VR17 : 12V, VR13 : 2V	3	5.1	7.6	10.1	dB
G _{VL1}	Low-frequency amplifier gain	TP20	SG3	VR19 : 5V	4	5.0	6.2	7.4	dB
G _{VD1}	DL damp Correction amplifier gain (1)	TP20	SG4		5	12.7	14.7	16.7	dB
G _{VD2}	DL damp Correction amplifier gain (2)	TP20	SG4	SW8 : b	5	7.4	8.8	11.4	dB
G _{VC1}	Chroma gain control amplifier (1)	TP4	SG5	SW4 : b	6	-12.1	-9.1	-6.1	dB
G _{VC2}	Chroma gain control amplifier (2)	TP4	SG5	SW4 : b, VR2 : 12V	6	-15.0	-13.0	-11.0	dB
G _{VC3}	Chroma gain control amplifier (3)	TP4	SG5	SW4 : b, VR2 : 0V	6	-2.9	-0.9	1.1	dB
G _{VY1}	Y/C adder/subtractor gain (1)	TP12	SG4	SW5, SW6-2 : b	7	4.6	6.6	8.6	dB
G _{VY2}	Y/C adder/subtractor gain (2)	TP12	SG4	SW5, SW6-2, SW8 : b	7	9.3	11.3	13.3	dB
G _{V3}	Y output gain (1)	TP12	SG5	SW4, SW6-1 : b, VR6 : 0V	8	-1.7	-0.2	0.8	dB
G _{V8}	Y output gain (2)	TP12	SG5		9	-1.7	-0.2	0.8	dB
G _{V11}	Y output gain (3)	TP12	SG5	VR19 : 5V	10	-1.7	-0.2	0.8	dB
G _{V1}	C output gain (1)	TP12	SG5		11	12.6	14.6	16.6	dB
G _{V10}	C output gain (2)	TP20	SG5	VR19 : 5V	12	-1.3	0.2	1.2	dB
C. T. Y	S mode/NORMAL crosstalk (Y)	TP18	SG6		13	—	-56	-50	dB
C. T. C	S mode/NORMAL crosstalk (C)	TP18	SG6		14	—	-63	-55	dB
D _{RY1}	Y output dynamic range (1)	TP18	SG7	SW4, SW6-1 : b, VR6 : 0V	15	2.8	3.7	—	V _{P-P}
D _{RY2}	Y output dynamic range (2)	TP18	SG7		16	2.8	3.5	—	V _{P-P}
D _{RY3}	Y output dynamic range (3)	TP18	SG7	VR19 : 5V	17	2.5	3.0	—	V _{P-P}
D _{RC1}	C output dynamic range (1)	TP20	SG7		18	3.2	4.6	6.0	V _{P-P}
D _{RC2}	C output dynamic range (2)	TP20	SG7	VR19 : 5V	19	4.9	7.0	9.1	V _{P-P}
F1	Frequency characteristic (1)	TP18	SG8	SW4, SW6-1 : b, VR6 : 0V	20	-2.5	-1.2	0.1	dB
F2	Frequency characteristic (2)	TP8	SG8		21	-1.1	0.4	1.9	dB
F3	Frequency characteristic (3)	TP18	SG8	VR19 : 5V	22	-1.0	0.5	2.0	dB
V _{TH19}	S/SW threshold voltage	TP20	SG3	VR19 : Variable	23	1.5	2.5	3.5	V _{DC}
V _{TH17}	Through SW (HF level) threshold voltage	TP18	SG3	SW16 : b, V17 : Variable, VR19 : 0V	24	1.0	1.7	2.7	V _{DC}
V _{TH6}	Simple mode SW threshold voltage	TP12	SG3	SW6-1 : b, VR6 : Variable	25	1.7	2.7	3.7	V _{DC}

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ELECTRICAL CHARACTERISTICS TEST METHOD

Note

- (1) Circuit current
With initial settings shown in test circuit diagram, change SW9 position to "b", and read ammeter A.
- (2) High-frequency amplifier gains (1), (2) and (3)
With initial settings shown in test circuit diagram, change VR13 to 12V, input SG1 at pin ⑭, and read output at pin ⑯ while changing VR17 to 12, 6 and 2V. G_{VH1} , G_{VH2} and G_{VH3} represent respective outputs.
- (3) Coring amplifier gains (1) and (2)
With initial settings shown in test circuit diagram, change VR17 to 12V, input SG2 at pin ⑭, and read output at pin ⑯ while changing VR13 from 6 to 2V. G_{VCO1} and G_{VCO2} represent respective outputs.
- (4) Low-frequency amplifier gain
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG3 at pin ⑪, and read output at pin ⑯.
- (5) DL damp correction amplifier gains (1) and (2)
With initial settings shown in test circuit diagram, input SG4 at pin ①, and read output at pin ⑳ as V_{D1} . Then, change SW8 position to "b", and read output at pin ㉑ as V_{D2} .
- (6) Chroma gain control amplifier characteristics
With initial settings shown in test circuit diagram, change SW4 position to "b", input SG5 at pin ③, and read output at pin ④ while changing VR2 to 12, 6 and 0 V in sequence. V_{C1} , V_{C2} and V_{C3} represent respective outputs.
- (7) Y/C adder/subtractor gains (1) and (2)
With initial settings shown in test circuit diagram, change SW5 and SW6-2 positions to "b", input SG4 at pin ⑥, and read output at pin ⑫ as V_{Y1} . Then change SW8 position to "b", and read output at pin ⑫ as V_{Y2} .
- (8) Y output gain (1)
With initial settings shown in test circuit diagram, change SW6-1 position to "b", input SG5 at pin ③, and read output at pin ⑫.
- (9) Y output gain (2)
With initial settings shown in test circuit diagram, input SG5 at pin ⑧, and read output at pin ⑫.
- (10) Y output gain (3)
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG5 at pin ⑪, and read output at pin ⑫.
- (11) C output gain (1)
With initial settings shown in test circuit diagram, input SG4 at pin ①, and read output at pin ㉑.
- (12) C output gain(2)
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG5 at pin ⑩, and read output at pin ㉑.
- (13) S/NORMAL crosstalk (Y)
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG6 at pin ⑪, and read output at pin ⑯ as V_{CTY} . Then, change VR19 to 0V, and read output at pin ⑯ as V_{CTY} .
- (14) S/NORMAL crosstalk (C)
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG6 at pin ⑩, and read output at pin ㉑ as V_{CTC} . Then, change VR19 to 0V, and read output at pin ㉑ as V_{CTC} .
- (15) Y output dynamic range (1)
With initial settings shown in test circuit diagram, change SW6-1 position to "b", input SG7 at pin ③, and increase amplitude gradually. Read output amplitude when output at pin ⑯ begins to distort. DR_{Y1} represents this amplitude.
- (16) Y output dynamic range (2)
With initial settings shown in test circuit diagram, input SG7 at pin ⑧, and increase amplitude gradually. Read output amplitude when output at pin ⑯ begins to distort. DR_{Y2} represents this amplitude.
- (17) Y output dynamic range (3)
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG7 at pin ⑪, and increase amplitude gradually. Read output amplitude when output at pin ⑯ begins to distort. DR_{Y3} represents this amplitude.
- (18) C output dynamic range (1)
With initial settings shown in test circuit diagram, input SG7 at pin ①, and increase amplitude gradually. Read output amplitude when output at pin ㉑ begins to distort. DR_{C1} represents this amplitude.
- (19) C output dynamic range (2)
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG7 at pin ⑩, and increase amplitude gradually. Read output amplitude when output at pin ㉑ begins to distort. DR_{C2} represents this amplitude.
- (20) Frequency characteristic (1)
With initial settings shown in test circuit diagram, change SW6-1 position to "b", input SG8 at pin ③, and read output at pin ⑯ at frequencies of 1 MHz and 10MHz. V_1 and V_2 represent respective outputs.
- (21) Frequency characteristic (2)
With initial settings shown in test circuit diagram, input SG8 at pin ⑧, and read output at pin ⑯ at frequencies of 1MHz and 10MHz. V_1 and V_2 represents respective outputs.
- (22) Frequency characteristic (3)
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG8 at pin ⑪, and read output at pin ⑯ at frequencies of 1MHz and 10MHz. V_1 and V_2 represent respective outputs.
- (23) S/SW threshold voltage
With initial settings shown in test circuit diagram, change VR19 to 5V, input SG3 at pin ⑩, and lower voltage of VR19 while observing output at pin ㉑. When output disappears at pin ㉑, read VR19 voltage as V_{TH19} .

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(24) Through SW threshold voltage

With initial settings shown in test circuit diagram, change SW16 position to "b", apply same voltage as at pin ⑫ to VR16, and input SG3 at pin ⑪. Then lower voltage of VR 17 while observing output at pin ⑱. When output appears at pin ⑱, read voltage of VR17 as V_{TH17} .

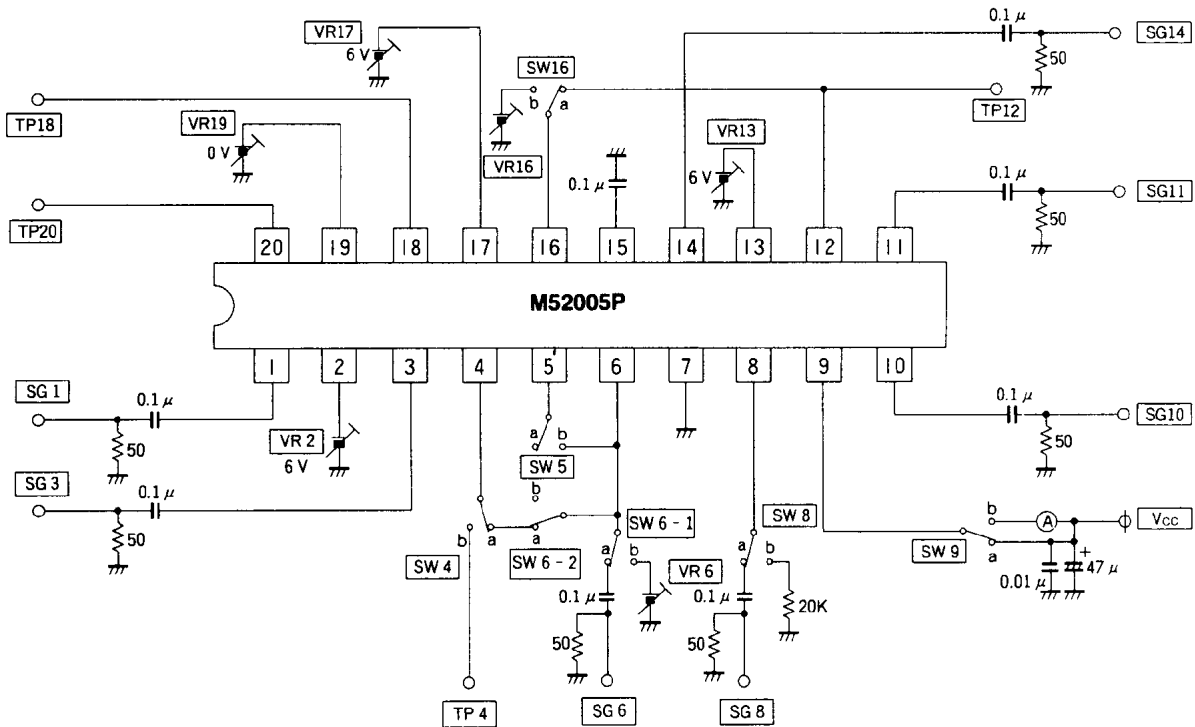
(25) Simple mode SW-threshold voltage

With initial settings shown in test circuit diagram, change SW6-1 position to "b", apply 5V to VR6, and input SG3 at pin ⑪. Then lower voltage of VR6 while observing output at pin ⑫. When output disappears at pin ⑫, read voltage of VR6 as V_{TH6} .

INPUT SIGNAL

SG. NO	Signal Content		
SG1	1MHz	100mVp-p	CW
SG2	1MHz	100mVrms	CW
SG3	1MHz	500mVp-p	CW
SG4	3.58MHz	100mVp-p	CW
SG5	3.58MHz	500mVp-p	CW
SG6	3.58MHz	1.5Vp-p	CW
SG7	500KHz	Variable	CW
SG8	1MHz/10MHz	100mVp-p	CW

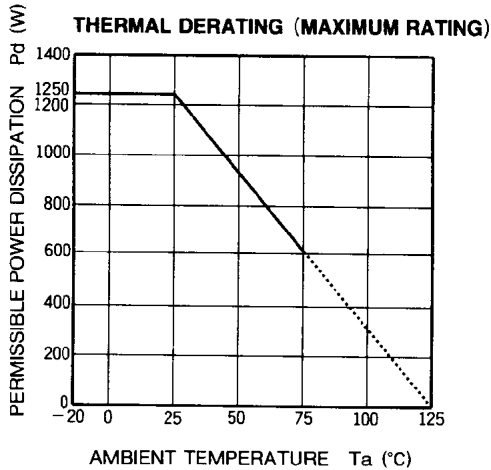
TEST CIRCUIT



Unit Resistance : Ω
 Capacitance : F

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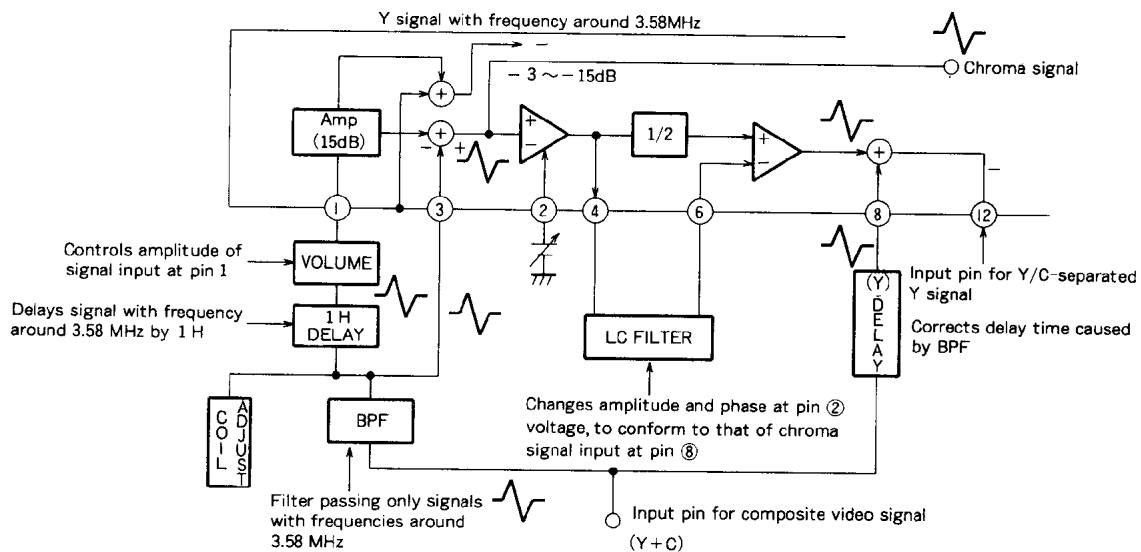
TYPICAL CHARACTERISTICS



DESCRIPTION OF Y/C SEPARATION BLOCK

Characteristics

Limited frequency band signal is passed through 1H DELAY line, to obtain ring-free Y signal.



OPERATION

Input composite chroma signal is passed through Y(DELAY)line and input to pin ⑧, while signal with frequency around 3.58MHz obtained by BPF is input to 1H DELAY line and to pin ③. signal passed through 1H DELAY line is phase-shifted by 180° with respect to signal input at pin ③, due to functions of VOLUME, ADJUST COIL and internal 15 dB amplifier in IC. Therefore, Y signal with frequency around 3.58MHz and chroma signal

are obtained by addition or subtraction between phase-shifted signal and signal input at pin ③. Chroma signal thus obtained is passed through gain control amplifier and all-pass filter to become phase-inverted signal with same level as chroma signal input at pin ⑧, and added to chroma signal. Thus, Y signal alone is separated from video signal.

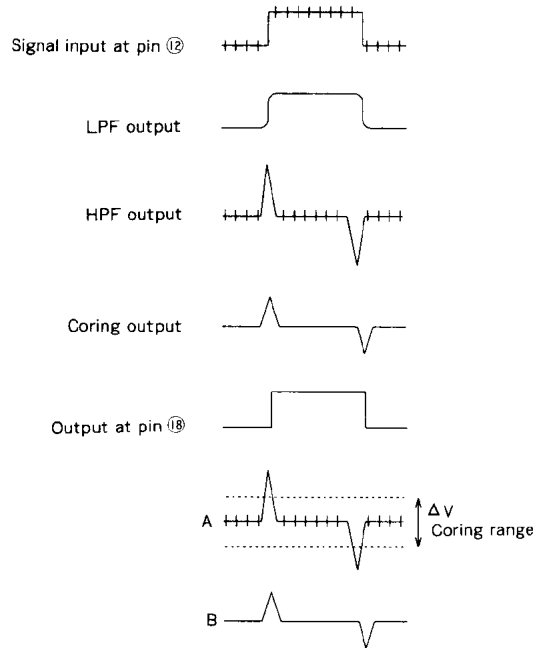
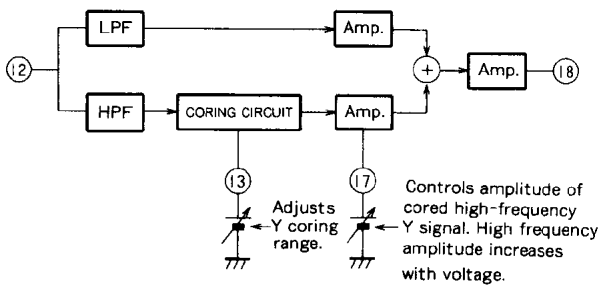
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DESCRIPTION OF CORING BLOCK

Characteristics

Coring block eliminates wide range of noise without impairing waveform.

Y/C-separated Y signal or S/Y signal is input.



OPERATION

Noise contains many high-frequency components. Therefore, Y signal input at pin 12 is first passed through LPF and HPF for separation into high- and low-frequency components. The high-frequency Y signal is then cored so that component with amplitude within specified range is not passed but output as DC. Cored high-frequency Y signal is amplified to same amplitude as Y signal before coring, and is combined with low-frequency Y signal. As a result, pin 18 outputs Y signal that is noiseless compared with signal input at pin 12.

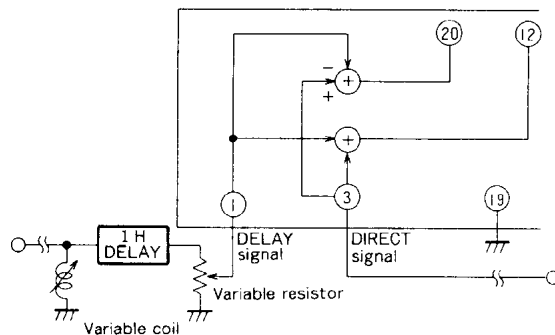
CORING OPERATION

When signal indicated by "A" below is input, coring circuit outputs cored component in range ΔV as DC, so that noise within range ΔV is not output. Accordingly, as indicated by "B," output signal has an amplitude smaller by ΔV than that of signal "A." Width of ΔV decreases as voltage at pin 13 is increased.

ADJUSTMENT OF EXTERNAL COMPONENTS OF RECOMMENDED CIRCUIT (Y/C Separation)

Connect pin 6 to GND, for simple comb filter mode. In this mode, result of addition/subtraction between signals input at pins 1 and 3 is output to pins 12 and 20. When composite video signal is input to this recommended IC in simple comb filter mode, DELAY signal and DIRECT signal are input at pins 1 and pin 3, respectively.

When values of variable coil and variable resistor are changed appropriately, sum of signals input at pins 1 and 3 is output to pin 12. signal thus output is Y signal component with frequency around 3.58 MHz. Adjust 1H DELAY line so that signal output at 12 pin does not contain chroma signal component.

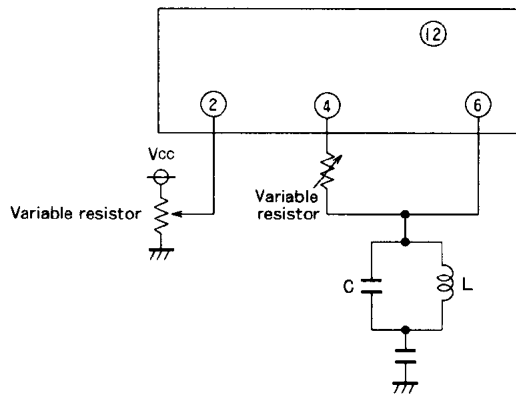


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Disconnect pin ⑥ from GND so that bias voltage is applied from pin ④ to pin ⑥. Recommended IC in ring-free mode is obtained. In this mode, pin ⑫ outputs Y/C-separated Y signal. However, chroma component remains, and can be removed completely by adjusting variable resistors connected to pins ② and ④.

If chroma component cannot be removed completely by this method, change LC filter.

If chroma component is shifted by half wavelength, replace LC filter with series resonance circuit.

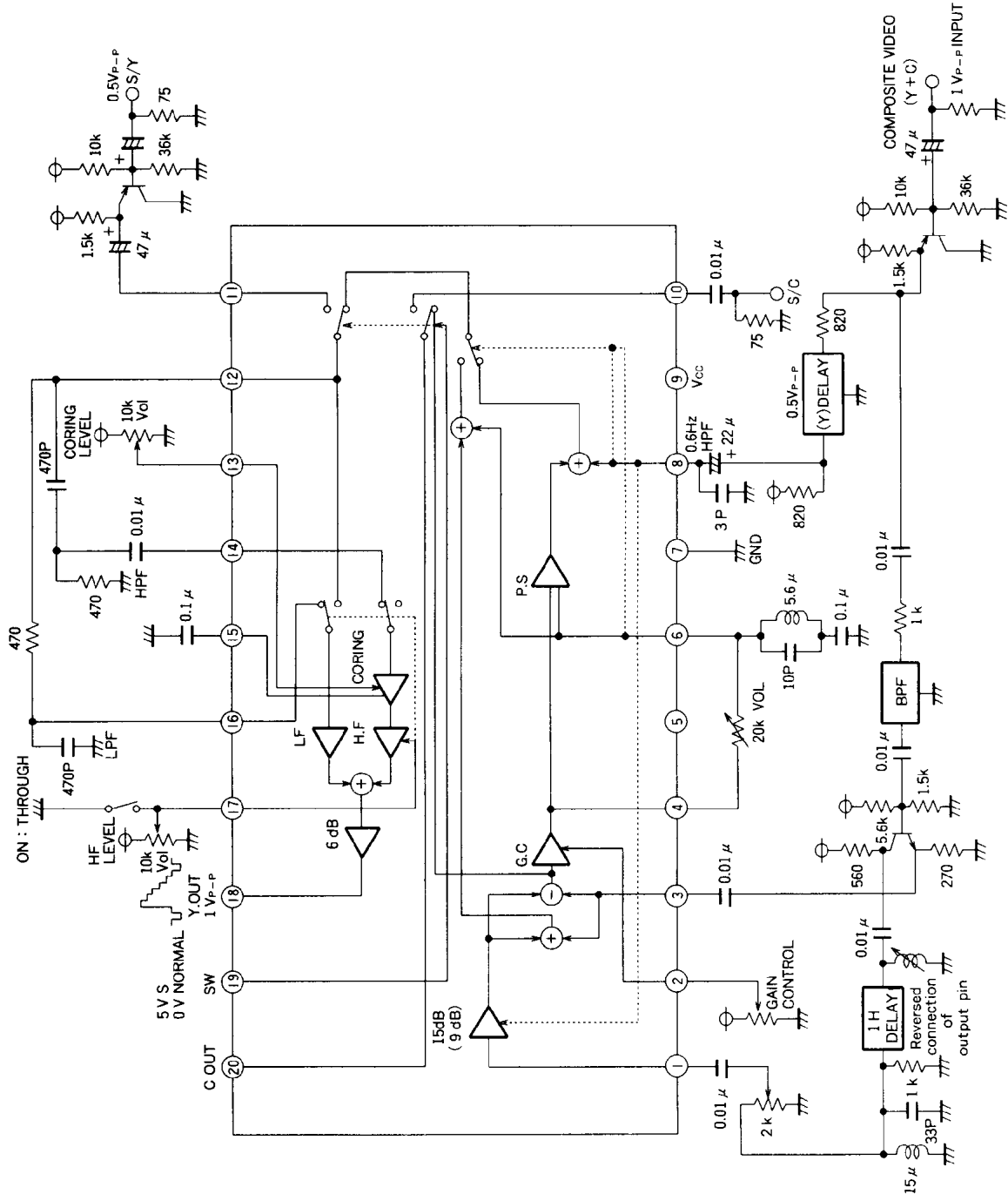


SW PIN SETTINGS FOR EACH OPERATION MODE

Operation Mode	Pin6	Pin17	Pin19
Ring-free, coring	Bias voltage applied from pin ④	About 1.5V min	GND
Ring-free, without coring	Bias voltage applied from pin ④	GND	GND
Simple comb filter, without coring	GND	GND	GND
Simple comb filter, coring	GND	About 1.5V min.	GND
S-pin input, coring	—	About 1.5V min.	About 2.5V min.
S-pin input, without coring	—	GND	About 2.5V min.

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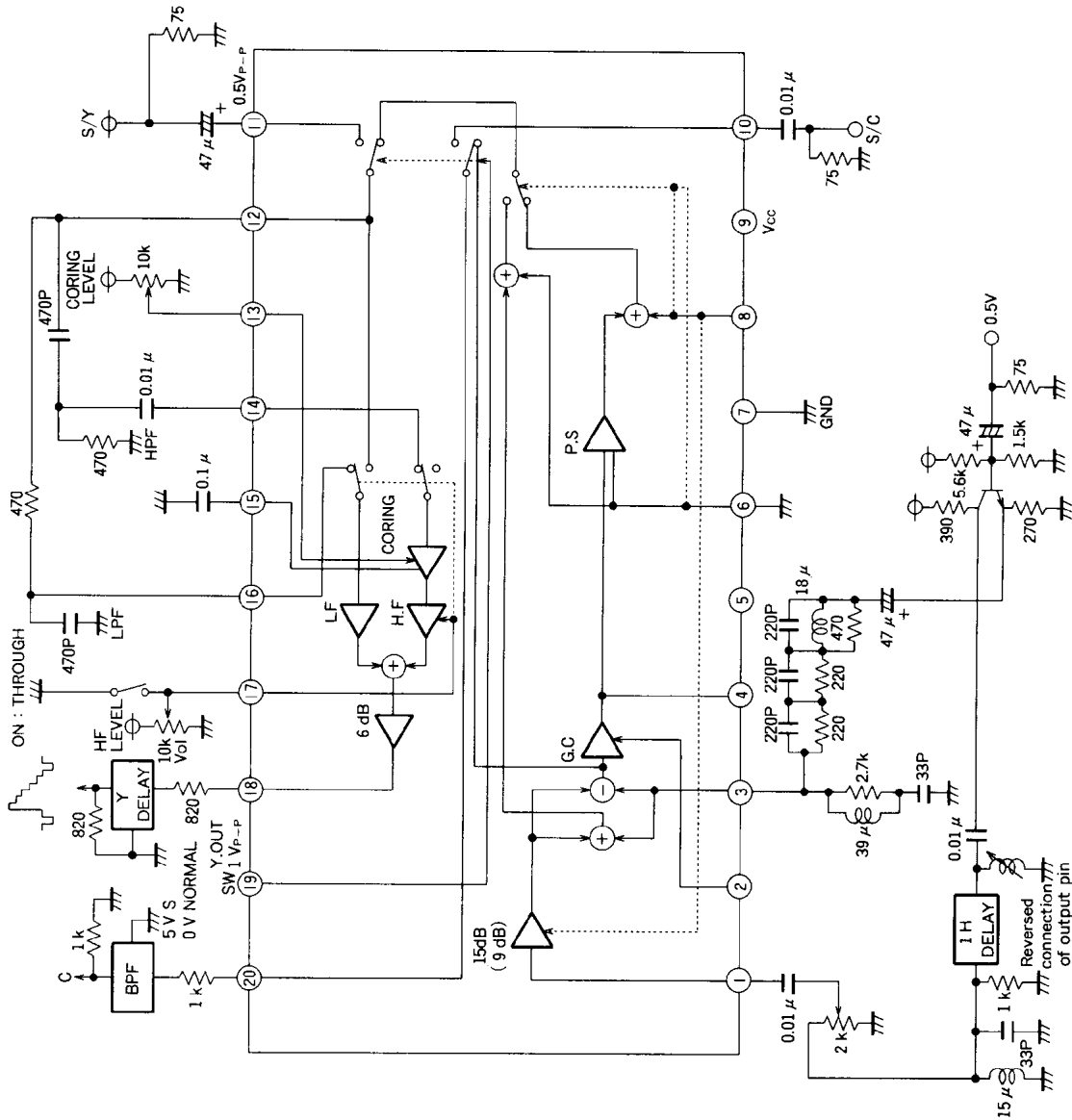
APPLICATION EXAMPLE 1 (Ring-free)



Unit Resistance : Ω
 Capacitance : F

COMB FILTER Y/C PROCESSOR, CORING

APPLICATION EXAMPLE 2 (Simple comb filter)



Unit Resistance : Ω
Capacitance : F

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DESCRIPTION OF PIN

Pin No.	Name	DC Voltage (V)	Peripheral Circuit of Pin	Function
①	1H DL IN	3.8		Input pin for chroma signal passed through 1H DELAY line
②	C GAIN CONTROL	-		Used to control chroma signal output amplitude at pin ④.
③	DIRECT IN	9.5		Input pin for chroma signal passed through BPF
④	GAIN CONTROL OUT	4.2		Output pin for chroma signal with amplitude controlled at pin ②
⑤	BIAS	4.2		Normally open

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC Voltage (V)	Peripheral Circuit of Pin	Function
⑥	PHASE SHIFTER IN	—		Chroma signal output from pin ④ is phase-shifted externally, and input at this pin.
⑦	GND	0		GND
⑧	Y IN	9.5		Input pin for composite video signal passed through (Y) DELAY line
⑨	Vcc	12		Vcc
⑩	S/C IN	9.5		Input pin for S-pin chroma signal
⑪	S/C IN	9.5		Input pin for S-pin Y signal

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC Voltage (V)	Peripheral Circuit of Pin	Function
12	Y SW OUT	9.5		Output pin for processing Y/C-separated Y signal
13	CORING LEVEL	—		Used to control coring range of high-frequency component of Y/C-separated Y signal.
14	HPF IN	2.5		Input pin for Y signal to be cored
15	CORING	—		Pin for connection with capacitor to provide bias for coring
16	LPF IN	Apply same DC voltage as at pin 12.		Input pin for low-frequency Y/C-separated Y signal passed through LPF

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC Voltage (V)	Peripheral Circuit of Pin	Function
17	HF LEVEL CORING OFF SW	—		Switch for selecting amplitude control of cored high-frequency Y signal, or direct output of Y signal without coring
18	Y OUT	About 9		Output pin for Y signal composed of cored high-frequency Y signal and low-frequency Y signal
19	S/SW	—		Input changeover switch ; selects NORMAL input at 1.4V or lower voltage, and S input at 3.5V or higher voltage
20	C OUT	About 4.7		Output pin for Y/C-separated chroma signal