DESCRIPTION

The M5224 are semiconductor integrated circuits designed as quad operational amplifiers in which single power supply operation is possible.

The devices come in a standard 14-pin DIP, FP and contain four circuits for yielding a high internal phase compensation and high performance. For both input and output, operation is possible from the GND level and this makes it possible for the device to be used widely as a general-purpose operational amplifier in the motor control circuits of such equipment as cassette decks, turntables, VTRs, and digital audio disc players as well as in automotive electronic products and communications equipment. It can be also employed as a simple comparator.

FEATURES

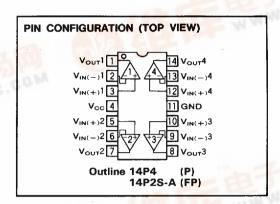
- Output voltage level can be reduced to near the GND level
- Wide operating supply voltage range and single power supply operation possible V_{CC}=3V~+36V(V_{CCmax})
- High voltage gain ························ G_{VO}=110dB(typ.)
- High allowable power dissipation

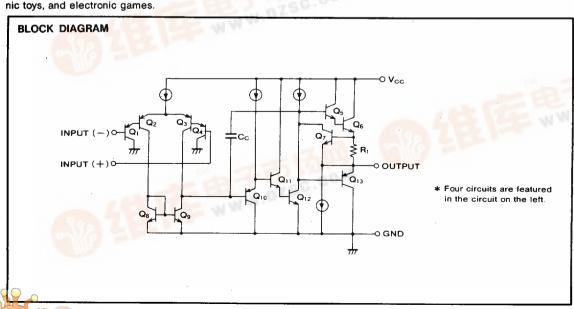
P_d=700mW(M5224P)
P_d=550mW(M5224FP)

APPLICATION

General-purpose amplifier in control circuits of cassette decks, turntable, VTRs, video disc players and audio disc players; general-purpose amplifier in automotive electronic products, communications equipment and copying machines.

General-purpose amplifier in radio-controlled and electronic toys, and electronic games.





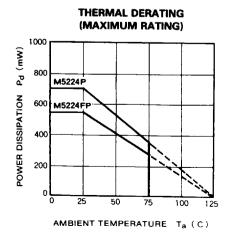
ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

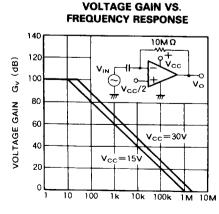
Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		36(±18)	V
Isink	Load current		1.50	mA
Isource	Edad current		±50	mA
Vid	Differential input voltage		±36	
Vi	Input voltage		-0.3~+36	V
Pd	Power dissipation		700(DIP)/550(FP)	mW
Kθ	Thermal derating	Ta≧25°C	7(DIP)/5.5(FP)	mW/°C
Topr	Ambient temperature		-20~+75	°c
T _{stg}	Storage temperature		-55~+125	Tc

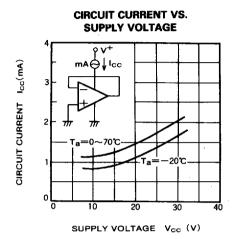
ELECTRICAL CHARACTERISTICS $(\tau_a=25^{\circ}c, v_{cc}=+15v)$

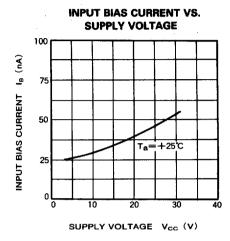
Symbol	Parameter	Test conditions	Limits			
			Min.	Тур.	Max.	Unit
Vio	Input offset voltage	A _S =∞		2	7	m∨
I _B	Input bias current			45	250	nA
lio	Input offset current			5	50	nA
V _{ICM}	Common phase input voltage width		0		V _{CC} -1.5	V
lcc	Circuit current	R _L =∞		1, 1	1.5	mA
G _{vo}	Open loop voltage gain	R _L ≥2kΩ	25	100		V/mV
V _o	Output voltage range	$R_L = 2k\Omega$	0		V _{CC} -1.5	V
CMRR	Common phase rejection ratio		65	85	00	dB
SVRR	Supply voltage rejection ratio		65	100	†	dB
CSR	Channel separation	f=1kHz~20kHz	1	120		₫B
Isource	Output source current	$V_{IN(+)}=1V, V_{IN(-)}=0V$	20	40		mA
Isink	Output sink current	$V_{1N(-)}=1V, V_{1N(+)}=0V$	10	20		mA
		$V_{IN(-)}=1V, V_{IN(+)}=0V, V_{O}=200mV$	12	50		μА

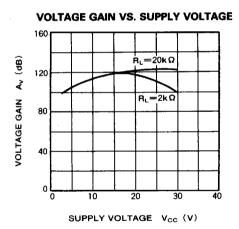
TYPICAL CHARACTERISTICS

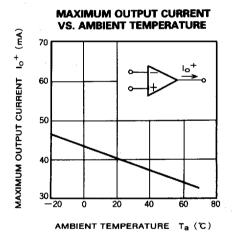


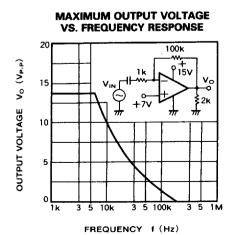


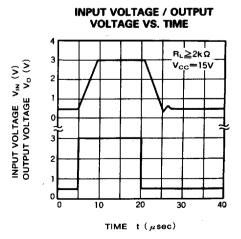


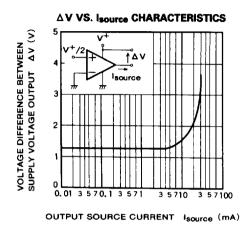


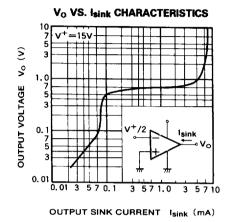












BASIC OPERATION OF SINGLE POWER SUPPLY OPERATIONAL AMPLIFIER

The M5224 is an operational amplifier that operates from OV (GND) level for both input and output if used at a single power supply voltage.

Basic operation of the device is explained in the following, comparing characteristics of the operational amplifier M5218.

Dual power supply operational amplifier

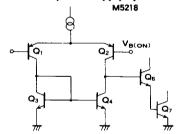


Fig. 1

Single power supply operational amplifier M5224

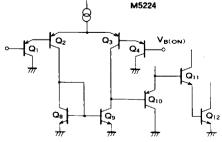


Fig. 2

Fig. 1 illustrates the dual power supply operational amplifier M5218, and Fig. 2 illustrates an input differential circuit of the single power supply operational amplifier M5224. In this case, the input stage base voltage VB(ON) for operating an input differential circuit in the M5218 is as follow;

$$V_{B(ON)} = V_{BE}7 + V_{BE}6 + V_{CE}2 - V_{BE}2$$

(If $V_{BE} = 0.6V$, $V_{CE} = 0.5V$)
= 1.1V

and, in the M5224.

$$V_{B(ON)} = V_{BE}12 + V_{BE}11 - V_{BE}10 + V_{CE}3 - V_{BE}3 - V_{BE}4$$

 $\doteqdot -0.1V$

and, in the M5224, the differential circuit is activated even when the input level is OV. The input and output characteristics are shown in Fig. 3.

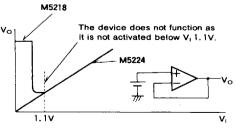


Fig. 3

Operation of an output stage is explained in the following.

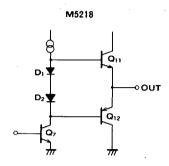


Fig. 4

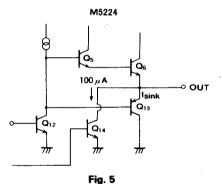


Fig. 4 illustrates an output stage of the M5218, which adopts and AB-class push-puss circuit of ordinary operational amplifier output type, where no crossover distortion occurs because idling current is running from D1, D2 bias to Q₁₁, Q₁₂ in guiescent state. In this case, the output never goes below the level of VBE12+VcE7, and the device is activated up to voltage of approximately 1.1V. Moreover, the voltage changes greatly according to conditions of load current.

Fig. 5 illustrates the M5224, to which rated current circuit of Ic≒100µA is connected by Q₁₄ and the output can be reduced to near GND level as A-class bias output stage up to the current of 100 µA. For a load in excess of this current, in case of the M5224 driven by Q13, no idling current is present because of C-class bias (where the base of output transistors Q5, Q6, Q13 are shorted), and crossover distortion occurs. Therefore, the device may not be suitable for audio signal amplifiers.

Both single and dual power supply amplifiers operate exactly with the same operating circuit logic (activation level of input and output and load driving methods are different), but bias must be set at V_{CC}/2 for output DC current in both single and dual power supply amplifiers.

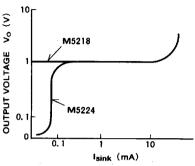


Fig. 6

REDUCTION OF DISTORTION IN A SINGLE POWER SUPPLY OPERATIONAL AMPLIFIER

As has been explained previously, a single power supply operational amplifier operates with low distortion as an A-class bias circuit up to a load condition that can be driven by current (100 μ A) in a rated current circuit which is built in the output stage, and it can be used for audio signals but, if the load condition exceeds the value of current, the device is placed into a C-class bias condition, and crossover distortion occurs. To reduce this distortion, a pull-up resistor (e.g. $3k \Omega$) for running A-class bias current externally can be connected as shown in Fig. 7 to increase the A-class bias current and reduce distortion. (Refer to Fig. 8 DISTOR-TION VS OUTPUT VOLTAGE.)

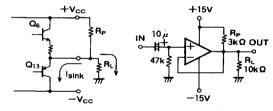


Fig. 7 (Explanation by dual power supply method)

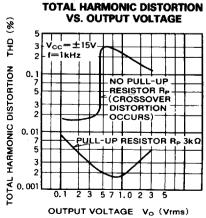


Fig. 8

