M52358VP

PAL JOG

DESCRIPTION

The M52358VP was developed for use with PAL-system VCRs. It processes variable speed playback signals.
This circuit has all signal processing circuits which are necessary to compensate color alignment during a variable speed playback using PAL-system VCRs.
This circuit consists of V-I converting circuit, TH/DL APC, 2-fsc PLL, color alignment detector, replacement burst circuit, AFC(f_H), BPF, timing pulse generator and fsc phase converter.

FEATURES

- The color alignment compensation system needs no 1 H delay line.
- No adjustment is necessary for AFC (f_H), TH/DL APC and 2-fsc PLL.
- The BPF has 2-fsc and 3-fsc traps. (fo: Adjusted automatically)
- A fsc phase converting circuit is built in. It is controlled by applying a voltage to pin 24 from an external source.
- Tuner system: PAL-M (3.58MHz) and 4.43-MHz NTSC-PAL

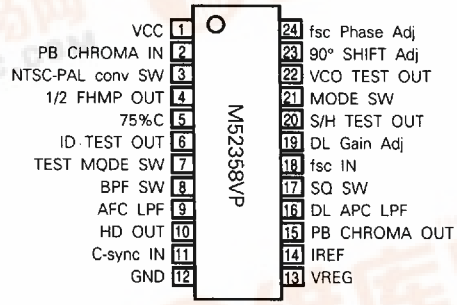
APPLICATION

PAL-system VCRs

RECOMMENDED OPERATING CONDITION

Operating Supply Voltage ..... 4.5 ~ 5.0V
Recommended Supply Voltage 4.75V

PIN CONFIGURATION (TOP VIEW)

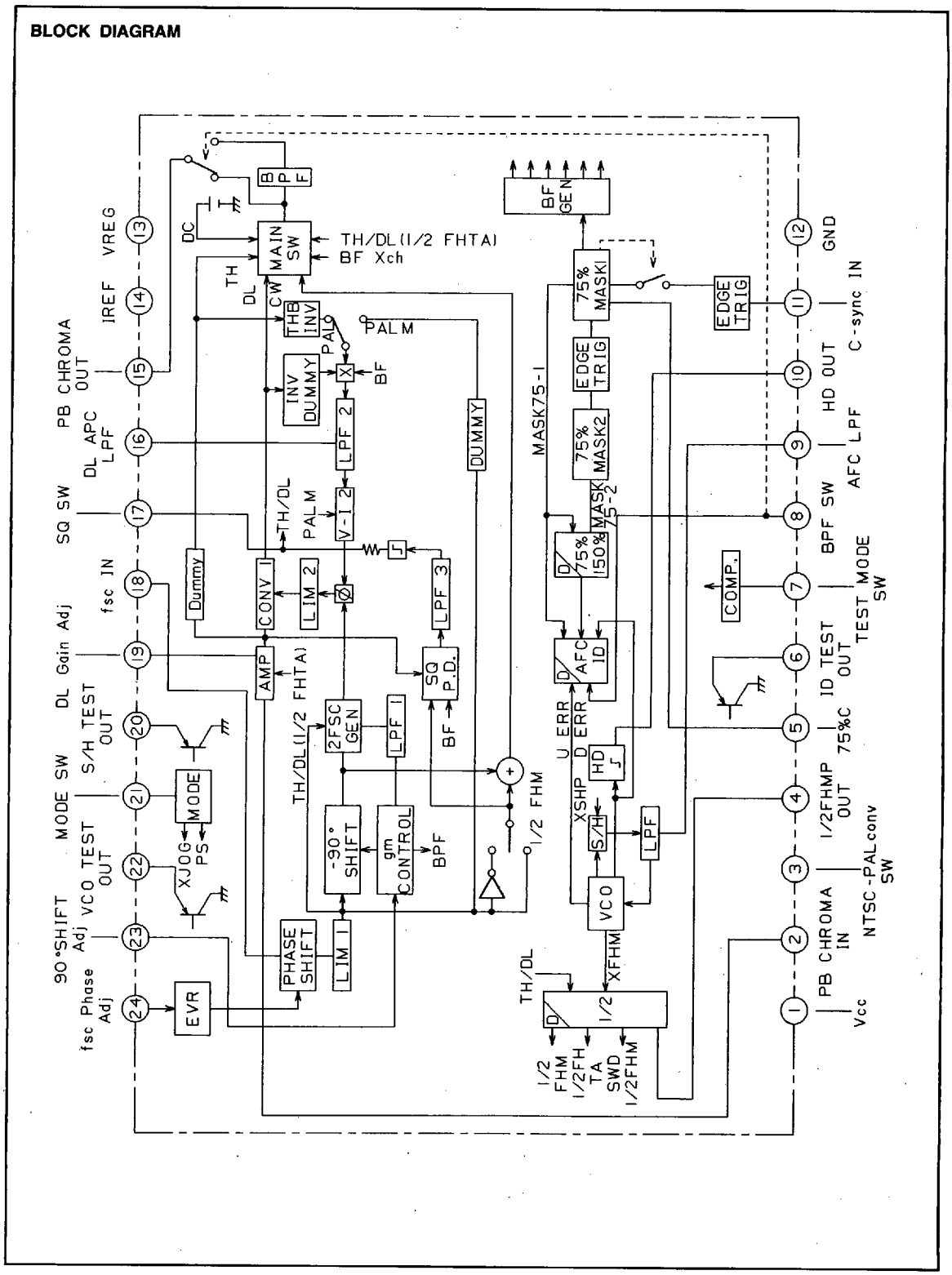


Outline 24P2E-A

M52358VP

PAL JOG

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6	V
P_d	Power dissipation	400 (500)	mW
T_{opr}	Operating temperature	−20~75	°C
T_{stg}	Storage temperature	−40~125	°C
K_θ	Thermal derating (Ta≧25°C)	4.0 (5.0)	mW/°C

Values in parentheses should apply when the IC is attached to a standard board.

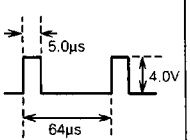
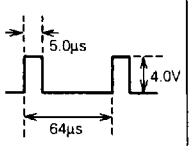
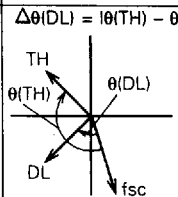
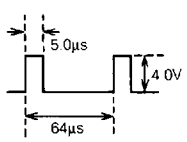
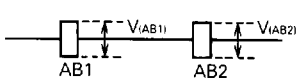
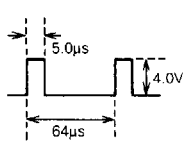
ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test point	Mode	Measuring procedure	Test conditions									Limits			Unit
					SW 5	SW 17	V_{CC}	V_2	V_3	V_5	V_7	V_{17}	V_{21}	V_{24}	Min.	Typ.	Max.	
$I_{CC\ (PB)}$	Circuit current (PAL PB BPF)	1	PAL PB BPF_{ON}	Measure DC amperage.			4.75 V	2.5 V	1.5 V				1.2 V	0V	25.0	32.0	40.0	mA
$I_{CC\ (PS)}$	Circuit current (PS mode)	1	PAL PS BPF_{ON}	Measure DC amperage.			4.75 V	2.5 V	1.5 V				0.8 V	0V	2.0	2.5	3.5	mA
$V_{REG\ (4.75)}$	VREG (4.75V)	13	PAL PB BPF_{ON}	Measure DC voltage.			4.75 V	2.5 V	1.5 V				1.2 V	0V	4.05	4.11	4.25	V
$V_{REG\ (4.5)}$	VREG (4.5V)	13	PAL PB BPF_{ON}	Measure DC voltage.			4.5 V	2.5 V	1.5 V				1.2 V	0V	4.05	4.11	4.25	V
$V_{REG\ (5.0)}$	VREG (5.0V)	13	PAL PB BPF_{ON}	Measure DC voltage.			5.0 V	2.5 V	1.5 V				1.2 V	0V	4.05	4.11	4.25	V
$V_{(IREF)}$	V (IREF)	14	PAL PB BPF_{ON}	Measure DC voltage.			4.75 V	2.5 V	1.5 V				1.2 V	0V	2.20	2.27	2.35	V
$G_{BPF\ (PAL)}$	TH BPF Gain (PAL)	15	PAL PB BPF_{ON}	Measure output level. (4.43 MHz)	○	○	4.75 V	2.5 V	1.5 V	3.4 V		3.0 V	1.9 V	0V	−1.5	0.2	2.0	dB
$G_{TRAP2\ (PAL)}$	2fsc TRAP Gain (PAL)	15	PAL PB BPF_{ON}	Measure output level. (8.86 MHz)	○	○	4.75 V	2.5 V	1.5 V	3.4 V		3.0 V	1.9 V	0V	−35	−27	−20	dB
$G_{TRAP3\ (PAL)}$	3fsc TRAP Gain (PAL)	15	PAL PB BPF_{ON}	Measure output level. (13.3 MHz)	○	○	4.75 V	2.5 V	1.5 V	3.4 V		3.0 V	1.9 V	0V	−40	−32	−20	dB
$G_{BPF\ (PAL-M)}$	TH BPF Gain (PAL-M)	15	PAL-M PB BPF_{ON}	Measure output level. (3.58 MHz)	○	○	4.75 V	2.5 V	1.5 V	3.4 V	0.5 V	3.0 V	1.9 V	0V	−1.5	0.2	2.0	dB
G_{TRAP2} (PAL-M)	2fsc TRAP Gain (PAL-M)	15	PAL-M PB BPF_{ON}	Measure output level. (7.16 MHz)	○	○	4.75 V	2.5 V	1.5 V	3.4 V	0.5 V	3.0 V	1.9 V	0V	−35	−28	−20	dB
G_{TRAP3} (PAL-M)	3fsc TRAP Gain (PAL-M)	15	PAL-M PB BPF_{ON}	Measure output level. (10.7 MHz)	○	○	4.75 V	2.5 V	1.5 V	3.4 V	0.5 V	3.0 V	1.9 V	0V	−40	−32	−20	dB
ΔG_{THDL}	TH/DL Gain ratio (PAL BPF)	15	PAL PB BPF	Measure output level.		○	4.75 V	2.5 V	1.5 V			2.0 V	1.9 V	0V	−0.7	−0.2	0.3	dB
$\Delta\theta_{DL\ (PAL)}$	TH/DL phase difference (PAL BPF)	15	PAL PB BPF	Measure phase.		○	4.75 V	2.5 V	1.5 V			2.0 V	1.9 V	0V	70	90	110	deg
$V_{AB\ (PAL)}$	TH/replacement burst level ratio (PAL BPF)	15	PAL JOG BPF	Measure output level.		○	4.75 V	2.5 V	1.5 V			3.0 V	2.3 V	0V	−13.3	−11.8	−10.3	dB
$\Delta V_{AB\ (PAL)}$	Replacement burst level ratio (PAL BPF)	15	PAL JOG BPF	Measure output level.		○	4.75 V	2.5 V	1.5 V			3.0 V	2.3 V	0V	−1.0	0	1.0	dB

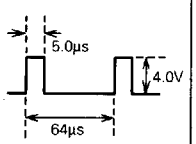
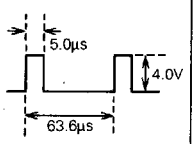
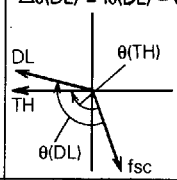
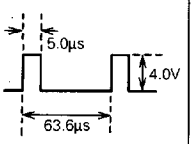
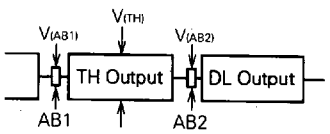
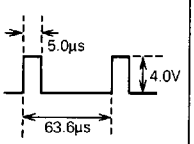
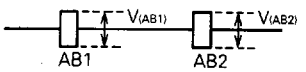
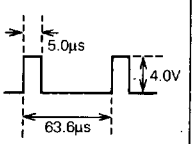
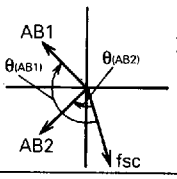
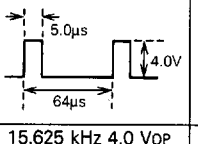
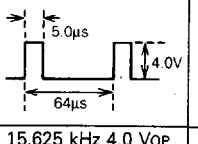
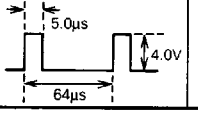
ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point	Mode	Measuring procedure	Test conditions										Limits			Unit
					SW 5	SW 17	Vcc	V_2	V_3	V_7	V_8	V_{17}	V_{21}	V_{24}	Min.	Typ.	Max.	
$\Delta\theta_{AB\ (PAL)}$	Replacement burst phase difference (PAL BPF)	15	PAL JOG BPF	Measure phase.		○	4.75 V	2.5 V	1.5 V			3.0 V	2.3 V	0V	85	90	95	deg
$\Delta\theta_{DL\ (PAL-M)}$	TH/DL phase difference (PAL-M BPF)	15	PAL-M PB BPF	Measure phase.		○	4.75 V	2.5 V	1.5 V	0.5 V		3.0 V	1.9 V	0V	−20	0	20	deg
$V_{AB\ (PAL-M)}$	TH/replacement burst level ratio (PAL-M BPF)	15	PAL-M JOG BPF	Measure output level.		○	4.75 V	2.5 V	1.5 V	0.5 V		3.0 V	2.3 V	0V	−13.3	−11.8	−10.3	dB
$\Delta V_{AB\ (PAL-M)}$	Replacement burst level ratio (PAL-M BPF)	15	PAL-M JOG BPF	Measure output level.		○	4.75 V	2.5 V	1.5 V	0.5 V		3.0 V	2.3 V	0V	−1.0	0	1.0	dB
$\Delta\theta_{AB\ (PAL-M)}$	Replacement burst phase difference (PAL-M BPF)	15	PAL-M JOG BPF	Measure phase.		○	4.75 V	2.5 V	1.5 V	0.5 V		3.0 V	2.3 V	0V	85	90	95	deg
SQ_{+V}	SQ DET +V detection	17	PAL PB BPF	Measure DC voltage.			4.75 V	2.5 V	1.5 V	3.8 V			1.9 V	0V	100		130	deg
SQ_{-V}	SQ DET −V detection	17	PAL PB BPF	Measure DC voltage.			4.75 V	2.5 V	1.5 V	3.8 V			1.9 V	0V	45		75	deg
CT_{TH}	Main SW crosstalk (Replacement burst → TH)	15	PAL PB BPF	Measure output level.		○	4.75 V	2.5 V	1.5 V			3.0 V	1.9 V	0V		−45	−40	dB
NT-PAL	4.43-MHz NTSC-PAL conversion check	15	NT-PAL PB BPF	Measure phase.			4.75 V	2.5 V	2.5 V				1.9 V	0V	−20	0	20	deg
$\theta_{fsc1\ (PAL)}$	fsc Phase Shift Phase variance 1 (PAL)	15	PAL JOG	Measure phase.		○	4.75 V	2.5 V	1.5 V			3.0 V	2.3 V	4.75 V	−21	−16	−11	deg
$\theta_{fsc2\ (PAL)}$	fsc Phase Shift Phase variance 2 (PAL)	15	PAL JOG	Measure phase.		○	4.75 V	2.5 V	1.5 V			3.0 V	2.3 V	1.8 V	12	17	22	deg
$\theta_{fsc1\ (PAL-M)}$	fsc Phase Shift Phase variance 1 (PAL-M)	15	PAL JOG	Measure phase.		○	4.75 V	2.5 V	1.5 V			3.0 V	2.3 V	4.75 V	−22	−17	−12	deg
$\theta_{fsc2\ (PAL-M)}$	fsc Phase Shift Phase variance 2 (PAL-M)	15	PAL JOG	Measure phase.		○	4.75 V	2.5 V	1.5 V			3.0 V	2.3 V	1.8 V	15	20	25	deg
T_{ABD}	TIMING Replacement burst delay	15	PAL JOG	Measure time.		○	4.75 V	2.5 V	1.5 V		2.2 V	3.0 V	2.3 V	0V	4.3	5.0	5.4	µs
T_{ABW}	TIMING Replacement burst width	15	PAL JOG	Measure time.		○	4.75 V	2.5 V	1.5 V		2.2 V	3.0 V	2.3 V	0V	2.9	3.2	3.6	µs
T_{CLD}	TIMING Burst cleaning delay	15	PAL PB	Measure time.		○	4.75 V	2.5 V	1.5 V		2.2 V	3.0 V	1.9 V	0V	7.5	8.2	8.7	µs
T_{CLW}	TIMING Burst cleaning width	15	PAL PB	Measure time.		○	4.75 V	2.5 V	1.5 V		2.2 V	3.0 V	1.9 V	0V	1.5	2.0	2.5	µs
T_{HDD}	AFC HD pulse delay	10	PAL PB	Measure time.			4.75 V	2.5 V	1.5 V				1.9 V	0V	−2.2	−1.2	−0.2	µs
T_{HDW}	AFC HD pulse width	10	PAL PB	Measure time.			4.75 V	2.5 V	1.5 V				1.9 V	0V	4.5	5.8	6.8	µs
$LOCK_D$	AFC LOCK Range (lower side)	10	PAL PB	Measure time.			4.75 V	2.5 V	1.5 V				1.9 V	0V	−50	0	50	Hz
$LOCK_U$	AFC LOCK Range (upper side)	10	PAL PB	Measure time.			4.75 V	2.5 V	1.5 V				1.9 V	0V	−50	0	50	Hz
ACK	ACK Check	15	PAL PB BPF	Measure output level.		○	4.75 V	0.25 V	1.5 V			3.0 V	1.9 V	0V		−45	−40	dB

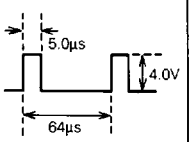
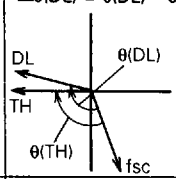
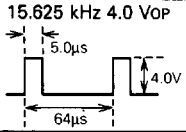
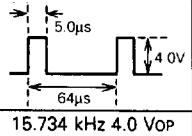
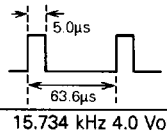
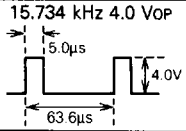
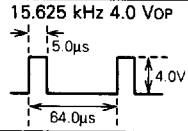
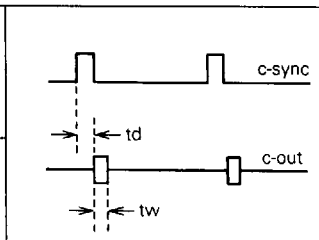
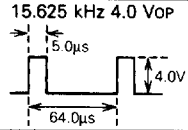
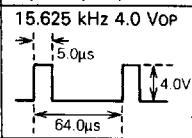
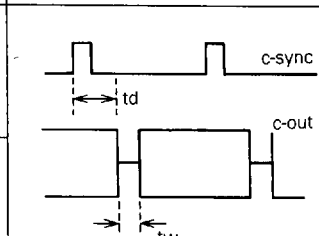
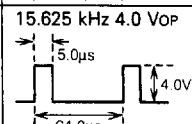
ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

Parameter	Input signals			Measuring procedure
	SG2	SG11	SG18	
Circuit current (PAL PB BPF)				
Circuit current (PS)				
VREG (4.75V)				Measure pin 13 DC voltage.
VREG (4.5V)				Measure pin 13 DC voltage.
VREG (5.0V)				Measure pin 13 DC voltage.
V (IREF)				Measure pin 14 DC voltage.
TH BPF Gain (PAL)	4.43 MHz CW 350 mVPP		4.43 MHz CW 350 mVPP	$20 \log \frac{\text{(pin 15 output 4.43–MHz element)}}{V_{SG2}}$
2fsc TRAP Gain (PAL)	8.86 MHz CW 350 mVPP		4.43 MHz CW 350 mVPP	$20 \log \frac{\text{(pin 15 output 8.86–MHz element)}}{V_{SG2}}$
3fsc TRAP Gain (PAL)	13.3 MHz CW 350 mVPP		4.43 MHz CW 350 mVPP	$20 \log \frac{\text{(pin 15 output 13.3–MHz element)}}{V_{SG2}}$
TH BPF Gain (PAL-M)	3.58 MHz CW 350 mVPP		3.58 MHz CW 350 mVPP	$20 \log \frac{\text{(pin 15 output 3.58–MHz element)}}{V_{SG2}}$
2fsc TRAP Gain (PAL-M)	7.16 MHz CW 350 mVPP		3.58 MHz CW 350 mVPP	$20 \log \frac{\text{(pin 15 output 7.16–MHz element)}}{V_{SG2}}$
3fsc TRAP Gain (PAL-M)	10.7 MHz CW 350 mVPP		3.58 MHz CW 350 mVPP	$20 \log \frac{\text{(pin 15 output 10.7–MHz element)}}{V_{SG2}}$
TH/DL gain ratio (PAL BPF)	4.43 MHz CW 150 mVPP	15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP (Adjust the input fsc phase such that the replacement burst phase will be at angles of 0° and 90° to that of output TH signals.)	$20 \log \frac{\text{(pin 15 DL mode output amplitude)}}{\text{(pin 15 TH mode output amplitude)}}$
TH/DL phase difference (PAL BPF)	4.43 MHz CW 150 mVPP	15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP (Adjust the input fsc phase such that the replacement burst phase will be at angles of 0° and 90° to that of output TH signals.)	$\Delta\theta(DL) = \lvert\theta(TH) - \theta(DL)\rvert$ (Measure TH and DL phases relative to the input fsc phase.) 
TH/replacement burst level ratio (PAL, BPF)		15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP (Adjust the input fsc phase such that the replacement burst phase will be at angles of 0° and 90° to that of output TH signals.)	 $20 \log \frac{V(AB1) + V(AB2)}{2 \times 350} - T7$
Replacement burst level ratio (PAL BPF)		15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP (Adjust the input fsc phase such that the replacement burst phase will be at angles of 0° and 90° to that of output TH signals.)	$\Delta V_{(AB)} = 20 \log \frac{V(AB2)}{V(AB1)}$

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Input signals			Measuring procedure
	SG2	SG11	SG18	
Replacement burst phase difference (PAL BPF)		15.625 kHz 4.0 V_{OP} 	4.43 MHz CW 350 mV_{PP} (Adjust the input fsc phase such that the replacement burst phase will be at angles of 0° and 90° to that of output TH signals.)	$\Delta\theta_{(AB)} = \lvert\theta_{(AB1)} - \theta_{(AB2)}\rvert$ (Measure the AB1 and AB2 phases relative to the input fsc phase.)
TH/DL phase difference (PAL-M, BPF)	3.58 MHz CW 150 mV_{PP}	15.734 kHz 4.0 V_{OP} 	3.58 MHz CW 350 mV_{PP} (Adjust the input fsc phase such that the replacement burst phase will be at angles of ±45° to that of output TH signals.)	$\Delta\theta(DL) = \lvert\theta(DL) - \theta(TH)\rvert$ (Measure TH and DL phases relative to the input fsc phase.) 
TH/replacement burst level ratio (PAL-M BPF)	3.58 MHz CW 150 mV_{PP}	15.734 kHz 4.0 V_{OP} 	3.58 MHz CW 350 mV_{PP} (Adjust the input fsc phase such that the replacement burst phase will be at angles of ±45° to that of output TH signals.)	 $20 \log \frac{V(AB1) + V(AB2)}{2 \times V(TH)}$
Replacement burst level ratio (PAL-M BPF)		15.734 kHz 4.0 V_{OP} 	3.58 MHz CW 350 mV_{PP} (Adjust the input fsc phase such that the replacement burst phase will be at angles of ±45° to that of output TH signals.)	 $\Delta V_{(AB)} = 20 \log \frac{V(AB2)}{V(AB1)}$
Replacement burst phase difference (PAL-M BPF)		15.734 kHz 4.0 V_{OP} 	3.58 MHz CW 350 mV_{PP} (Adjust the input fsc phase such that the replacement burst phase will be at angles of ±45° to that of output TH signals.)	$\Delta\theta(AB) = \lvert\theta(AB1) - \theta(AB2)\rvert$ (Measure the AB1 and AB2 phases relative to the input fsc phase.) 
SQ DET +V detection	4.43 MHz CW 150 mV_{PP} Delay the phase relative to fsc.	15.625 kHz 4.0 V_{OP} 	4.43 MHz CW 350 mV_{PP}	Measure the SG2 signal phase relative to fsc when pin 17 DC voltage changes from L to H (4.0 V).
SQ DET –V detection	4.43 MHz CW 150 mV_{PP} Delay the phase relative to fsc.	15.625 kHz 4.0 V_{OP} 	4.43 MHz CW 350 mV_{PP}	Measure the SG2 signal phase relative to fsc when pin 17 DC voltage changes from H to L (0 V).
Main SW crosstalk (Replacement burst → TH)		15.625 kHz 4.0 V_{OP} 	4.43 MHz CW 350 mV_{PP}	Measure the crosstalk with reference to the TH signal output timing.

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Input signals			Measuring procedure
	SG2	SG11	SG18	
4.43 MHz NTSC-PAL conversion check	4.43 MHz CW 150 mVPP	15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP (Adjust the input fsc phase such that the replacement burst phase will be at angles of ±45° to that of output TH signals.)	Δθ(DL) = θ(DL) − θ(TH) (Measure TH and DL phases relative to the input fsc phase.) 
fsc Phase Shift Phase variance 1 (PAL mode)		15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP	θ(AB) − θ(fix) (Measure replacement burst phase (θ1) relative to the input fsc phase. The fixed phase is expressed by θ (fix).)
fsc Phase Shift Phase variance 2 (PAL mode)		15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP	θ(AB) − θ(fix) (Measure replacement burst phase (θ1) relative to the input fsc phase. The fixed phase is expressed by θ (fix).)
fsc Phase Shift Phase variance 1 (PAL-M mode)		15.734 kHz 4.0 VOP 	3.58 MHz CW 350 mVPP	θ(AB1) − θ(fix) (Measure replacement burst phase (θ1) relative to the input fsc phase when pin 4 output DC voltage is "H" (4.0 V). The fixed phase is expressed by θ (fix).)
fsc Phase Shift Phase variance 2 (PAL-M mode)		15.734 kHz 4.0 VOP 	3.58 MHz CW 350 mVPP	θ(AB1) − θ(fix1) (Measure replacement burst phase (θ1) relative to the input fsc phase when pin 4 output DC voltage is "H". The fixed phase is expressed by θ (fix).)
TIMING replacement burst delay		15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP	td 
TIMING replacement burst width		15.625 kHz 4.0 VOP 	4.43 MHz CW 350 mVPP	tw
TIMING burst cleaning delay	4.43 MHz CW 350 mVPP	15.625 kHz 4.0 VOP 		td 
TIMING burst cleaning width	4.43 MHz CW 350 mVPP	15.625 kHz 4.0 VOP 		tw

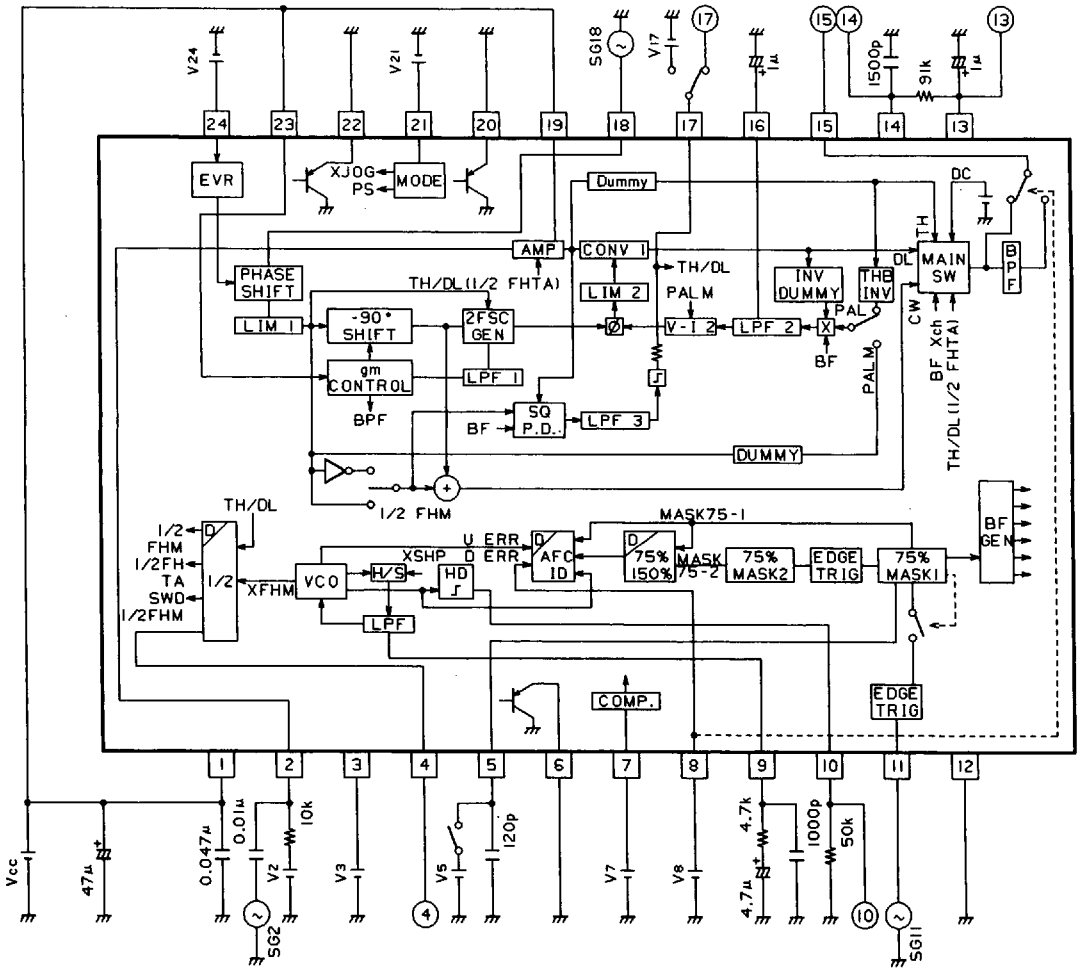
ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Input signals			Measuring procedure
	SG2	SG11	SG18	
AFC HD pulse delay		15.625 kHz 4.0 VOP 5.0µs 4.0V 64.0µs		td C-sync td 2.0V HD out tw
AFC HD pulse width		15.625 kHz 4.0 VOP 5.0µs 4.0V 64.0µs		tw
AFC lock range (lower side)		11.0 kHz 4.0 VOP 5.0µs 90.9µs		HD out t (SG11 input frequency) $-\frac{1}{t}$
AFC lock range (upper side)		18.0 kHz 4.0 VOP 5.0µs 55.6µs		HD out t (SG11 input frequency) $-\frac{1}{t}$
ACK Check	4.43 MHz CW 350 mVPP	18.0 kHz 4.0 VOP 5.0µs 55.6µs		20 log $\frac{\text{(pin 15 output amplitude)}}{V_{SG2}}$

M52358VP

PAL JOG

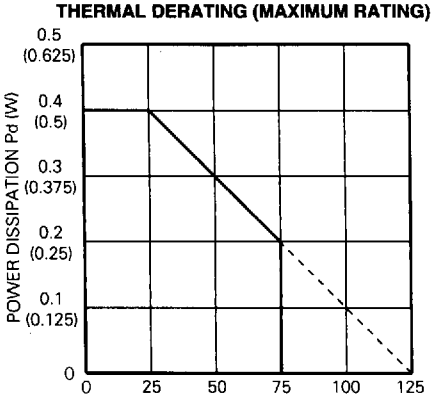
TEST CIRCUIT



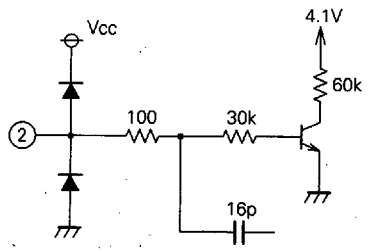
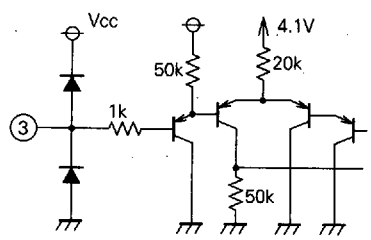
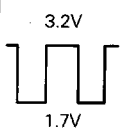
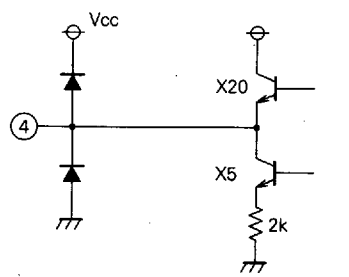
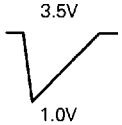
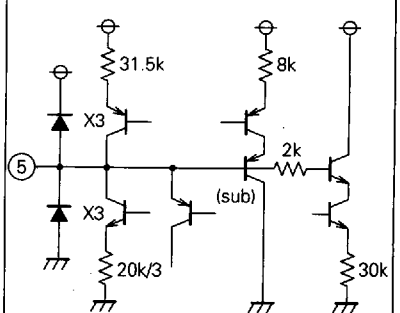
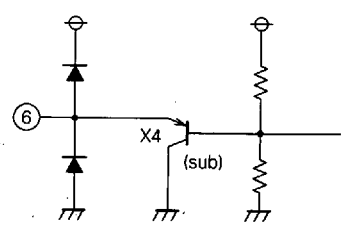
TYPICAL CHARACTERISTICS

Units Resistance: Ω
Capacitance: F

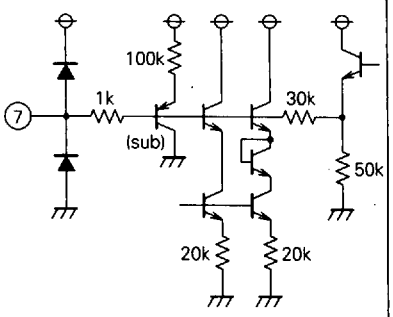
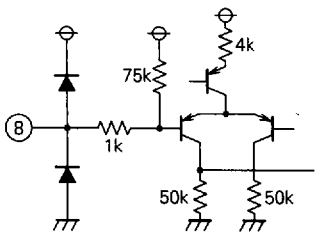
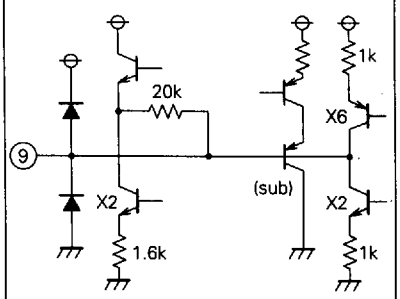
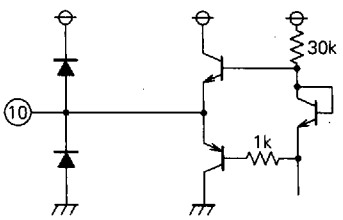
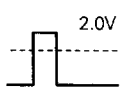
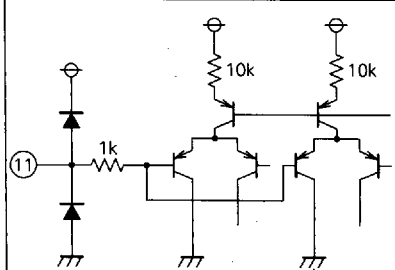
THERMAL DERATING (MAXIMUM RATING)



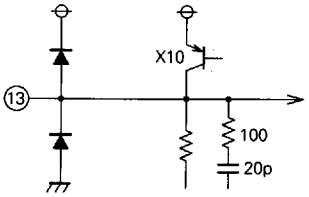
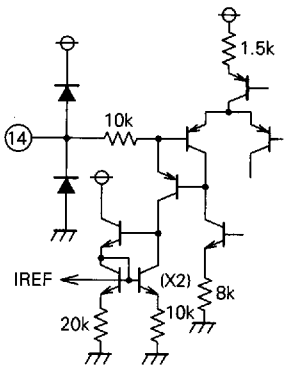
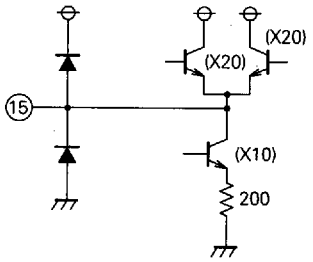
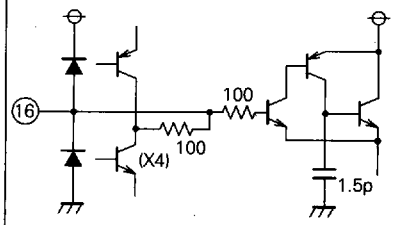
DESCRIPTION OF PIN

Pin No.	Name	Voltage and wave information DC	Voltage and wave information AC	Peripheral circuit of pins	Description of pin
①	Vcc	4.75V (reference)	——	——	● Supply voltage is applied to this pin.
②	PB C IN	——	350mVP-P 150mVP-P (burst)		● PB chroma signals are input to this pin. ● The chroma ACK is activated when the pin 2 DC bias is 0.7V or less. Pin ⑮ output is turned OFF.
③	NTSC-PAL SW	——	——		● The mode switches depending on a DC voltage supplied externally. PAL mode: 0V ~ 1.8V NTSC-PAL conversion: 2.2V ~ 4.75V ● The NTSC-PAL conversion mode automatically switches to the JOG mode and DL mode.
④	1/2 FHMP	——			● Pulses which are produced by dividing AFC (f_H–PLL) output by two are output.
⑤	75% C	——			● This pin leads charge/discharge capacitance that produces a triangular wave synchronous with C-sync. All timing pulses used in the IC are generated from this wave.
⑥	AFC ID OUT	3.5V (H) 3.0V (M) 2.5V (L)	——		● AFC ID is output in the TEST mode.

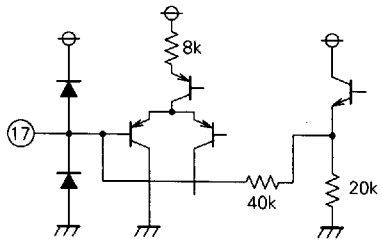
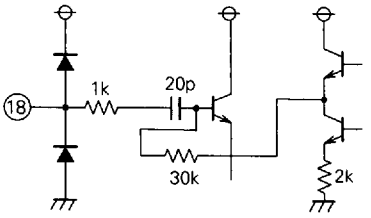
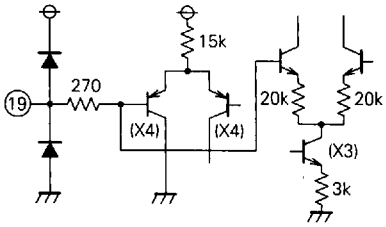
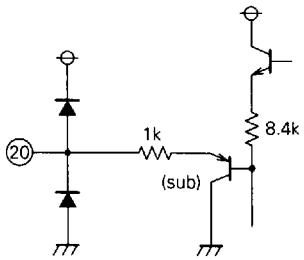
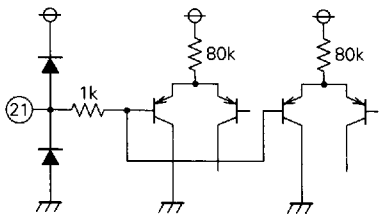
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information DC	Voltage and wave information AC	Peripheral circuit of pins	Description of pin
⑦	TEST MODE SW	——	——		● The mode switches depending on a DC voltage supplied to this pin externally. PAL-M: 0 ~ 0.5V PAL : open RESET: 3.6 ~ 4.1V TEST : 4.3 ~ .4.75V
⑧	BPF SW	——	——		● The mode switches depending on a DC voltage applied to this pin externally. BPF ON : 2.6 ~ 4.75V BPF OFF: 0 ~ 2.2V ● TEST VCOP is input in the TEST mode.
⑨	AFC LPF	2.0V	——		● This pin leads the constant in AFC (f_H-PLL) LPF.
⑩	HD	——			● HD pulses generated in AFC (f_H-PLL) are output.
⑪	C Sync	——			● The composite sync is input. The external threshold is 2.0V. The polarity is "active High."

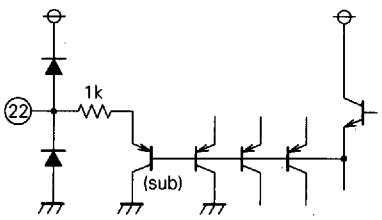
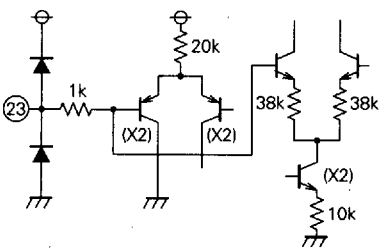
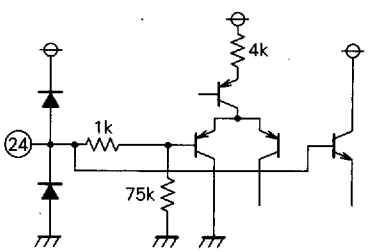
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information DC	Voltage and wave information AC	Peripheral circuit of pins	Description of pin
⑫	GND	———	———	———	• This pin is used for grounding.
⑬	VREG	4.11V	———		• The IC reference voltage source (4.11V) is output.
⑭	IREF	2.27V	———		• This pin leads reference resistance that generates IC reference current source.
⑮	C OUT	2.5V	350mV$_{P-P}$ 150mV$_{P-P}$ (burst)		• PAL PB signals (TH/DL replacement burst) and PAL-M signals output.
⑯	DL APC LPF	1.8V	———		• This circuit leads the constant in TH/DL APC loop LPF. • The TH/DL lock phase is changed by applying an external DC current to this pin.

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information		Peripheral circuit of pins	Description of pin
		DC	AC		
⑰	SQ ID	4.0V (H) 0V (L)	——		● The SQ detector is output. ● Pin ⑮ output signals are automatically switched to TH or DL by applying an external DC voltage to this pin. DL: 0 ~ 2.0V TH: 3.0 ~ 4.75V
⑱	fsc IN	——	350mVP-P		● "fsc" (color sub-carrier wave) is input.
⑲	DL GAIN ADJ	4.75V (reference)	——		● This pin is used to adjust DL signal gain. The gain is varied depending on a DC voltage applied to this pin. The gain is fixed internally with a voltage of 4.75V.
⑳	S/H OUT	——	3V 2.95V		● The S/H circuit is output in the TEST mode.
㉑	MODE	——	——		● The mode is switched depending on a DC voltage applied to this pin externally. PS: 0 ~ 0.8V PB: 1.2 ~ 1.8V JOG: 2.3 ~ 4.75V

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Voltage and wave information		Peripheral circuit of pins	Description of pin
		DC	AC		
㉒	VCO OUT	——			● VCO is output in the TEST mode.
㉓	ϕ ADJ	4.75V (reference)	——		● This pin is used to adjust the replacement burst phase. The phase is varied depending on a DC voltage applied to this pin externally. It is fixed internally with a voltage of 4.75V.
㉔	fsc PHASE ADJ	0V (reference)	——		● This pin is used to adjust the externally-input fsc phase. The phase is varied depending on a DC voltage applied to this pin externally. It is fixed internally with a voltage of 0V.

DESCRIPTION OF MODES

Mode	Control pin	Voltage	Description
—	Pin 3	0~1.5V	Used in the PAL mode.
NTSC-PAL conversion		2.5~4.75V	When NTSC signals (3.58 MHz or 4.43 MHz) are input to pin 2, conversion PAL signals are output to pin 15. The mode is switched to JOG and DL automatically.
PAL-M		0~0.5V	The mode is fixed to PAL-M. When pin 3 is set to "H," or the mode is DL or JOG, the mode is switched to the NTSC (3.58 MHz)-PAL conversion.
PAL	Pin 7	Open	The mode is fixed to PAL. When pin 3 is set to "H," the mode is switched to the NTSC (4.43 MHz)-PAL conversion.
RESET		3.6~4.0V	The AFC (f_H-PLL) logic section (AFC ID, 150% mask, 1/2 divider) is turned OFF.
TEST		4.4~4.75V	Checks the operation of AFC (f_H-PLL) AFC ID, VCO and S/H block.
BPF OFF	Pin 8	0~2.2V	The internal BPF is turned OFF. Signals that are not through it are output to pin 15.
BPF ON		Open	Pin 15 outputs signals that are through the internal BPF.
DL	Pin 17	0~2.0V	Pin 15 outputs DL signals.
AUTO		Open	Pin 15 outputs TH or DL signals depending on judgment by the SQ detector.
TH		3.0~4.75V	Pin 15 outputs TH signals.
PS	Pin 21	0~0.8V	The REC power save is turned on.
PB		1.2~1.8V	PB mode
JOG		2.3~4.75V	Replacement burst signals are inserted to a real burst signal section during PAL playback.