**MITSUBISHI ICs (AV COMMON)** 

M52693SP

#### **BURST LOCK CLOCK GENERATOR**

#### DESCRIPTION

The M52693SP is a semiconductor integrated circuit developed for analog signal processing of a picture-in-picture system, consisting of a sync separator, an ACC, a burst lock clock generator circuit, an analog switch and a clamp circuit, etc. It is also available on digital video signal systems other than the above.

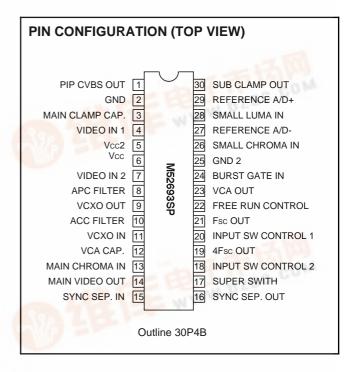
#### **FEATURES**

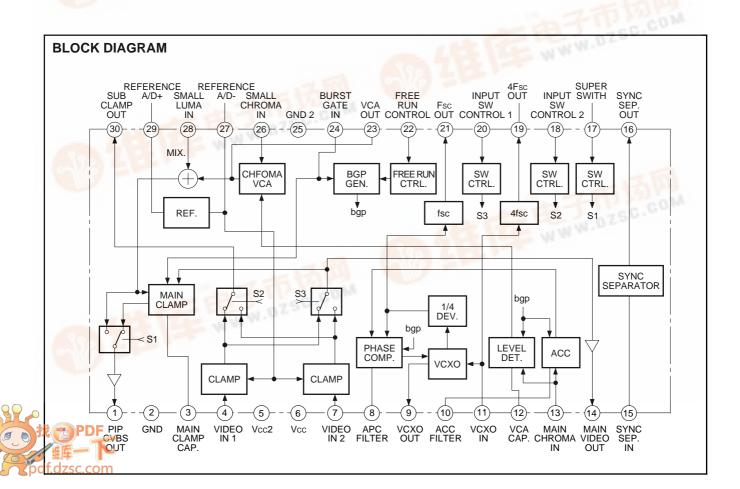
- Low power dissipation of supply voltage 5.0V and circuit current 32mA (Typ.)
- Built-in 4fsc burst lock clock generator circuit required for digital video signal processing
- Small picture chroma level following main picture burst level
- Main picture pedestal level matching small picture pedestal level
- Built-in reference voltage source for A/D converter

#### **APPLICATION**

TV, VCR

#### RECOMMENDED OPERATING CONDITION





#### **BURST LOCK CLOCK GENERATOR**

#### ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
Vcc	Supply voltage	6.0	V
Pd	Power dissipation	1265	mW
Topr	Operating temperature	-20 to +75	°C
Tstg	Storage temperatare	-40 to +125	°C

## **BURST LOCK CLOCK GENERATOR**

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														<u>∃</u>	Test conditions	inditi	suo													Limits		
Svmbol	Parameter	Test									Д	in cc	Pin conditions	ions										Swi	tch c	Switch conditions	tions					Unit
		pin	4	5	9	2	11	13	14	15	16	17	18	19	20 2	21 2	22 23	23 2	26 27	7 28	8 29	9 30		/S/v	/SW 11	/SW 13	SW 26	SW 28	SW SW SW SW SW Min. Typ. Max 4 7 11 13 26 28	Typ.∧	Лах.	5
၁၁	Circuit current	99	SG 1	5.0 V	5.0 V	I	I	SG 2	_	PG 1	1	0 >	5.0	1	5.0 V	1	- - ->	<u>'</u> 			1	ı	q	ď	OFF	۵	B	а	20.8	32.0	43.2	mA
Vin1	Video signal input 1 output voltage	4	I	5.0	5.0	ı	ı	ı	I	D -	ı	0 >	5.0	ı	5.0	1	0 >	'	'	1		I	ď	ď	N O	ď	ď	a	2.16	2.41	2.66	>
Vin2	Video signal input 2 output voltage	0	ı	5.0	5.0	ı	ı	ı	I	g -	ı	0 >	> 5.0	1	5.0	1	0 >	<u> </u>	'			1	ď	ď	N O	a	ď	ď	2.16	2.41	5.66	>
Vвн	Reference voltage H	8	ı	5.0	5.0	ı	ı	ı	1	2 t	1	0 >	5.0	ı	5.0	1	0 >	'				I	a	ď	Z O	ď	ď	ď	3.60	3.75	3.90	>
VRL	Reference voltage L	(2)	ı	5.0	5.0	1	ı	ı	ı	ე +	ı	0 >	5.0	ı	5.0	1	0 >	' I	ı	1		ı	ď	ď	N O	ď	ď	ď	2.18	2.33	2.48	>
VB	(VRT - VRB) voltage	1	ı	5.0	5.0	ı	ı	I	I	- PG	ı	0 >	5.0	ı	5.0	1	0 >	'		1		I	ď	ď	o O	ď	ď	a	1.27	1.42	1.57	>
Vsон	Sync separation signal output voltage H	9	I	5.0 V	5.0 V	I	I	I	I	PG +	ı	0 >	5.0	1	5.0	1	0 >	'	1			I	ď	ď	O N	a	ď	a	3.40	4.20	ı	>
Vsol	Sync separation signal output voltage L	9	ı	5.0	5.0	ı	ı	ı	1	- PG	1	0 >	5.0	1	5.0	1	0 >	' I	'			I	ď	ď	NO NO	ď	ď	ď	ı	0.90	1.20	>
耳	Sync separation signal output pulse width	9	ı	5.0	5.0	I	ı	I	I	- PG	ı	0 >	5.0	1	5.0	1	0 >	'	'	1		I	ď	ď	N O	ď	ď	ď	5.00	5.30	5.80	sm
ноч	Sync separation signal output delay time	(1)	ı	5.0 V	5.0 V	I	ı	I	I	PG +	ı	0 >	5.0	ı	5.0	1	0 >	'	'	-		ı	Ø	ď	N O	Ø	જ	ď	ı	0.12 (	0:30	sn
Sync-in	Sync separation signal input level	9	ı	5.0	5.0	I	ı	I	I	- PG	ı	0 >	5.0	ı	5.0	1	0 >	ı '	'			ı	ď	ď	o O	ď	ď	ø	0.10	0.30	09.0	Vp-р
Vsub	Video signal output voltage (small picture system)	60	ı	5.0 V	5.0 V	I	I	I	Ι	PG 1	ı	0 >	5.00	- 2	0V 5.0V		0 ^	<u>'</u> 	<u>'</u>	-	<u> </u>	I	В	ď	O	В	ď	В	2.25	2.40	2.55	>
AVSRB	Clamp offset	8	1	5.0 V	5.0 V	I	ı	I	I	PG 	ı	0 >	5.00	- 1 - 2	00.5	1	0 >	1		-		I	ď	a	O N	ď	ø	a	30	09	06	/m
ganp	Video signal output gain (small picture system)	8	SG 1	5.0 V	5.0 V	SG 1	ı	I	_	PG 1-	ı	0 >	5.00	1	5.0	1	0 >	'	1	1		1	q	٩	o O	a	ď	a	-1.00	0	1.00	ф
CTSUB	Video signal output crosstalk (small picture system)	30	SG3	5.0 V	5.0 V	SG3	1	I	ı	PG 1-	1	0 >	5→0V 0→5V	1	5.0 V	1	0 >	<u>'</u>		-	1	ı	b/a	t b/a	NO	В	ď	В	ı	-55	-45	dB
fBWsub	Video signal output frequency band (small picture system)	6	SG 4	5.0 V	5.0 V	SG 4	ı	ı	1	PG 1-	ı	0 >	5.0V 0V	1	5.0		0 >	<u>'</u>	<u>'</u> 	 	<u> </u>	ı	q	q	N O	В	a	В	10	ı	ı	MHz
Vmain	Video signal output voltage (main picture system)	<b>(4)</b>	1	5.0 V	5.0 V	I	ı	I	I	PG-	1	0 >	5.0	- 2	5.0V 0V	1	0 >	'	1	1		I	Ø	ď	N O	Ø	ď	Ø	1.20 1.45		1.70	>
Gmain	Video signal output gain (main picture system)	(14)	SG 1	5.0 V	5.0 V	SG 1	ı	ı	1	PG 1-	1	0 >	5.0	- 2	5.0V 0V	1	0 >	'	'			I	q	q	NO N	В	В	В	1.3	2.3	3.3	dB
										1		1									l	l	l								l	

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise noted)

## **BURST LOCK CLOCK GENERATOR**

														⁴	1 5	Test conditions	1 2												L	imit	I.	
		_												Ď	3		2						-					T				
Symbol	- Parameter	Test			İ				İ		۱	in co	Pin conditions	ons				}			-	-		Swit	Switch conditions	ondii	tions					Unit
`		oint	4	5	9	7	11	13	14	15	16	17	18	6	20 2	21 2	22 23	3 26	3 27	7 28	29	30	SW 4	/SW	13€ 11	SW 13	SW 26	SW SW SW SW SW Min. Typ. Max. 7 11 13 26 28	Min	Typ.	Max.	
CTmain	Video signal output crosstalk (main picture system)	<b>(4)</b>	SG3	> >	> 5.0	SG3	I	ı	ı	₽ <del>-</del>	ı	0 >	5.0	  r	5-0V 0-5V	0 /	0 >			1	ı	ı	b/a	a/b	8	ď	ď	ď	ı	-55	-45	ВВ
fBW <sub>main</sub>	Video signal output frequency band (main picture system)	(14)	SG 4	5.0	5.0	SG 4	I	ı	I	g +	ı	0 >	5.0	ا 0	5.0V 0V	0 /	0 >			1	I	I	۵	۵	o O	Ø	B	ø	10	I	ı	MHz
VPIP	PIP output voltage (Sub)	1	ı	5.0	5.0	I	I	ı	ı	- R	1	5.0 8	5.0	ιω ·	5.0	0 /	0 >	1		1	ı	ı	ď	Ø	N O	ď	В	g	1.40	1.65	1.90	>
AVPIP	PIP output clamp offset	_	ı	5.0	5.0	1	I	ı	ı	- RG	ı	0 >	5.0	- 5.	5.0V -	0 /	0 >			1	ı	ı	a	a	o O	ď	g	a	0	ı	15	μV
GPIPSC	PIP output gain (Sub-C)	ı	Ι	5.0 V	5.0	-	_	1	1	RG 1	1	5.0 8	5.0	٦	5.0	-	0 /	SG - 5	(5	1	I	1	Ø	ď	N O	ď	q	В	4.3	5.3	6.3	dВ
GPIPSI	PIP output gain (Sub- Luma)	1	ı	5.0 V	5.0 V	1	_	ı	1	RG 1	1	5.0 t	5.0 V	- 5	5.0	0 /	0 /	<u> </u>		SG e	I I	ı	Ø	ď	O O	ß	В	q	4.6	5.6	9.9	dВ
GPIP	PIP output gain	ı	SG 1	5.0	5.0	SG 1	I	ı	ı	유 -	ı	0 >	5.0	ا 0	5.0V 0V	1	0 >			1	I	ı	٩	۵	o O	ď	ø	ø	4.3	5.3	6.3	фB
fBWPIP	PIP output frequency band	ı	SG 4	5.0	5.0	SG 4	I	I	ı	- RG	I	0 >	5.0	ا نی	5.0V 0V	1	0 >			1	I	I	Q	Q	N O	ď	Ø	ď	10	I	ı	MHz
fBWPIPS	PIP output frequency band (s)	ı	ı	5.0	5.0	ı	ı	ı	ı	₽ -	ı	5.0 5	5.0	ا س	5.0	. 5	5.0	SG 7	(5.	1	ı	ı	ď	ď	o O	ď	Ω	ø	10	1	ı	MHz
СТРІР	PIP output crosstalk	ı	ဗ္ဗဇ	> 2.0	5.0	SG 8	I	ı	ı	- B	1	2,000	5.0	I S	5.00	0 /	0 >			1	ı	I	۵	۵	8 O	ď	ď	a	I	-50	-45	ВВ
CTPIPS	PIP output crosstalk (s)	ı	ı	> >	5.0	ı	I	SG 2	ı	- B	1	3,→3	5.0	ا ا	5.07	,	0 >	SG	(7	1	ı	ı	ď	ď	o O	۵	Ω	ď	I	-50	-45	ВВ
VCAtyp.	VCA output	8	ı	5.0	5.0	ı	I	SG 2	ı	- R	I	0 >	5.0	ري ا	5.0	1	0 >	SG	(7	1	I	ı	ď	ď	o O	۵	Ω	ø	2.0	3.5	5.0	ф
VCAmax	VCA control maximum	8	_	5.0	5.0 V	ı	ı	SG 2	1	RG 1	ı	0 >	5.0 V	(J)	5.0 V		- ^	SG 5	(7	1	ı	ı	В	ø	O	q	q	а	7.0	8.5	10.0	dВ
VCAmin.	VCA control minimum	8	ı	5.0	5.0	ı	ı	SG _2	ı	- RG	ı	0 >	5.0	ا ت	5.0	1	0 >	SG	(7	1	ı	ı	ď	ď	N O	Ω	q	a	-12.0	-9.0	-6.0	ф
Gmax.	VCA control maximum gain	8	ı	5.0	5.0	ı	ı	S -2	ı	윤 -	ı	0 >	5.0	ري	5.0	- 55	5.0	SG -	(7	1	I	ı	ß	ď	8	۵	۵	ď	0.8	2.8	4.8	ВВ
Lvca	VCA output leak	83	_	5.0 V	5.0 V	_	I	I	1	RG 1	I	0 >	5.0 V	- 5	5.0 V	-	- ^	SG	(7	1	I	Ι	В	В	O	B	q	я	-	1	0.6-	dВ
ſFR	VCXO free running frequency	<b>(1)</b>	_	5.0	5.0	_	_	I	1	RG 1	I	0 >	5.0 V	- 5	5.0 0.5	0 >		-	-	1	I	1	В	В	OFF	В	a	а	-	14.318	I	MHz
<b>V4f</b> scн	4fsc output voltage H	<b>(</b>	I	5.0	5.0	ı	I	sg 2	ı	- PG	ı	0 >	5.0	ا ک	5.0 (	0 >			1	1	I	1	ď	ď	9	Q	ď	В	3.4	3.9	I	>

# ELECTRICAL CHARACTERISTICS (cont.)

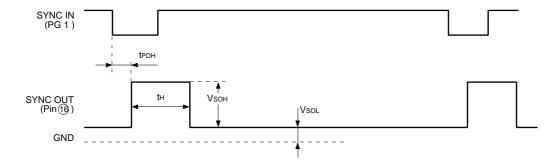
#### **BURST LOCK CLOCK GENERATOR**

	II I	<u> </u>	>	>	>	MHz	MHz	HZ	Ŧ	Vp-p
<b>"</b>		SW SW SW SW SW SW Min. Typ. Max. 4 7 11 13 26 28	0.5	ı	0.5	ı	ı	ı	-1200 -400	0.10 0.20
Limits		Typ.	0.1	3.9	0.1	14.318	3.5795	650	-1200	0.10
		Min.	ı	3.4	I	ı	ı	400	1	0.01
		SW 28	ď	ď	ď	ď	ď	ď	ď	ď
	ions	SW 26	જ	ಹ	ď	ď	ત	ď	ď	ત્ય
	Judit	SW 13	۵	۵	۵	۵	۵	۵	۵	۵
	Switch conditions	SW SW 11 13	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
	Swit	SW 7	ø	ď	ď	ď	ત	ď	ď	ø
		SW 4	ď	ď	ď	ď	ď	ď	ď	ď
		30	ı	ı	ı	ı	- 1	ı	ı	ı
		29	ı	I	ı	ı	ı	I	I	ı
		28	ı	ı	ı	ı	I	I	I	ı
		27	ı	I	ı	ı	I	I	I	ı
		26	ı	I	ı	ı	I	I	I	ı
s		23	ı	I	ı	- 1	I	I	I	ı
Test conditions		22	ı	ı	ı	ı	I	ı	ı	ı
cond		21	0 >	0 >	0 >	0 >	0 >	0 >	0 >	0 >
est	(N	20	> >	5.0	5.0	5.0	5.0	5.0	5.0	5.0
_	Pin conditions	19	ı	ı	I	I	I	ı	ı	ı
	puo	18	> >	5.0	5.0	5.0	5.0	5.0	5.0	5.0
	Pin (	17	0 >	0 >	0 >	0 >	0 >	0 >	0 >	0 >
		16	ı	ı	ı	ı	ı	ı	ı	ı
		15	원 <del>-</del>	g -	გ <b>-</b>	g -	g -	g -	გ <del>-</del>	<u>გ</u> –
		14	ı	ı	I	ı	ı	ı	ı	1
		13	SG 2	SG 2	Sg 2	Sg ~	S <sub>G</sub>	SG 8	S &	SG2' SG2'
		7	ı	ı	I	ı	I	ı	ı	ı
		7	ı	ı	I	ı	I	ı	ı	ı
		9	> >	5.0	5.0	5.0	5.0	5.0	5.0	5.0
		5	> >	5.0	5.0	5.0	5.0	5.0	5.0	5.0
		4	ı	ı	ı	1	ı	ı	ı	ı
	Test	point	•	(a)	8	•	8	•	•	•
	Parameter		4fsc output voltage L	fsc output voltage H	fsc output voltage L	4fsc output frequency	fsc output frequency	Capture range (+)	Capture range (-)	Chroma signal input level (burst)
	Symbol	i i	V4fscL	<b>Vf</b> scн	VfscL	4fsc	fsc	fcP (+)	fcP (-)	0-IN

#### **BURST LOCK CLOCK GENERATOR**

#### **ELECTRICAL CHARACTERISTICS TEST METHOD**

#### VR VR=VRH-VRL VSOH, VSOL, tH and tPDH



#### Sync-in

Measure th and tPDH when the input amplitude of pin  $^{\textcircled{1}}$  is 0.1VP-P. Make sure that th and tPDH are within the allowable range. When the input amplitude of pin  $^{\textcircled{1}}$  is 0.6VP-P, make sure that th and tPDH are within the allowable range.

#### Vsub and VSRB

Measure pin  $\,\,^{\mbox{\tiny $30$}}$  DC output voltage in correspondence to the "H" and "L" states of pin  $\,^{\mbox{\tiny $30$}}$  .

If the voltage which appears at pin 3 when pin 1 is "H" is taken as Vsub1, and the voltage which appears at pin 3 when pin 1 is "L" is taken as Vsub2, the clamp offset is given by the following expression:

DVsrB = (Vsub1 - V27), (Vsub2 - V27)

#### Gsub

Measure pin @ gain in correspondence to the "H" and "L" states of pin  $\textcircled{\tiny{18}}$  .

#### CTsub, Cmain, and CTPIP

Measure crosstalk under the following input conditions:

Pran	neter	Input signal	Swit	nnection ching co it coditio	ondition:	Left			
			4	ŀ	7	7	17	18	20
CTsub	CTsub 1	Sine wave	b	IN	а		0V	5 ⇒ 0V	0V
CTSUD	Ctsub 2	Amplitude	a		b	_ <u>IN</u>	ŌV	0 ⇒ 5V	
CTmain	CTmain 1	: 0.3VP-P	b	IN	а		0V	0V	5 ⇒ 0V
Crinain	CTmain 2	Frequency	а		b	ĪÑ	0V	0V	0 ⇔ 5V
СТыр	CTPIP 1	: 3.58MHz	b	IN	а		0 🖒 5V	0V	5V
CTPIP	CTPIP 2	· 3.36IVITZ	а		_ b	ĪN	0 ⇒ 5V	0V	0V

#### **fBWsub**

Measure pin 30 frequency characteristics in correspondence to the "H" and "L" states of pin 10 Condition: -3dB

#### **Vmain**

Measure pin  $^{(4)}$  DC output voltage in correspondence to the "H" and "L" states of pin( $^{(2)}$ ).

#### Gmain

Measure pin  $^{\textcircled{4}}$  gain in correspondence to the "H" and "L" states of pin  $^{\textcircled{20}}$  .

#### **fBWmain**

Measure pin (4) frequency characteristics in correspondence to the "H" and "L" states of pin (2). Condition: -3dB

#### VPIP

If the voltage which appears at pin ① when pin ② is "H" is taken as Vpip1, and the voltage which appears at pin 1 when pin ② is "L" is taken as Vpip2, VPIP is given by the following expression:

VPIP = Vpip1 - VPIP , Vpip2 - VPIP

## MITSUBISHI ICs (AV COMMON)

### M52693SP

#### **BURST LOCK CLOCK GENERATOR**

#### **GPIPSC**

Pin 2 = 2.185V V1 = Amplitude of pin 1 V23 = Amplitude of pin 2 GPIPSC = 20 log (V1/V23)

#### **GPIP**

Measure pin  ${\bf \widehat{\ \ }}$  gain in correspondence to the "H" and "L" states of pin  ${\bf \widehat{\ \ }}$  ).

#### **fBWPIP**

Measure pin ① frequency characteristics in correspondence to the "H" and "L" states of pin ② Condition: -3dB

#### **fBW**PIPS

Condition: -3dB

#### **CTPIPS**

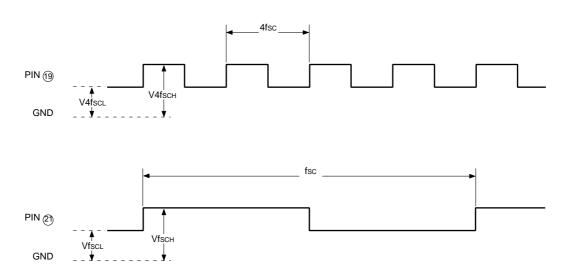
Apply 5.0V to pin 3. Define as VOS1 the amplitude which appears at pin 1 a when pin 2 is "H", and as VOM1 the amplitude which appears when pin 2 is "L". Then apply 0V to pin 3. Define as VOS2 the amplitude which appears at pin 1 when pin 2 is "H", and as VOM2 the amplitude which appears at pin 1 when "L". CTPIPS is given under the above conditions by the equation given below.

CTPIPS=20log (VOMI/VOSI), 201log (VOM2/VOS2)

## VCAtyp, VCAmax, VCAmin, Gmax, Lvca 20 log {(amplitude of pin 23)/SG5}

#### V4fscH, L; VfscH, L; 4fsc; fsc

Make sure that the input signal at  $pin_{\Large \textcircled{3}}$  is synchronous with the output signal at  $pin_{\Large \textcircled{9}}$  .



#### fcp (+)

- 1) Raise the frequency of SG8 input signal so that the signal is synchronous with pin (1) output signal.
- 2) Lower the SG8 frequency.
- 3) Measure the SG8 frequency (f1) when the SG8 input signal is synchronous with the pin (19) output signal.
- 4) fcp(+) = f1 fc (fc = 3.579545MHz)

#### fcp (-)

- 1) Lower the frequency of SG8 input signal so that the signal is synchronous with pin (19) output signal.
- 2) Raise the SG8 frequency.
- 3) Measure the SG8 frequency (f2) when the SG8 input signal is synchronous with the pin (9) output signal.
- 4) fcp(-) = f2 fc (fc = 3.579545MHz)

#### C-IN

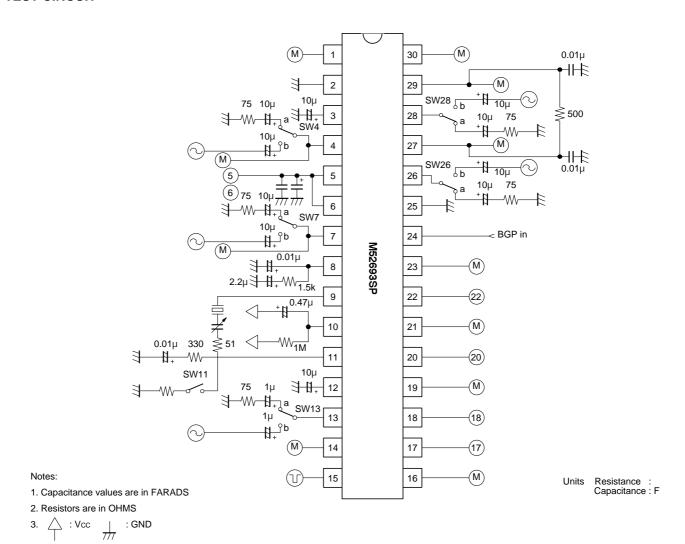
Make sure that the pin 3 input signal is synchronous with the pin 9 output signal when the input amplitude of pin 3 is 0.20VP-P. Then make sure that the pin 3 input signal is synchronous with the pin 9 output signal when the input amplitude is 0.01VP-P.

#### **BURST LOCK CLOCK GENERATOR**

#### **INPUT SIGNAL**

SG No.	Input signal	Remarks
SG1	NTSC system composite video signal (1VP-P)	
SG2	Sine wave Frequency: 3.58MHz Amplitude : 0.1VP-P	
SG2'	Sine wave Frequency: 3.58MHz Amplitude : 0.2V <sub>P-P</sub>	
SG2"	Sine wave Frequency: 3.58MHz Amplitude : 0.01V <sub>P-P</sub>	
SG3	Sine wave Frequency: 3.58MHz Amplitude : 0.3V <sub>P-P</sub>	
SG4	C-Sync + sine wave C-Sync Frequency: 15.734kHz Amplitude: 0.285VP-P Sine wave Frequency: 1/10MHz Amplitude: 0.715VP-P	
SG5	Sine wave Frequency: 3.58MHz Amplitude : 0.2V <sub>P-P</sub>	
SG6	Y signal Amplitude : 0.715VP-P	
SG7	Sine wave Frequency: 1/10MHz Amplitude : 0.2V <sub>P-P</sub>	
SG8	Sine wave Frequency: Variable Amplitude : 0.1V <sub>P-P</sub>	
PG1	C-Sync Frequency: 15.734kHz Amplitude : 0.3V <sub>P-P</sub> Vo <sub>L</sub> =2.75V	
PG1'	C-Sync Amplitude : 0.1VP-P 0.6VP-P	

#### **TEST CIRCUIT**



#### **TYPICAL CHARACTERISTICS**

#### THERMAL DERATING (MAXIMUM RATING)

