

MITSUBISHI <CONTROL / DRIVER IC>

M54972P/FP

Bi-CMOS 8-BIT SERIAL-INPUT LATCHED DRIVER

DESCRIPTION

The M54972 is a semiconductor integrated circuit consisting of 8 stages of CMOS shift registers and latches with serial inputs and serial or parallel outputs. It is based on Bi-CMOS process technology, and has 8 bipolar drivers at the parallel outputs.

FEATURES

- Serial input and serial or parallel output
- Serial output enables cascade connection
- Built-in latch for each stage
- Enable input provides output control
- Low supply current (standby current $I_{CC} \leq 10\mu A$)
- Serial I/O level is compatible with typical CMOS devices
- Driver features: High withstand voltage ($BV_{CEO} \geq 30V$)
Capable of large drive currents ($I_{O(max)}=300mA$)
Low output saturation voltage $V_{OL} < 0.6V$ at $I_o=300mA$
- Wide operating temperature range $T_a=-20 - +75^{\circ}C$

APPLICATION

Dot drivers for thermal print heads. Serial/parallel conversion. Drivers for relays and solenoids.

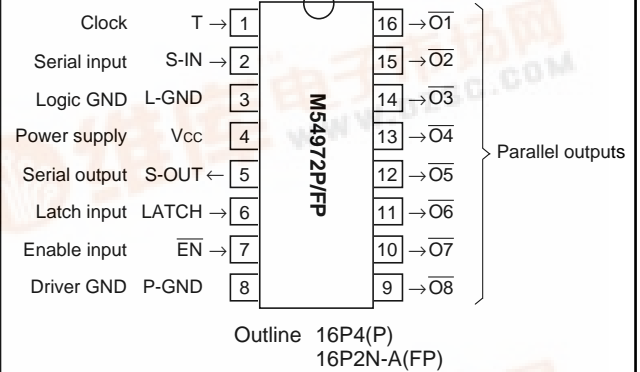
FUNCTION

The M54972 consists of 8 stages of D-type flip flops connected to 8 latches.

Data is input to serial input S-IN, and clock pulses are input to clock input T. When the clock changes from low to high, the input data enters the first shift register and data already in the shift registers is shifted sequentially.

The serial output S-OUT is used to connect multiple M54972 to expand the number of parallel outputs. S-OUT is connected to S-IN of the next stage.

PIN CONFIGURATION (TOP VIEW)



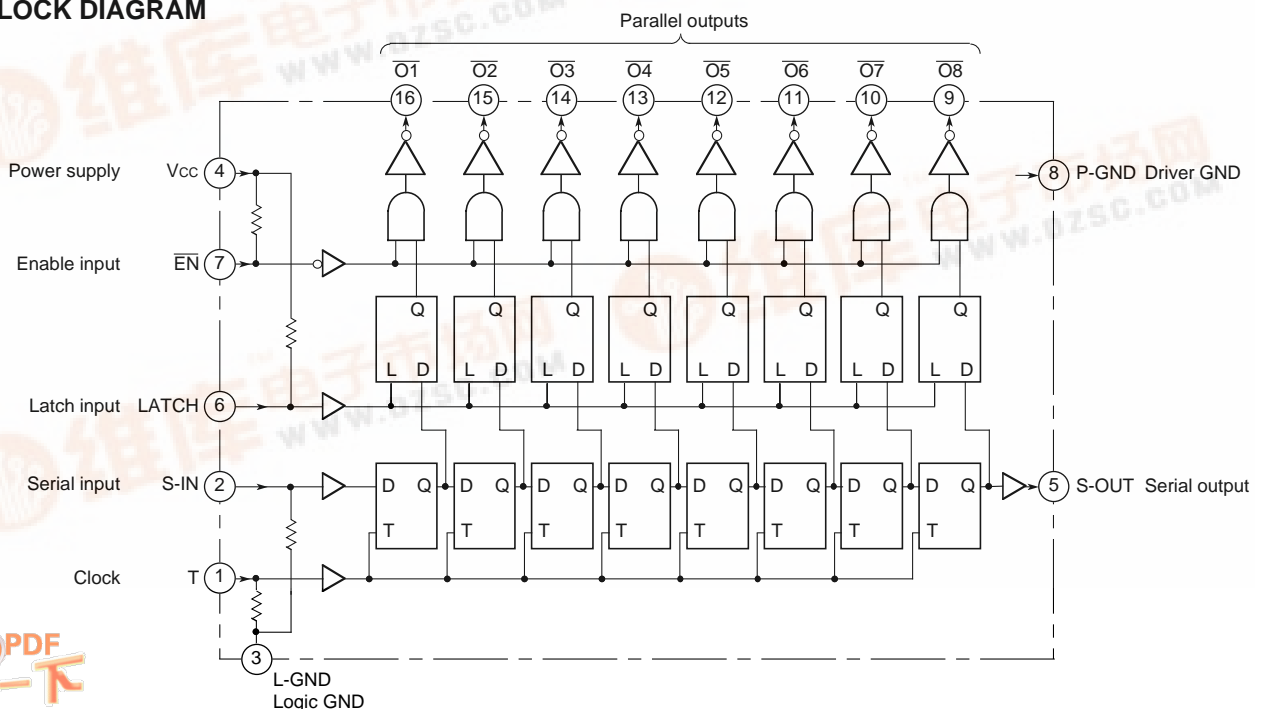
For parallel output. When the clock pulse changes from low to high, latch input (LATCH) is high and output enable input (\overline{EN}) is low the serial input data at S-IN appears at output $\overline{O1}$ and the other data already present is shifted sequentially to outputs $\overline{O2}$ through $\overline{O8}$.

The parallel outputs are inverted.

When the latch input is held low, the latch retains the stored data. When the \overline{EN} input is high, outputs $\overline{O1}$ through $\overline{O8}$ all turn off. As the internal logic is unstable when the power is turned on, the \overline{EN} input should be kept high (setting outputs $\overline{O1}$ through $\overline{O8}$ off) until input data is set and the internal logic is initialized.

L-GND is the GND of CMOS logic circuit and P-GND is the GND of output driver circuits $\overline{O1}$ through $\overline{O8}$ which employ bipolar transistors capable of large drive currents.

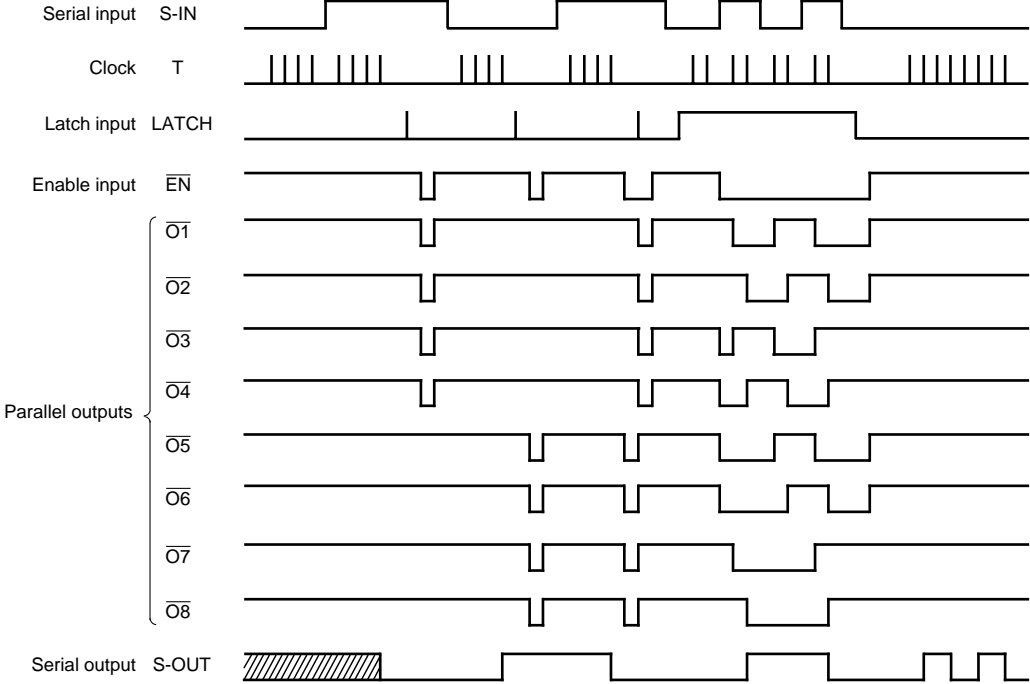
BLOCK DIAGRAM



M54972P/FP

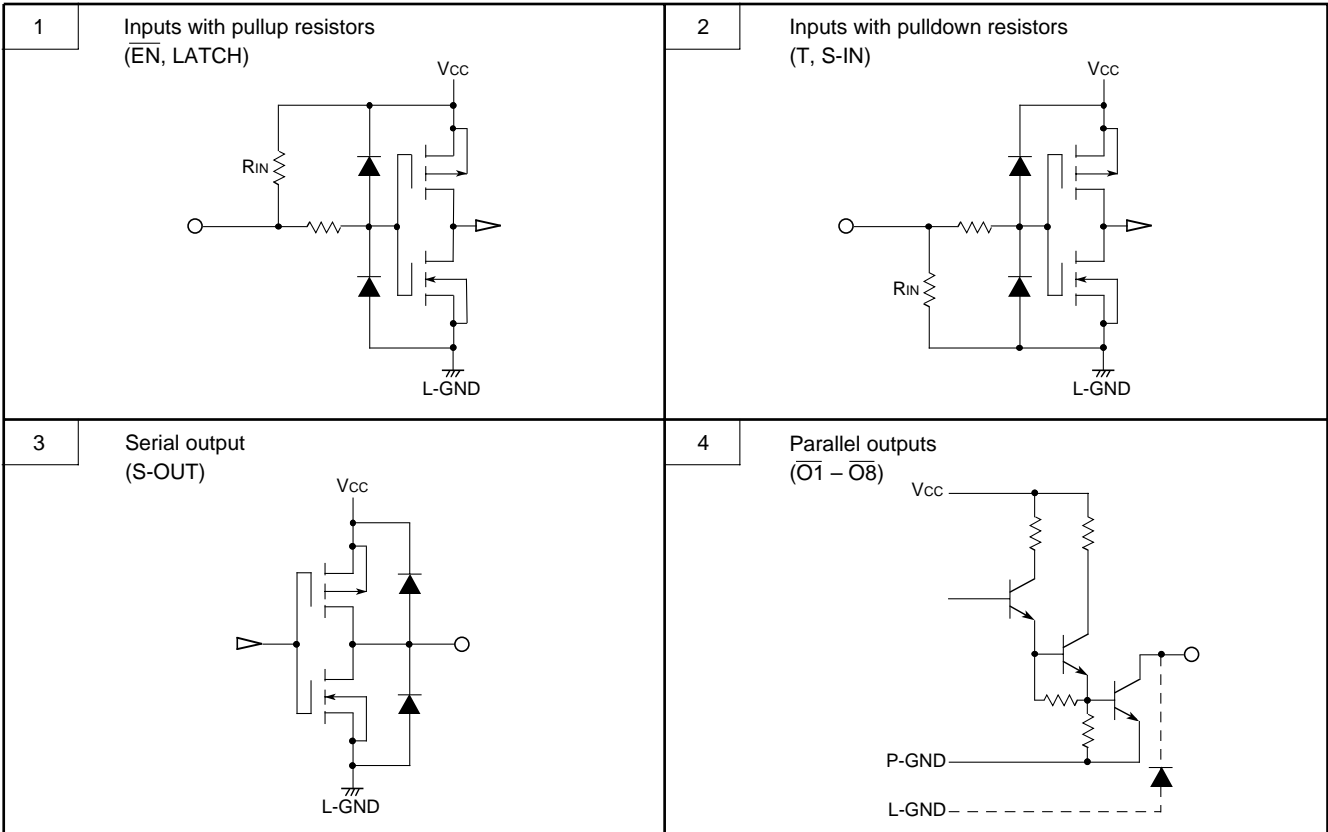
Bi-CMOS 8-BIT SERIAL-INPUT LATCHED DRIVER

TIMING CHART



*The shaded area shows the unstable state.

INPUT/OUTPUT CIRCUIT DIAGRAM



M54972P/FP

Bi-CMOS 8-BIT SERIAL-INPUT LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5 – +8	V
V _I	Input voltage		-0.5 – V _{CC} +0.5	V
V _O	Output voltage	S-OUT	-0.5 – V _{CC} +0.5	V
		$\overline{O1} - \overline{O8}$: OFF	-0.5 – +30	V
I _O	Output current	$\overline{O1} - \overline{O8}$: ON	300	mA
P _d	Power dissipation	T _a =25°C	M54972P 1.25 M54972FP 0.8	W
T _{opr}	Operating temperature		-20 – 75	°C
T _{stg}	Storage temperature		-55 – 125	°C

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage		4	5	6	V
V _O	Applied output voltage	$\overline{O1} - \overline{O8}$: OFF			30	V
I _O	Output current (per circuit)	$\overline{O1} - \overline{O8}$: ON, Duty cycle < 35%			300	mA
		$\overline{O1} - \overline{O8}$: ON, Duty cycle < 70%	M54972P		200	
		$\overline{O1} - \overline{O8}$: ON, Duty cycle < 15%	M54972FP		200	

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{IH}	High-level input voltage	T _a =-20 – 75°C, V _{CC} =4 – 6V	0.7V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage		0		0.3V _{CC}	V
I _{IH}	High-level input current	T, S-IN			100	μA
I _{IL}	Low-level input current	\overline{EN} , LATCH			-100	μA
R _{IN}	Input resistance		50			kΩ
V _{OH}	High-level output voltage	S-OUT	4.9			V
V _{OL}	Low-level output voltage	S-OUT			0.1	V
I _{OH}	High-level output current	S-OUT	-100			μA
I _{OL}	Low-level output current	S-OUT	400			μA
V _{OL1}	Low-level output voltage	$\overline{O1} - \overline{O8}$			0.5	V
V _{OL2}			I _{OL} =200mA			
V _{OL3}			I _{OL} =300mA			0.6
I _{OLK}	Output leak current	$\overline{O1} - \overline{O8}$			50	μA
I _{CC1}	Supply current				10	μA
I _{CC2}		One driver output is ON.			7.5	mA

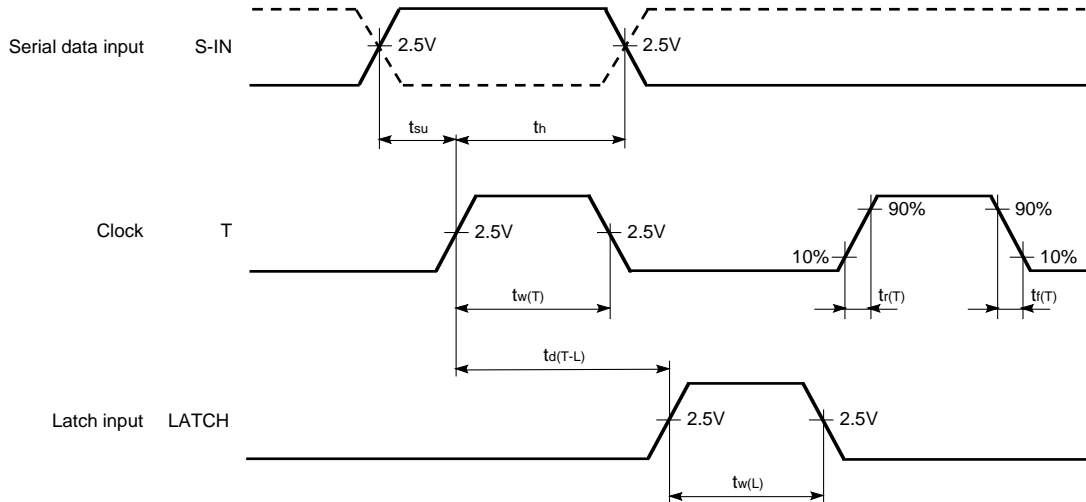
TIMING REQUIREMENTS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
f _(T)	Clock frequency	Input duty cycle: 40 – 60%			2	MHz
t _{w(T)}	Clock pulse width		200			ns
t _{w(L)}	Latch pulse width		200			ns
t _{su}	Data setup time		100			ns
t _h	Data hold time		100			ns
t _{d(T-L)}	Clock-latch time		400			ns
t _{r(T)}	Clock pulse rise time				500	ns
t _{f(T)}	Clock pulse fall time				500	ns

M54972P/FP

Bi-CMOS 8-BIT SERIAL-INPUT LATCHED DRIVER

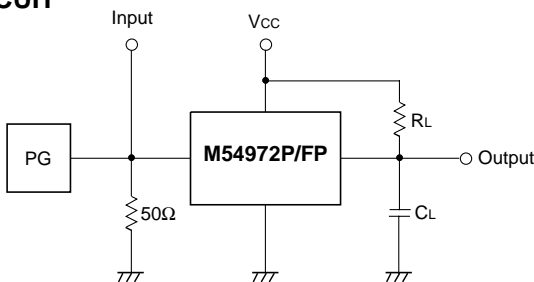
TIMING CHART



SWITCHING CHARACTERISTICS (Ta=25°C, VCC=5V, unless otherwise noted)

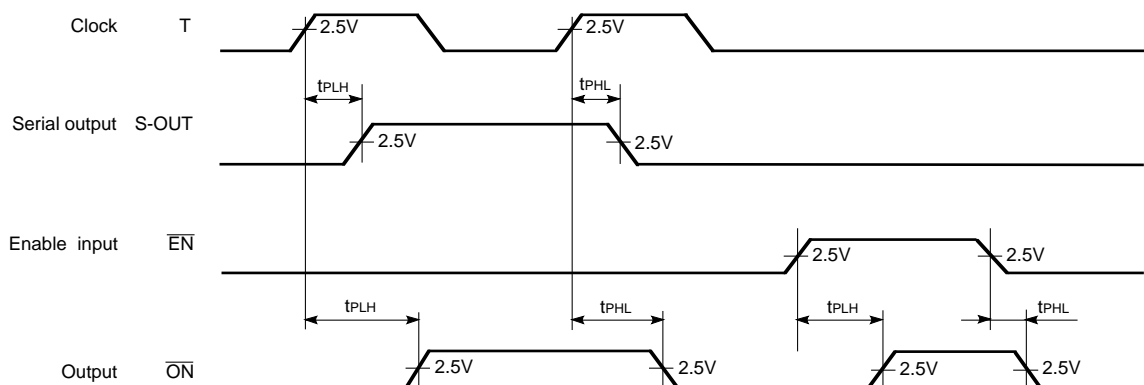
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{PLH}	Low-to-high-level output propagation time From input T to output S-OUT	V _{IH} =5V V _{IL} =0V R _L (S-OUT)=∞ R _L (ON)=100Ω (N=1-8) C _L =15pF			0.3	μs
t _{PHL}	High-to-low-level output propagation time From input T to output S-OUT				0.3	μs
t _{PLH}	Low-to-high-level output propagation time From input T to output ON				10	μs
t _{PHL}	High-to-low-level output propagation time From input T to output ON				5	μs
t _{PLH}	Low-to-high-level output propagation time From input EN to output ON				10	μs
t _{PHL}	High-to-low-level output propagation time From input EN to output ON				5	μs

TEST CIRCUIT



- The input waveform:
t_r ≤ 20ns, t_f ≤ 20ns
- The capacitance C_L includes the stray wiring capacitance and probe input capacitance.

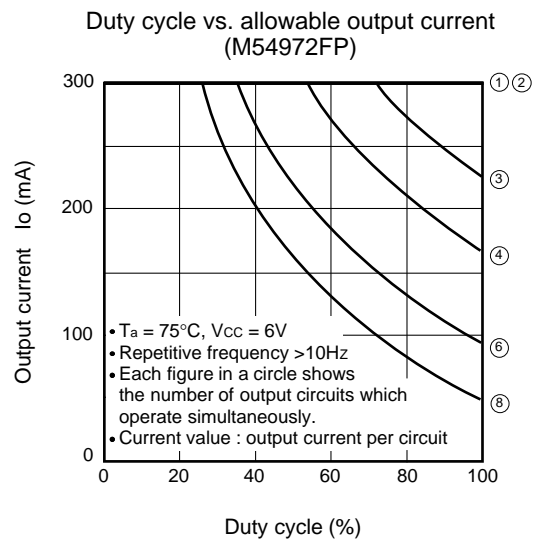
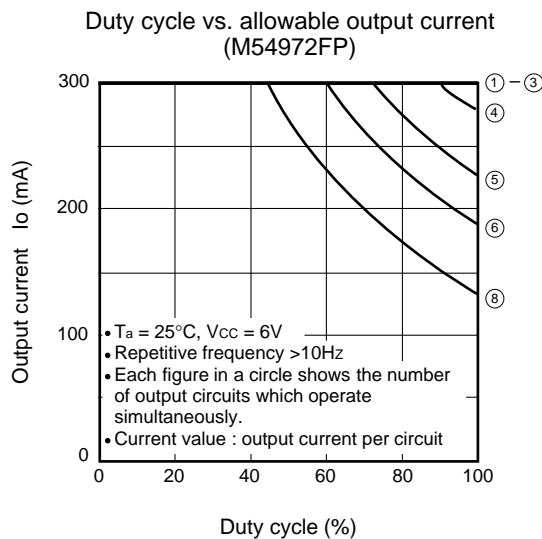
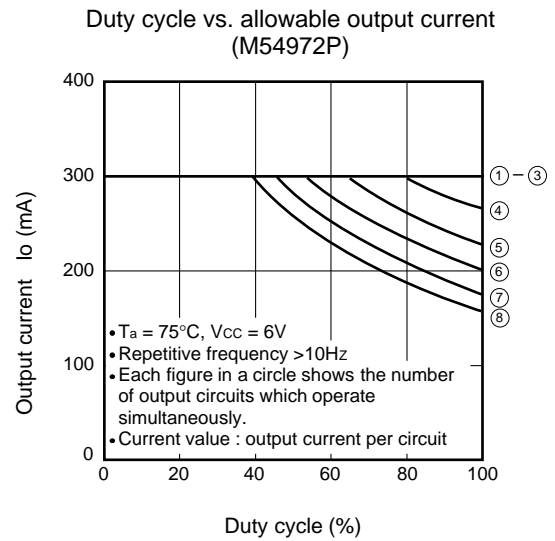
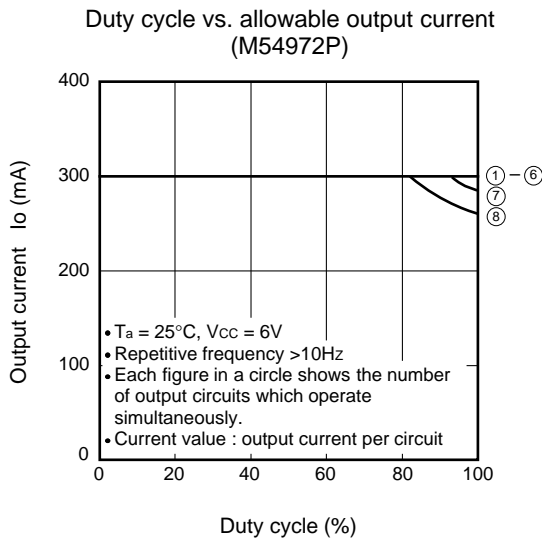
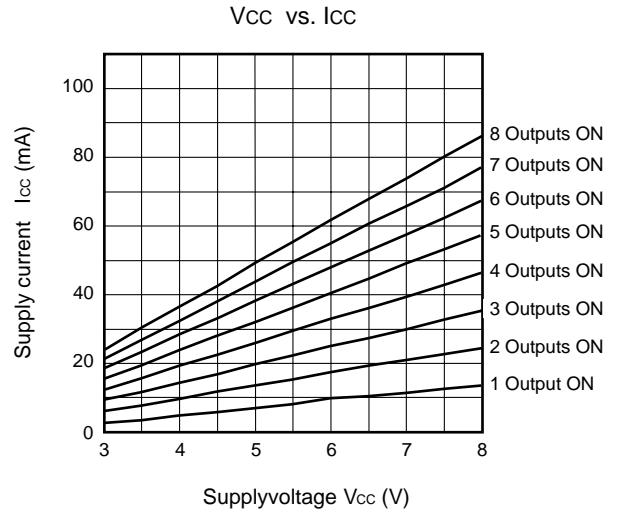
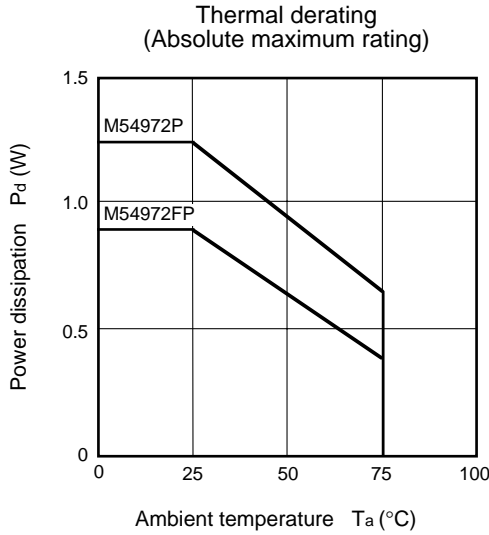
TIMING CHART



M54972P/FP

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TYPICAL CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)



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Driver output V_{OL} vs. I_{OL} (common)

