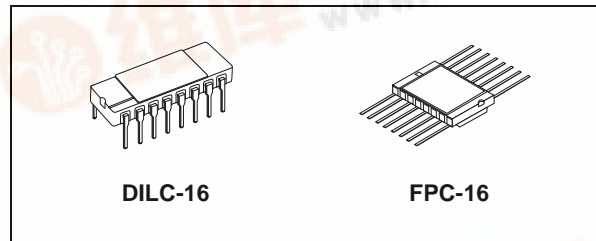




M54HC165

RAD-HARD 8 BIT PISO SHIFT REGISTER

- HIGH SPEED:
 $t_{PD} = 15\text{ns}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH
 54 SERIES 165
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON
 REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS
 IRRADIATION
- DEVICE FULLY COMPLIANT WITH
 SCC-9306-042



ORDER CODES

PACKAGE	FM	EM
DILC	M54HC165D	M54HC165D1
FPC	M54HC165K	M54HC165K1

DESCRIPTION

The M54HC165 is an high speed CMOS 8 BIT PISO SHIFT REGISTER fabricated with silicon gate C²MOS technology.

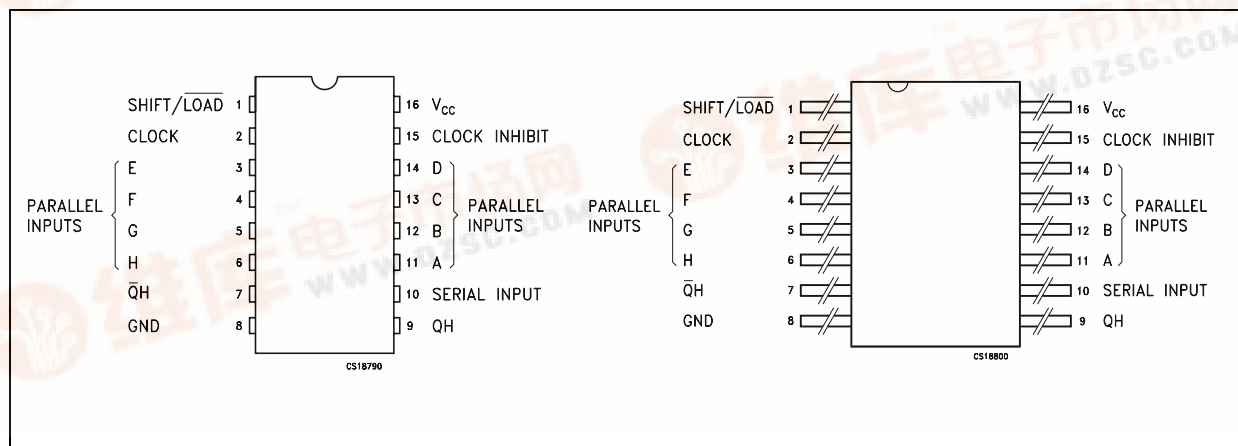
This device contains eight clocked master slave RS flip-flops connected as a shift register, with auxiliary gating to provide over-riding asynchronous parallel entry. Parallel data enters

when the shift/load input is low. The parallel data can change while shift/load is low, provided that the recommended set-up and hold times are observed. For clocked operation, shift/load must be high. The two clock input perform identically; one can be used as a clock inhibit by applying a high signal; to permit this operation clocking is accomplished through a 2 input nor gate.

To avoid double clocking, however, the inhibit signal should only go high while the clock is high. Otherwise the rising inhibit signal will cause the same response as rising clock edge.

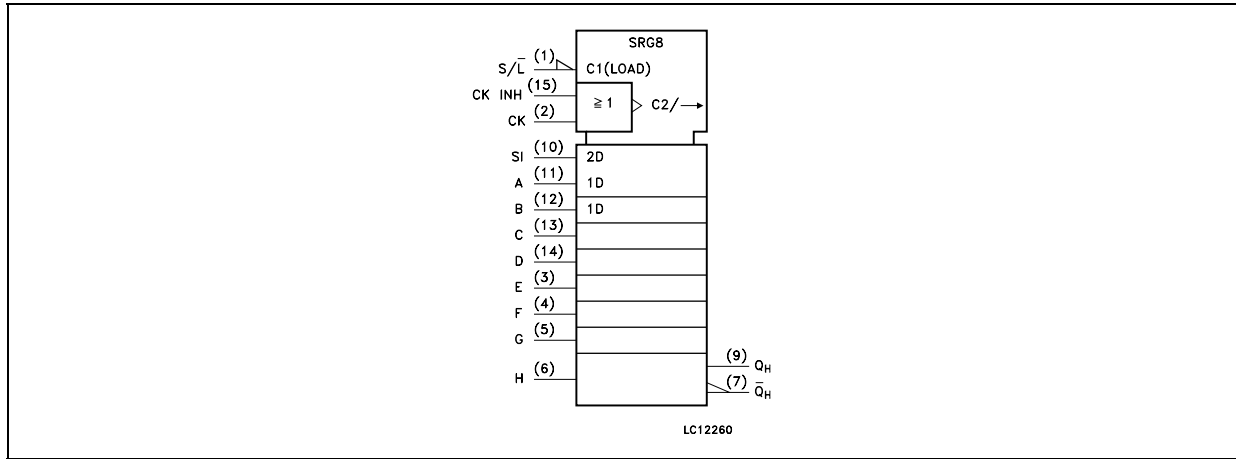
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

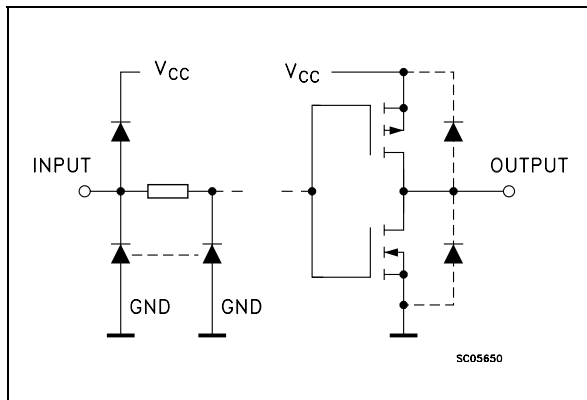


M54HC165

IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

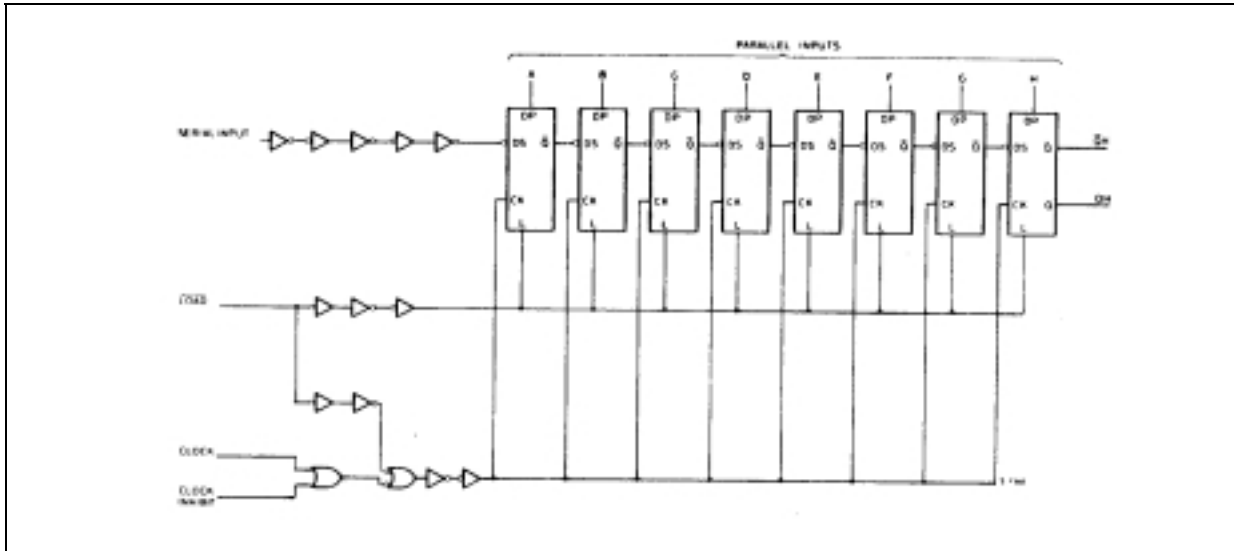
PIN N°	SYMBOL	NAME AND FUNCTION
1	SHIFT/LOAD	Data Inputs
2	QH	Complementary Output
7	QH	Serial Output
9	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
10	SI	Serial Data Inputs
11, 12, 13, 14, 3, 4, 5, 6	A to H	Parallel Data Inputs
15	CLOCK INH	Clock Inhibit
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

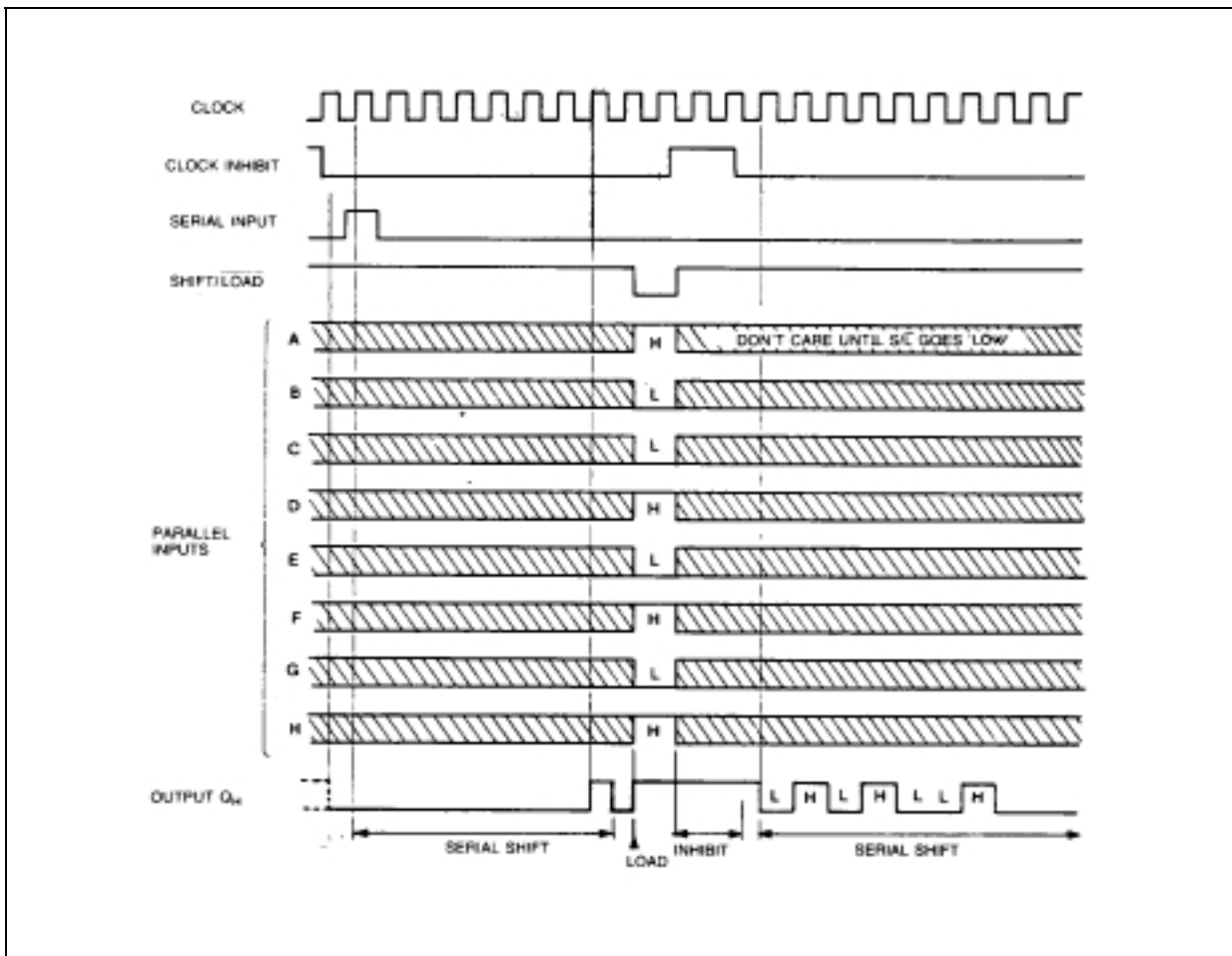
INPUTS					INTERNAL OUTPUTS		OUTPUTS
SHIFT/LOAD	CLOCK INH	CLOCK	SI	A.....H	QA	QB	QH
L	X	X	X	a.....h	a	b	h
H	L	⎓	H	X	H	QAn	QGn
H	L	⎓	L	X	L	QAn	QGn
H	⎓	L	H	X	H	QAn	QGn
H	⎓	L	L	X	L	QAn	QGn
H	X	H	X	X	NO CHANGE		
H	H	X	X	X	NO CHANGE		

a.....h : The level of steady input voltage at inputs a through respectively
 QAn - QGn : The level of QA - QG, respectively, before the most-recent transition of the clock

LOGIC DIAGRAM



TIMING CHART



M54HC165

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	°C	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1	
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA

M54HC165

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

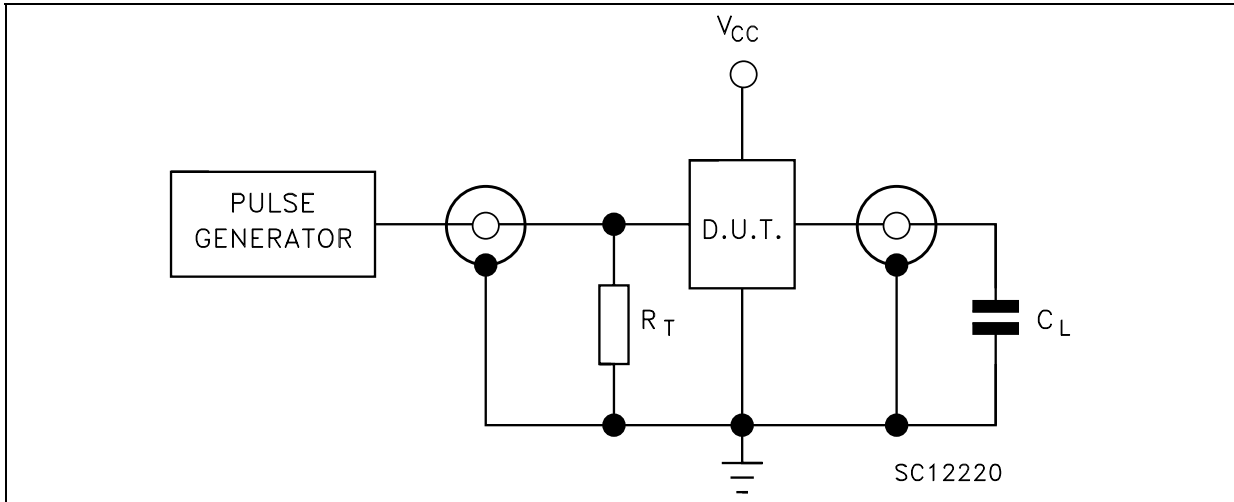
Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QH, \overline{QH})	2.0			55	150		190		225	ns
		4.5			18	30		38		45	
		6.0			15	26		33		38	
t_{PLH} t_{PHL}	Propagation Delay Time (SHIFT/LOAD - QH, \overline{QH})	2.0			65	165		205	250		ns
		4.5			21	33		41		50	
		6.0			18	28		35		43	
t_{PLH} t_{PHL}	Propagation Delay Time (H - QH, \overline{QH})	2.0			52	135		170		205	ns
		4.5			17	27		34		41	
		6.0			14	23		29		35	
f_{MAX}	Maximum Clock Frequency	2.0		7.4	15		6.0		4.8		MHz
		4.5		37	60		30		24		
		6.0		44	71		35		28		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (SHIFT/LOAD)	2.0			32	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_s	Minimum Set-up Time (PI - SHIFT/LOAD) (SI - CLOCK) (SHIFT/LOAD - CK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t_h	Minimum Hold Time (PI - SHIFT/LOAD) (SI - CLOCK) (SHIFT/LOAD - CK)	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time (CLOCK - CK INH)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			55						pF

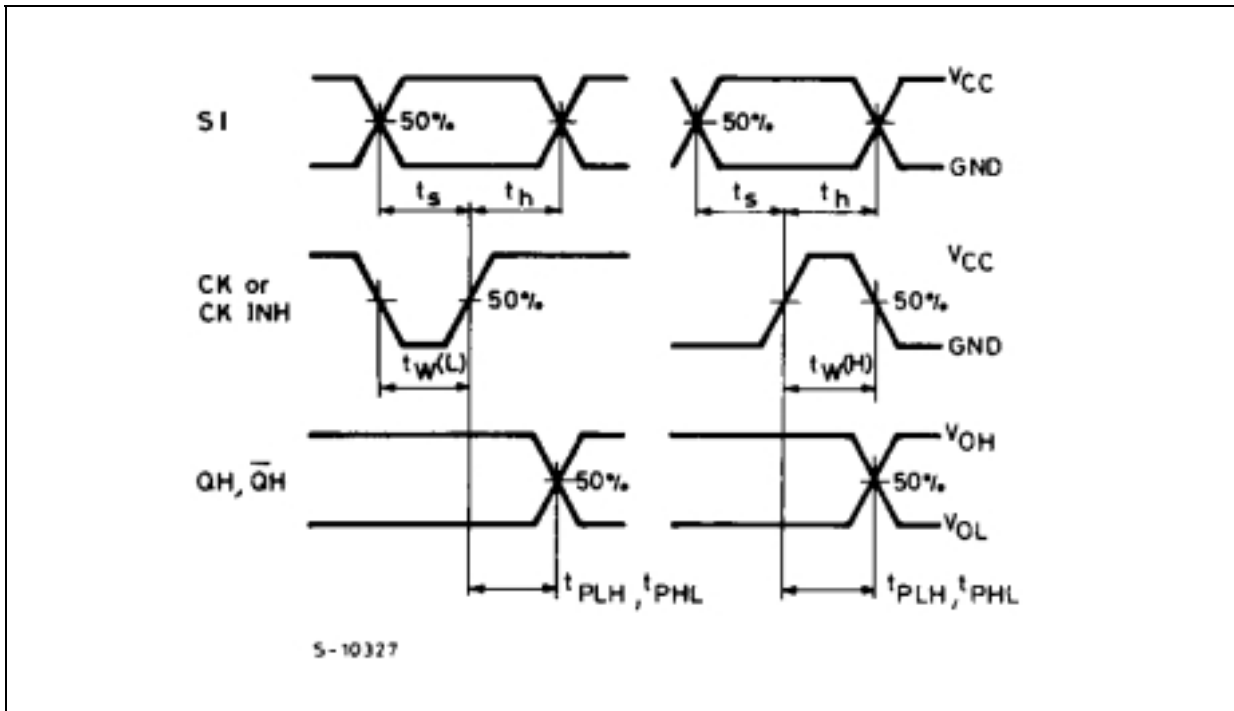
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

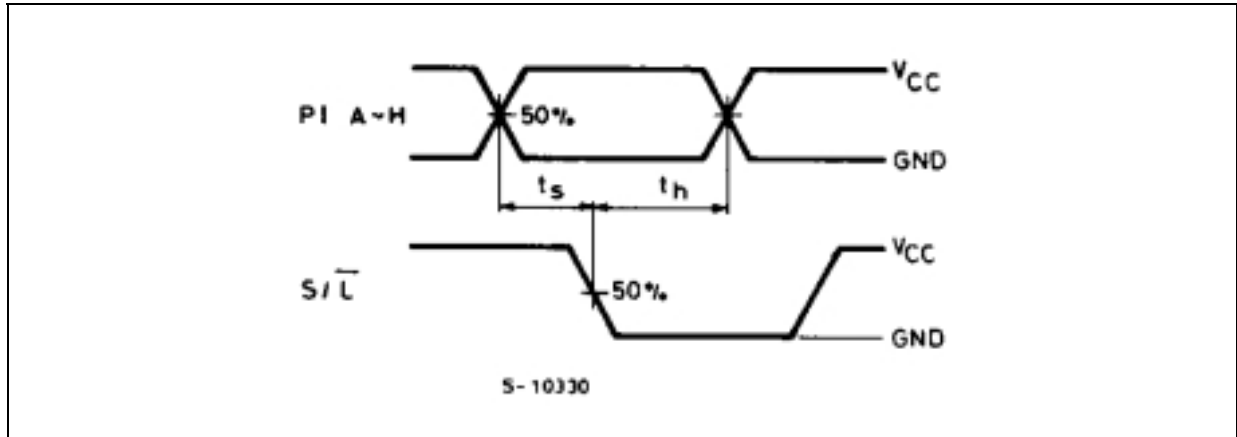
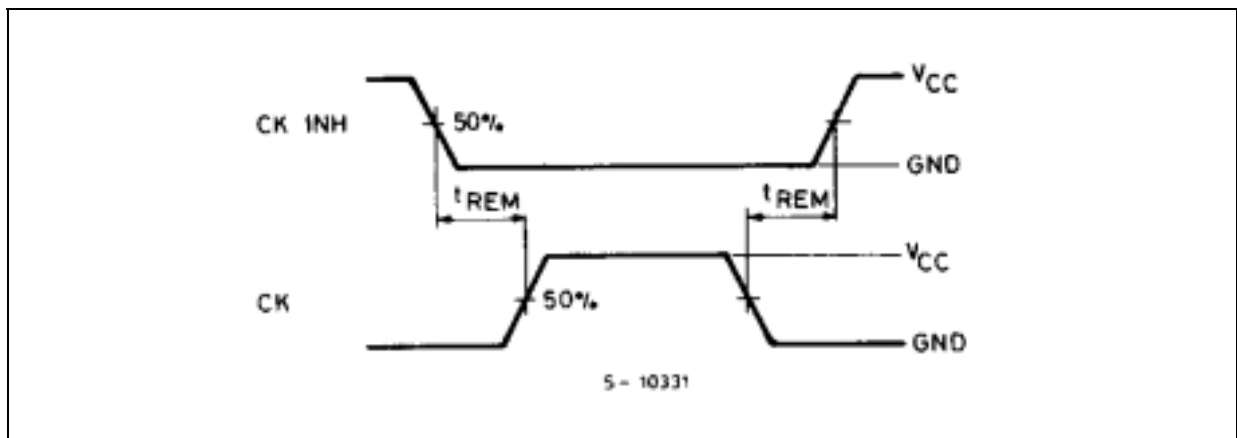
TEST CIRCUIT



$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

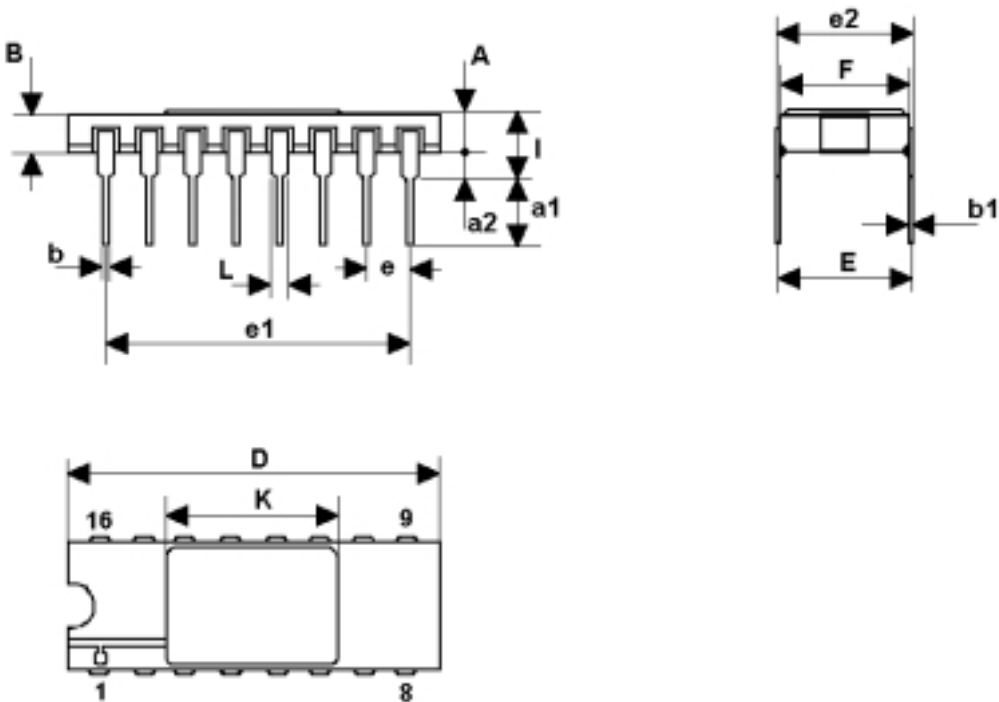
WAVEFORM 1: SERIAL MODE PROPAGATION DELAY ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 4: SETUP AND HOLD TIME (PI TO S/L) ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 5: MINIMUM REMOVAL TIME (CK INH TO CK)** ($f=1\text{MHz}$; 50% duty cycle)

DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
e	7.36	7.62	7.87	0.290	0.300	0.310
e1		2.54			0.100	
e2	17.65	17.78	17.90	0.695	0.700	0.705
e3	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



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