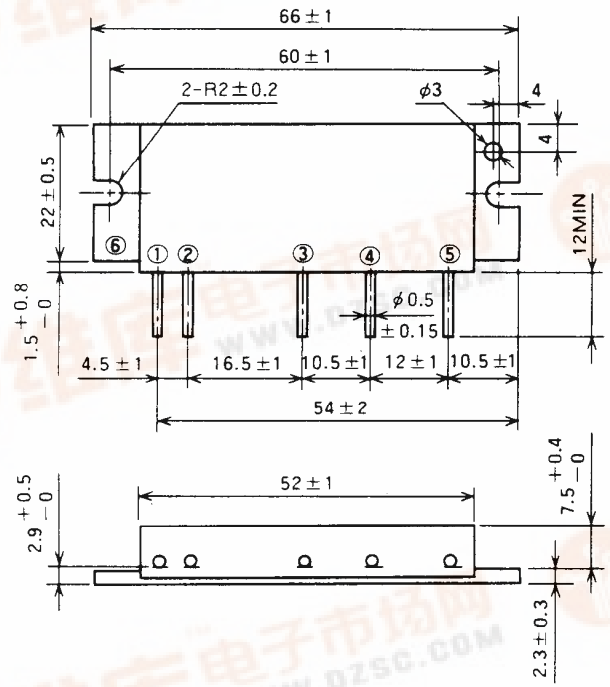
M57704M

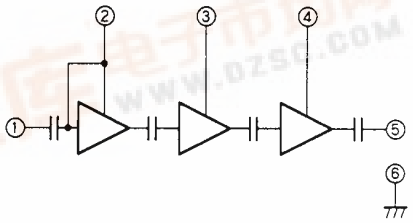
430-450MHz, 12.5V, 13W, FM MOBILE RADIO

OUTLINE DRAWING Dimensions in mm



H3

BLOCK DIAGRAM



PIN :
①Pin : RF INPUT
②VCC1 : 1st. DC SUPPLY
③VCC2 : 2nd. DC SUPPLY
④VCC3 : 3rd. DC SUPPLY
⑤Po : RF OUTPUT
⑥GND : FIN

ABSOLUTE MAXIMUM RATINGS (Tc = 25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		17	V
I_{CC}	Total current		5	A
$P_{in(max)}$	Input power	$Z_G = Z_L = 50\ \Omega$	0.4	W
$P_{O(max)}$	Output power	$Z_G = Z_L = 50\ \Omega$	20	W
$T_{C(OP)}$	Operation case temperature		− 30 to 110	℃
T_{stg}	Storage temperature		− 40 to 110	℃

Note. Above parameters are guaranteed independently.

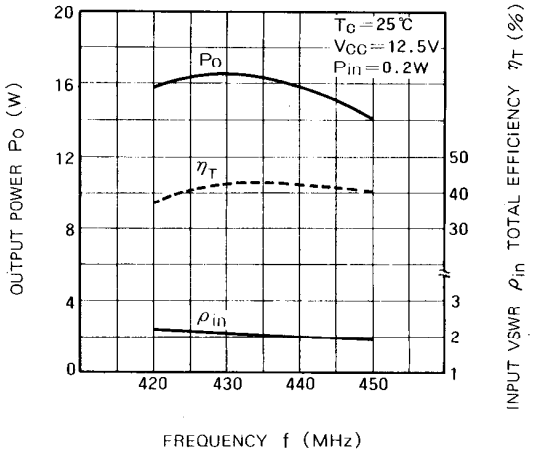
ELECTRICAL CHARACTERISTICS (Tc = 25℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	P_{in} = 0.2W V_{CC} = 12.5V $Z_G = Z_L = 50\ \Omega$	430	450	MHz
P_O	Output power		13		W
η_T	Total efficiency		35		%
2fo	2nd. harmonic			− 30	dBc
ρ_{in}	Input VSWR			2.8	−
−	Load VSWR tolerance	V_{CC} = 15.2V, P_O = 14W (P_{in} : controlled) Load VSWR=20:1 (All phase), 2sec. $Z_G = 50\ \Omega$	No degradation or destroy		−

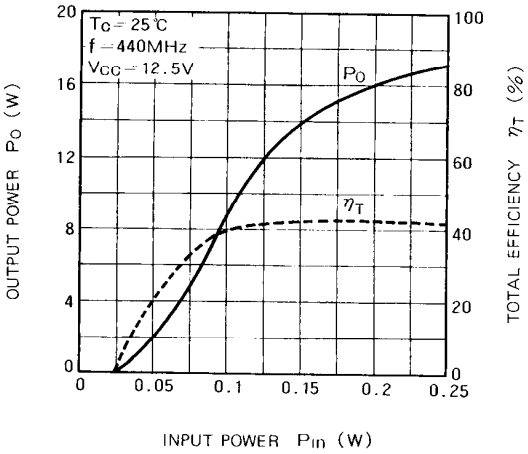
Note. Above parameters, ratings, limits and conditions are subject to change.

TYPICAL PERFORMANCE DATA

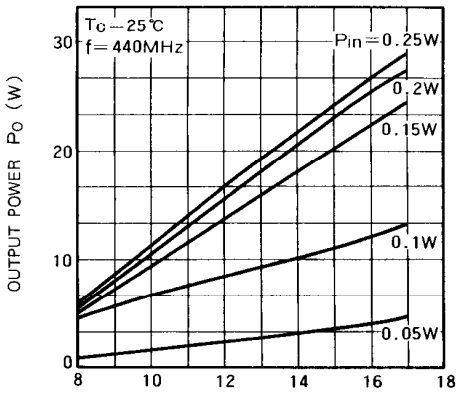
OUTPUT POWER TOTAL EFFICIENCY INPUT VSWR VS. FREQUENCY



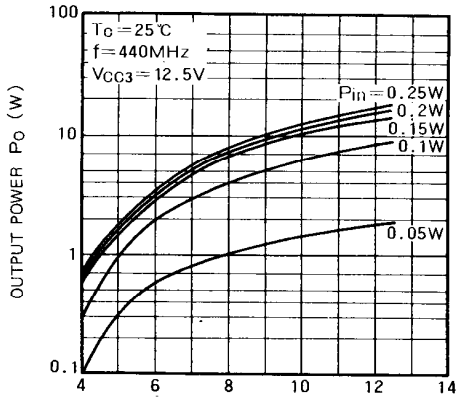
OUTPUT POWER TOTAL EFFICIENCY VS. INPUT POWER



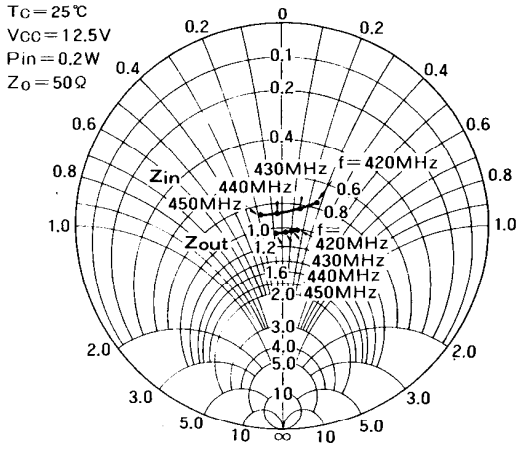
OUTPUT POWER VS. DC SUPPLY VOLTAGE



OUTPUT POWER VS. 1st AND 2nd VOLTAGE



INPUT IMPEDANCE OUTPUT IMPEDANCE



DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to following consideration when designing heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistance between junction and package of incorporated transistors.
   a) First stage transistor
      $R_{th(j-c)1}$ = 15°C/W (Typ.)
   b) Second stage transistor
      $R_{th(j-c)2}$ = 6°C/W (Typ.)
   c) Final stage transistor
      $R_{th(j-c)3}$ = 2.5°C/W (Typ.)

(2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.
  P_O = 13W, V_{CC} = 12.5V, P_{in} = 0.2W, η_T = 35% (minimum rating), P_{O1} (Note 1) = 1.5W, P_{O2} (2) = 6W, I_T = 3.0A (I_{T1} (3) = 0.25A, I_{T2} (4) = 0.75A, I_{T3} (5) = 2.0A)
  Note 1: Output power of the first stage transistor
  Note 2: Output power of the second stage transistor
  Note 3: Circuit current of the first stage transistor
  Note 4: Circuit current of the second stage transistor
  Note 5: Circuit current of the final stage transistor
- Junction temperature of the first stage transistor
  $T_{j1} = (V_{CC} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C$ (6)
  $= (12.5 \times 0.25 - 1.5 + 0.2) \times 15 + T_C$
  $= 27 + T_C$ (°C)
  Note 6: Package temperature of device
- Junction temperature of the second stage transistor
  $T_{j2} = (V_{CC} \times I_{T2} - P_{O2} + P_{O1} \times R_{th(j-c)2} + T_C$
  $= (12.5 \times 0.75 - 6 + 1.5) \times 6 + T_C$
  $= 29 + T_C$ (°C)
- Junction temperature of the final stage transistor
  $T_{j3} = (V_{CC} \times I_{T3} - P_O + P_{O2}) \times R_{th(j-3)} + T_C$
  $= (12.5 \times 2.0 - 13 + 6) \times 2.5 + T_C$
  $= 45 + T_C$ (°C)

2. Heat sink design

In thermal design of heat sink, try to keep to package temperature at the upper limit of the operating ambient temperature (normally T_a = 60°C) and at the output power of 13W below 90°C.

The thermal resistance $R_{th(c-a)}$ (7) of the heat sink to realize this:

$$R_{th(c-a)} = \frac{T_c - T_a}{(P_o/\eta_T) - P_o + P_{in}} = \frac{90 - 60}{(13/0.35) - 13 + 0.2}$$
$$= 1.2\ (°C/W)$$

Note 7: Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

T_{j1} = 117°C, T_{j2} = 119°C, T_{j3} = 135°C at T_{j3} = 135°C at Ta = 60°C, T_C = 90°C.

In the annual average of ambinet temperature is 30°C,

T_{j1} = 87°C, T_{j2} = 89°C, T_{j3} = 105°C.

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C, application under fully derated condition is ensured.