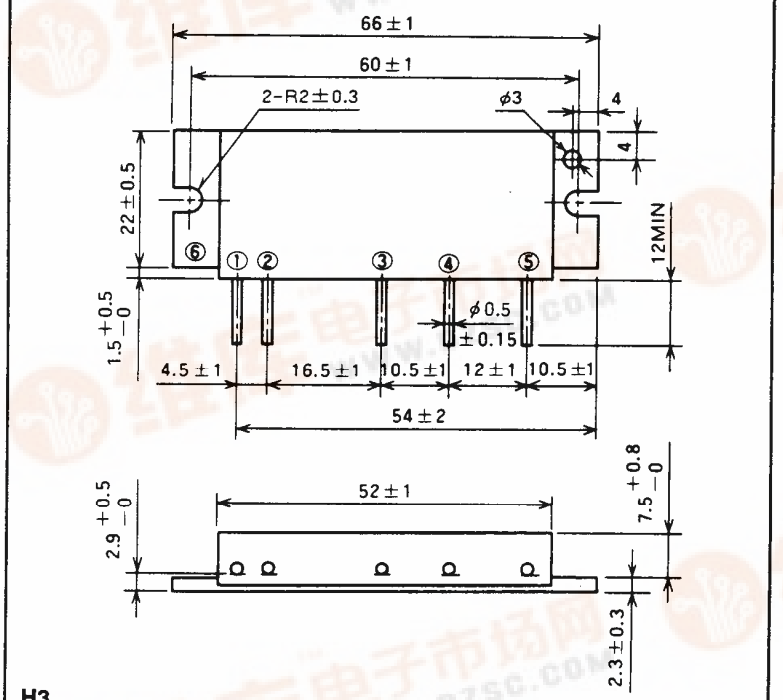
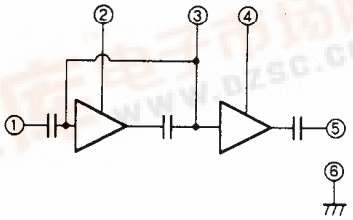
M57713

144-148MHz, 12.5V, 17W, SSB MOBILE RADIO

OUTLINE DRAWING Dimensions in mm



BLOCK DIAGRAM



PIN :
①Pin : RF INPUT
②VCC1 : 1st. DC SUPPLY
③VBB : BASE BIAS SUPPLY
④VCC2 : 2nd. DC SUPPLY
⑤Po : RF OUTPUT
⑥GND : FIN

ABSOLUTE MAXIMUM RATINGS (Tc = 25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		17	V
VBB	Base bias		10	V
Icc	Total current		6	A
Tc(OP)	Operation case temperature		− 30 to 110	℃
Tstg	Storage temperature		− 40 to 110	℃

Note. Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS (Tc = 25℃ unless otherwise noted)

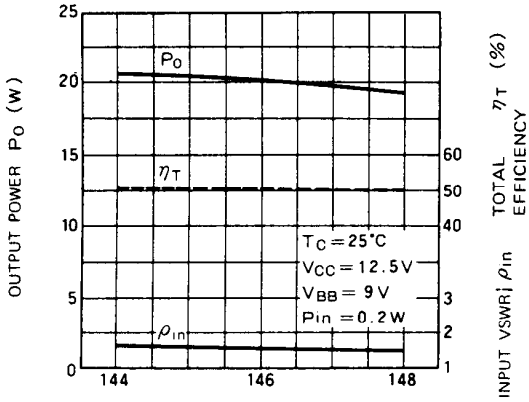
Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	Pin = 0.2W Vcc = 12.5V VBB = 9V ZG = ZL = 50 Ω	144	148	MHz
Po	Output power		17		W
ηT	Total efficiency		40		%
2fo	2nd. harmonic			− 25	dBc
3fo	3rd. harmonic			− 30	dBc
ρin	Input VSWR			2.2	−
−	Load VSWR tolerance	Vcc = 15.2V, VBB = 9V Po = 14W (Pin : controlled) Load VSWR=20:1(All phase) ZG = 50 Ω	No degradation or destroy		−

Note. Above parameters, ratings, limits and conditions are subject to change.

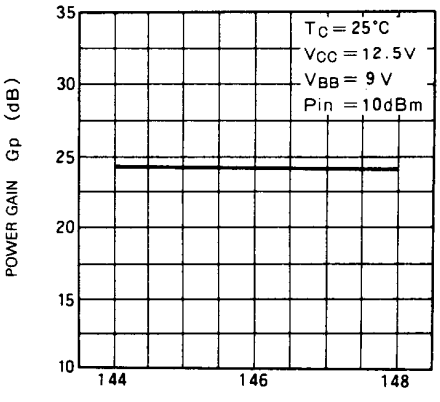
MITSUBISHI ELECTRIC

TYPICAL PERFORMANCE DATA

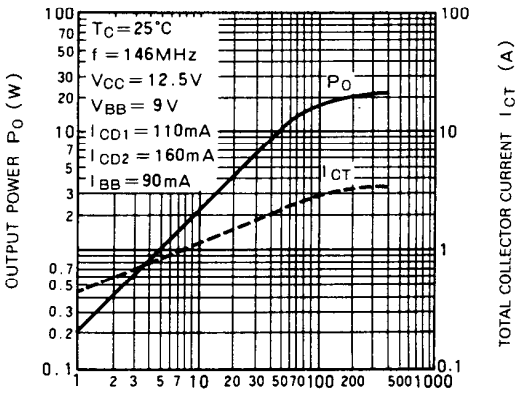
OUTPUT POWER, TOTAL EFFICIENCY, INPUT VSWR VS. FREQUENCY



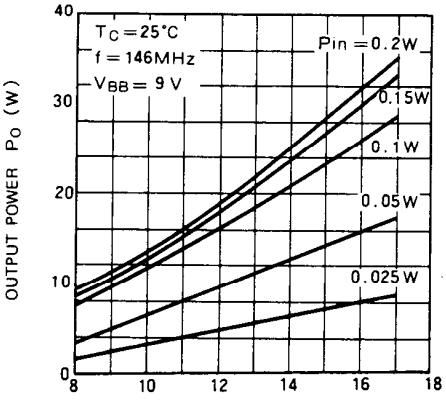
POWER GAIN VS. FREQUENCY



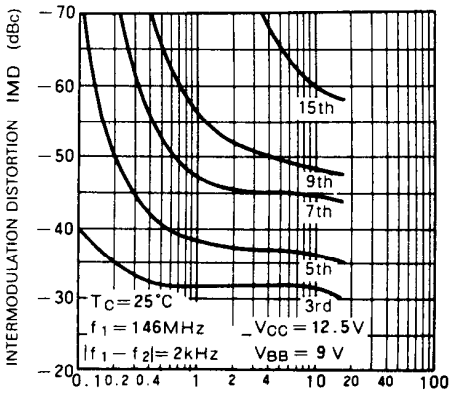
OUTPUT POWER, TOTAL COLLECTOR CURRENT VS. INPUT POWER



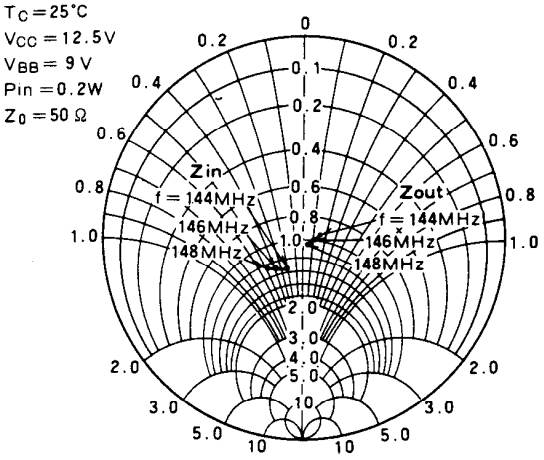
OUTPUT POWER VS. DC SUPPLY VOLTAGE



INTERMODULATION DISTORTION VS. OUTPUT POWER



INPUT IMPEDANCE, OUTPUT IMPEDANCE VS. FREQUENCY



DESIGN CONSIDERATION OF HEAT RADIATION.

Please refer to following consideration when designing heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistance between junction and package of incorporated transistors.
   a) First stage transistor
      $R_{th(j-c)1}$ = 10°C/W (Typ.)
   b) Final stage transistor
      $R_{th(j-c)2}$ = 2°C/W (Typ.)

(2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.
  P_O = 14W, V_{CC} = 12.5V, P_{in} = 0.07W, η_T = 40% (minimum rating), P_{O1} (Note 1) = 2.5W, I_T = 2.8A (I_{T1} (2) = 0.5A, I_{T2} (3) = 2.3A)
  Note 1: Output power of the first stage transistor
  Note 2: Circuit current of the first stage transistor
  Note 3: Circuit current of the final stage transistor
- Junction temperature of the first stage transistor
  $T_{j1} = (V_{CC} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C$ (4)
  $= (12.5 \times 0.5 - 2.5 + 0.07) \times 10 + T_C$
  $= 39 + T_C$ (°C)

  Note 4: Package temperature of device
- Junction temperature of the final stage transistor
  $T_{j2} = (V_{CC} \times I_{T2} - P_O + P_{O1}) \times R_{th(j-c)2} + T_C$
  $= (12.5 \times 2.3 - 14 + 2.5) \times 2 + T_C$
  $= 35 + T_C$ (°C)

2. Heat sink design

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambinet temperature (normally T_a = 60°C) and at the output power of 14W below 90°C.

The thermal resistance $R_{th(c-a)}$ (5) of the heat sink to realize this:

$$R_{th(c-a)} = \frac{T_C - T_a}{(P_O/\eta_T) - P_O + P_{in}} = \frac{90 - 60}{(14/0.4) - 14 + 0.07}$$

$$= 1.42\ (°C/W)$$

Note 5: Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

T_{j1} = 129°C, T_{j2} = 125°C at T_a = 60°C, T_C = 90°C.

In the annual average of ambient temperature is 30°C,

T_{j1} = 99°C, T_{j2} = 95°C

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C, application under fully derated condition is ensured.