M61527FP

6ch ELECTRONIC VOLUME WITH 10 INPUT SELECTOR

REJ03F0036-0100Z
Rev.1.0
Sep.19.2003

Feature

FUNCTION	FEATURE
Electric Volume	6 channel independent with High Voltage Transistor. (0 to -99dB/ 1dBstep, -∞dB)
Input Selector	Front L/R channel 10 Input Selector.
Multi Channel Input	All channel 2 Input Selector.
REC Output	4 Lines REC Output (Both L and R channels)
Input ATT	Input ATT (for ADC:0/-6/-12/-18dB)
Input Gain Control	Input Gain Control (0/+6/+12/+18dB)
Output Gain Control	Output Gain Control (0/+6/+12/+18dB)
Balance Out	Built-in Balance out (for ADC)

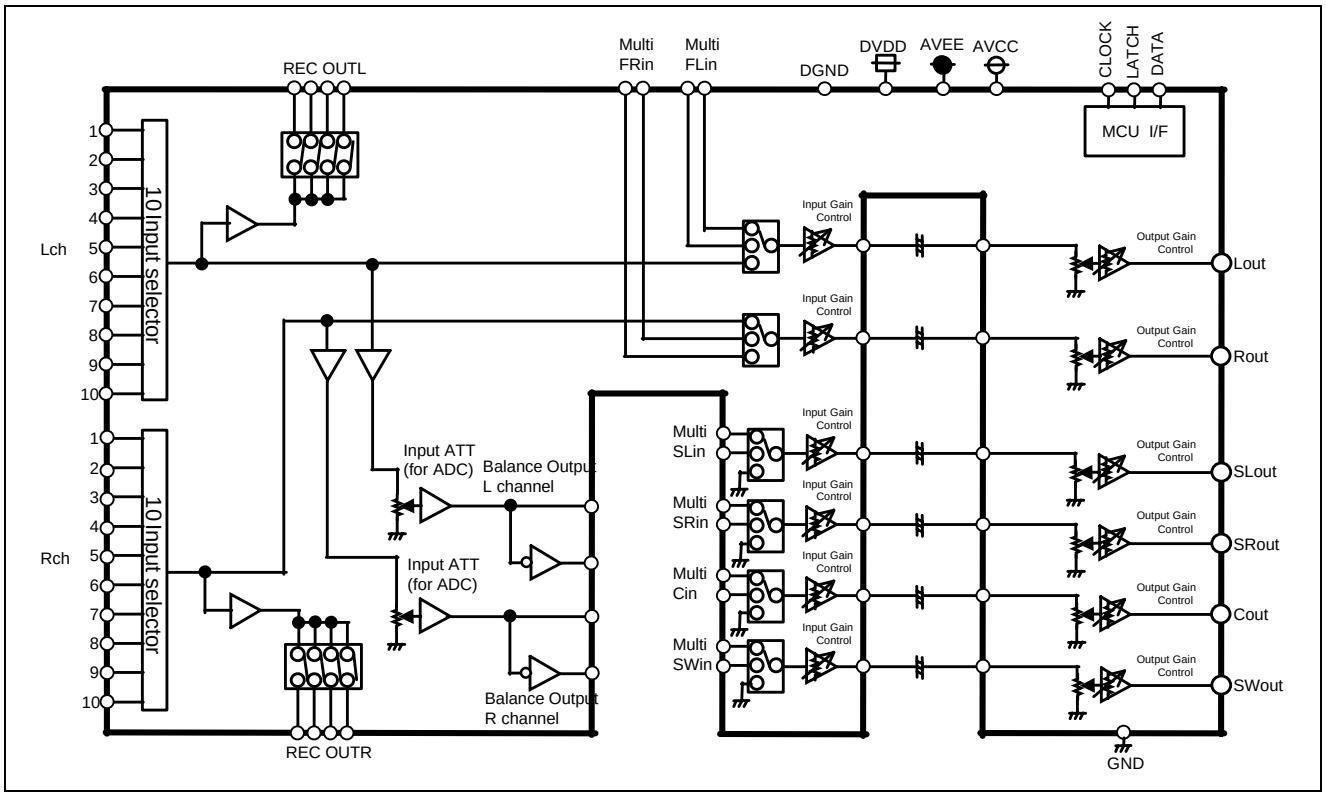
Recommended Operating Condition

Rated Supply Voltage ……AVCC=7.0V(typ), AVEE=-7.0V(typ), DVDD=3.3V(typ)

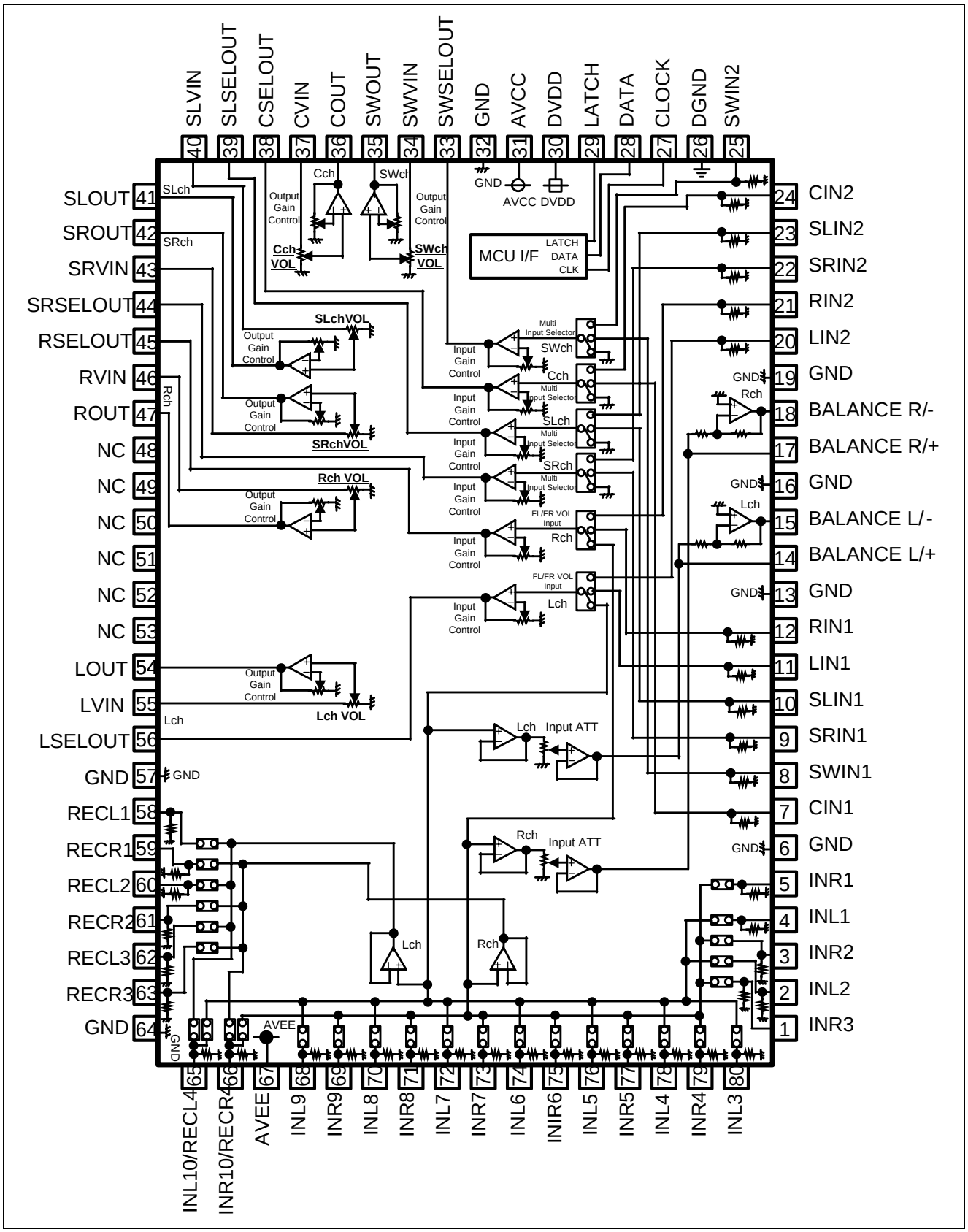
Application

Receiver, AV Amp, Mini Stereo etc.

System Block Diagram



Block Diagram and Pin Configuration (Top View)

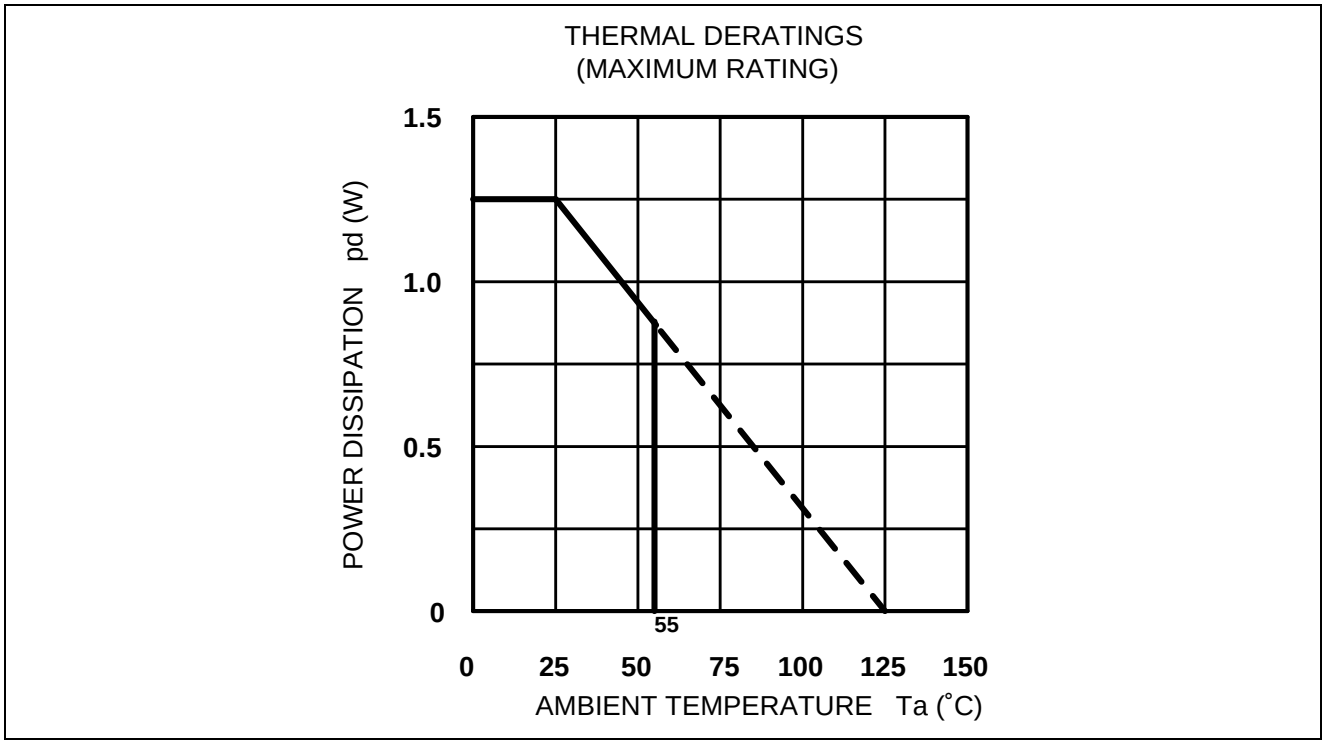


Pin Description

PIN No.	Name	Function
5,3,1,79,77,75,73, 71,69	INR1,2,3,4,5,6,7,8,9	Input pin of R channel (Input Selector)
4,2,80,78,76,74,72, 70,68	INL1,2,3,4,5,6,7,8,9	Input pin of L channel (Input Selector)
6,13,16,19,32,57,64	GND	Analog Ground
7,24	CIN1/CIN2	Input pin of C channel (2 Input Selector)
8,25	SWIN1/SWIN2	Input pin of SW channel (2 Input Selector)
9,22	SRIN1/SRIN2	Input pin of SR channel (2 Input Selector)
10,23	SLIN1/SLIN2	Input pin of SL channel (2 Input Selector)
11,20	LIN1/LIN2	Input pin of L channel (2 Input Selector)
12,21	RIN1/RIN2	Input pin of R channel (2 Input Selector)
14,15	BALANCE L/+,L/-	Output pin of L channel Balance Output(+/-)
17,18	BALANCE R/+,R/-	Output pin of R channel Balance Output(+/-)
26	DGND	Ground of internal logic circuit
27,28,29	CLOCK,DATA,LATCH	Input pin of Control clock /data/ trigger
30	DVDD	Power supply to internal logic circuit
31	AVCC	Positive power supply to internal analog circuit
33	SWSELOUT	Output pin of SW channel volume input selector
34	SWVIN	Input pin of SW channel volume
35	SWOUT	Output pin of SW channel
36	COUT	Output pin of C channel
37	CVIN	Input pin of C channel volume
38	CSELOUT	Output pin of C channel volume input selector
39	SLSELOUT	Output pin of SL channel volume input selector
40	SLVIN	Input pin of SL channel volume
41	SLOUT	Output pin of SL channel
48,49,50,51,52,53	NC	Non-connection terminal
42	SROUT	Output pin of SR channel
43	SRVIN	Input pin of SR channel volume
44	SRSELOUT	Output pin of SR channel volume input selector
45	RSELOUT	Output pin of R channel volume input selector
46	RVIN	Input pin of R channel volume
47	ROUT	Output pin of R channel
54	LOUT	Output pin of L channel
55	LVIN	Input pin of L channel volume
56	LSELOUT	Output pin of L channel volume input selector
58,60,62 /59,61,63	REC L1,L2,L3 /REC R1,R2,R3	Output pin of REC (Lch and Rch)
65	INL10/REC L4	Input pin of L channel (Input Selector) / Output pin of REC (Lch)
66	INR10/REC R4	Input pin of R channel (Input Selector) / Output pin of REC (Rch)
67	AVEE	Negative power supply to internal analog circuit

Absolute Maximum Ratings

Symbol	Parameter	Condition	Ratings	Unit
Supply voltage	Power supply	AVCC-AVEE	±8.0	V
		DVDD-GND	6.0	
Pd	Power dissipation	Ta≤25°C	1250	mW
Kθ	Thermal derating	Ta>25°C	12.5	mW/°C
Topr	Operating temperature		-20 to +55	°C
Tstg	Storage temperature		-40 to +125	°C



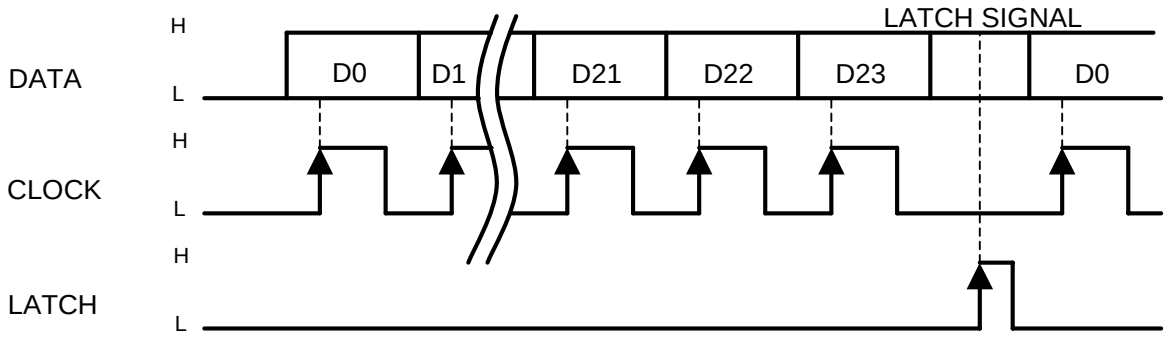
Recommended Operating Conditions

(Ta=25°C, unless otherwise noted)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Analog supply voltage (Positive)	AVCC		4.5	7.0	7.5	V
Analog supply voltage (Negative)	AVEE		-7.5	-7.0	-4.5	V
Digital supply voltage	DVDD		3.0	3.3	5.5	V
Logic “H” level input voltage	VIH	DGND reference	DVDD x 0.7	—	DVDD	V
Logic “L” level input voltage	VIL	DGND reference	DGND	—	DVDD x 0.2	V

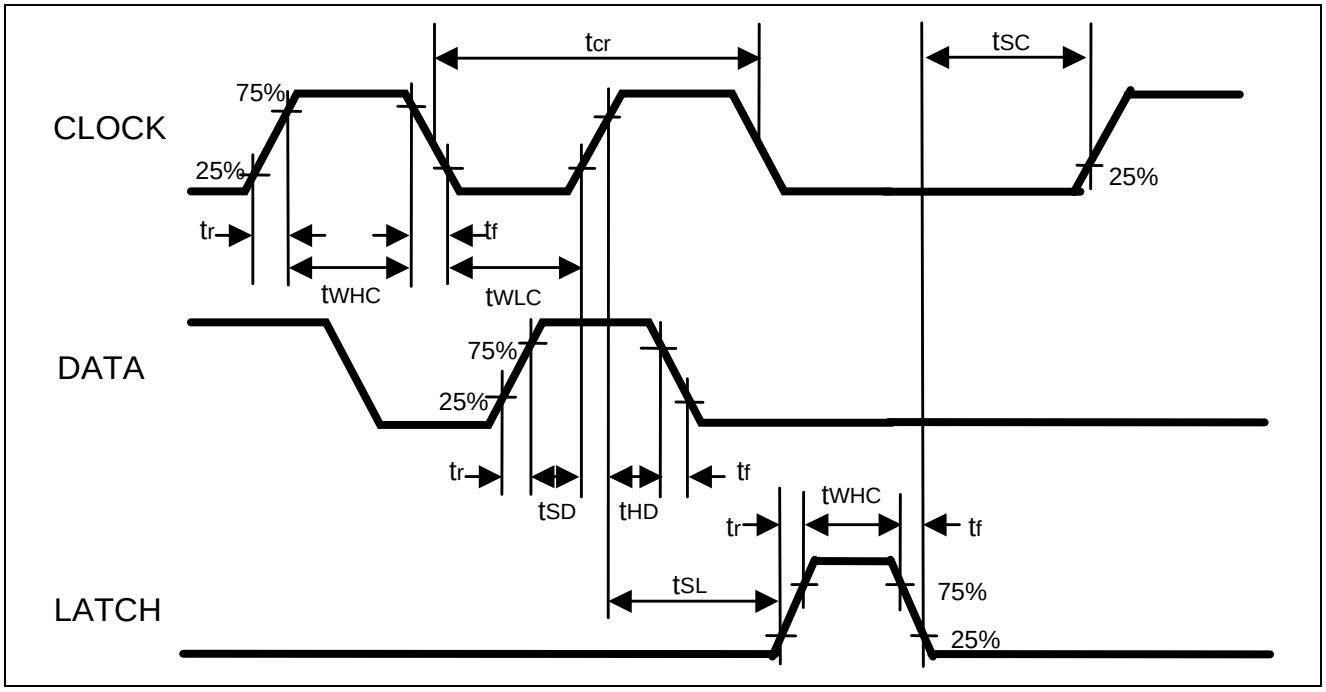
Note: AVEE≤DGND<DVDD≤AVCC

Relationship between Data and Clock



DATA signal is read at the rising edge of CLOCK.
Serial data (D0–D23) is loaded at the rising edge of the LATCH signal.

Clock and Data Timings

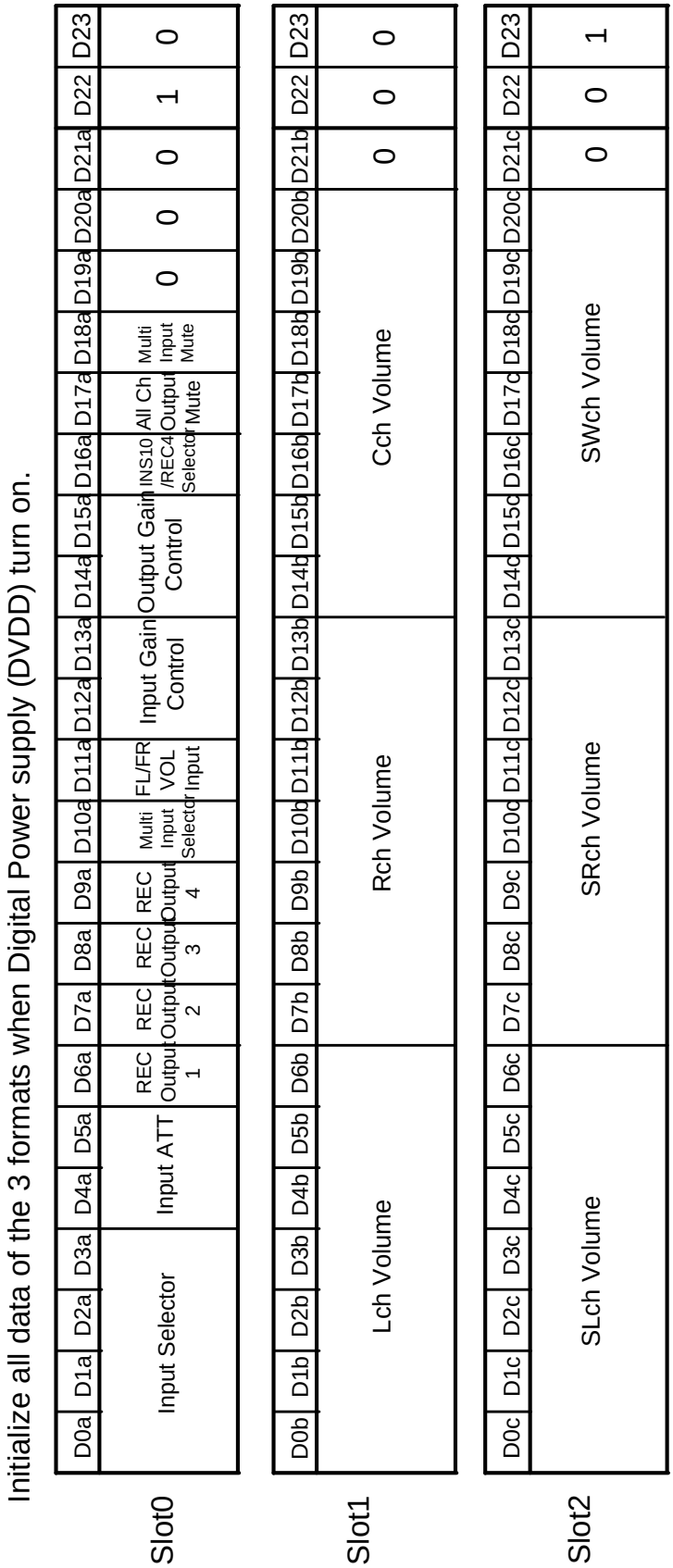


Timing Definition of Digital Block

Symbol	Parameter	Limits			Unit
		Min	typ	Max	
tcr	Clock cycle time	4	—	—	µsec
tWHC	Clock pulse width (“H” level)	1.6	—	—	
tWLC	Clock pulse width (“L” level)	1.6	—	—	
tr	Rising time of clock,data and latch	—	—	0.4	
tf	Falling time of clock,data and latch	—	—	0.4	
tSD	Data setup time	0.8	—	—	
tHD	Data hold time	0.8	—	—	
tSL	Latch setup time	1	—	—	
tWHL	Latch pulse width	1.6	—	—	
tSC	Clock setup time	4	—	—	

Data Control Specification

Initialize all data of the 3 formats when Digital Power supply (DVDD) turn on.



Setting Code

(1)Input Selector

Setting	D0a	D1a	D2a	D3a
ALL OFF	0	0	0	0
IN1	0	0	0	1
IN2	0	0	1	0
IN3	0	0	1	1
IN4	0	1	0	0
IN5	0	1	0	1
IN6	0	1	1	0
IN7	0	1	1	1
IN8	1	0	0	0
IN9	1	0	0	1
IN10	1	0	1	0

(2)Input ATT

Setting	D4a	D5a
0dB	0	0
-6dB	0	1
-12dB	1	0
-18dB	1	1

(3)REC Output

REC Output	REC1	REC2	REC3	REC4
Setting	D6a	D7a	D8a	D9a
OFF	0	0	0	0
ON	1	1	1	1

(10)All Ch Output Mute

Setting	D17a
Mute off	0
Mute on	1

(11)Multi Input Mute(Except for L/R)

Setting	D18a
Mute off Depend on (4) Multi Input	0
Mute on	1

(4)Multi Input Selector

Setting	D10a
Multi IN1	0
Multi IN2	1

(5)FL/FR VOL Input

Setting	D11a
Bypass	0
Multi Input	1

(6)Input Gain Control

Setting	D12a	D13a
0dB	0	0
+6dB	0	1
+12dB	1	0
+18dB	1	1

(7)Output Gain Control

Setting	D14a	D15a
0dB	0	0
+6dB	0	1
+12dB	1	0
+18dB	1	1

(8)IN10/REC4 Selector

Setting	D16a
IN10	0
REC4	1

It's initial setting when power is turned on.

Note : Please don't input except specification data.

(9)6 channel Volume

ATT	Lch	D0b	D1b	D2b	D3b	D4b	D5b	D6b
	SLch	D0c	D1c	D2c	D3c	D4c	D5c	D6c
	Rch	D7b	D8b	D9b	D10b	D11b	D12b	D13b
	SRch	D7c	D8c	D9c	D10c	D11c	D12c	D13c
	Cch	D14b	D15b	D16b	D17b	D18b	D19b	D20b
	SWch	D14c	D15c	D16c	D17c	D18c	D19c	D20c
0dB		0	0	0	0	0	0	0
-1dB		0	0	0	0	0	0	1
-2dB		0	0	0	0	0	1	0
-3dB		0	0	0	0	0	1	1
-4dB		0	0	0	0	1	0	0
-5dB		0	0	0	0	1	0	1
-6dB		0	0	0	0	1	1	0
-7dB		0	0	0	0	1	1	1
-8dB		0	0	0	1	0	0	0
-9dB		0	0	0	1	0	0	1
-10dB		0	0	0	1	0	1	0
-11dB		0	0	0	1	0	1	1
-12dB		0	0	0	1	1	0	0
-13dB		0	0	0	1	1	0	1
-14dB		0	0	0	1	1	1	0
-15dB		0	0	0	1	1	1	1
-16dB		0	0	1	0	0	0	0
-17dB		0	0	1	0	0	0	1
-18dB		0	0	1	0	0	1	0
-19dB		0	0	1	0	0	1	1
-20dB		0	0	1	0	1	0	0
-21dB		0	0	1	0	1	0	1
-22dB		0	0	1	0	1	1	0
-23dB		0	0	1	0	1	1	1
-24dB		0	0	1	1	0	0	0
-25dB		0	0	1	1	0	0	1
-26dB		0	0	1	1	0	1	0
-27dB		0	0	1	1	0	1	1

ATT	Lch	D0b	D1b	D2b	D3b	D4b	D5b	D6b
	SLch	D0c	D1c	D2c	D3c	D4c	D5c	D6c
	Rch	D7b	D8b	D9b	D10b	D11b	D12b	D13b
	SRch	D7c	D8c	D9c	D10c	D11c	D12c	D13c
	Cch	D14b	D15b	D16b	D17b	D18b	D19b	D20b
	SWch	D14c	D15c	D16c	D17c	D18c	D19c	D20c
-28dB		0	0	1	1	1	0	0
-29dB		0	0	1	1	1	0	1
-30dB		0	0	1	1	1	1	0
-31dB		0	0	1	1	1	1	1
-32dB		0	1	0	0	0	0	0
-33dB		0	1	0	0	0	0	1
-34dB		0	1	0	0	0	1	0
-35dB		0	1	0	0	0	1	1
-36dB		0	1	0	0	1	0	0
-37dB		0	1	0	0	1	0	1
-38dB		0	1	0	0	1	1	0
-39dB		0	1	0	0	1	1	1
-40dB		0	1	0	1	0	0	0
-41dB		0	1	0	1	0	0	1
-42dB		0	1	0	1	0	1	0
-43dB		0	1	0	1	0	1	1
-44dB		0	1	0	1	1	0	0
-45dB		0	1	0	1	1	0	1
-46dB		0	1	0	1	1	1	0
-47dB		0	1	0	1	1	1	1
-48dB		0	1	1	0	0	0	0
-49dB		0	1	1	0	0	0	1
-50dB		0	1	1	0	0	1	0
-51dB		0	1	1	0	0	1	1
-52dB		0	1	1	0	1	0	0
-53dB		0	1	1	0	1	0	1
-54dB		0	1	1	0	1	1	0
-55dB		0	1	1	0	1	1	1

ATT		D0b	D1b	D2b	D3b	D4b	D5b	D6b
	Lch	D0b	D1b	D2b	D3b	D4b	D5b	D6b
	SLch	D0c	D1c	D2c	D3c	D4c	D5c	D6c
	Rch	D7b	D8b	D9b	D10b	D11b	D12b	D13b
	SRch	D7c	D8c	D9c	D10c	D11c	D12c	D13c
	Cch	D14b	D15b	D16b	D17b	D18b	D19b	D20b
	SWch	D14c	D15c	D16c	D17c	D18c	D19c	D20c
-56dB		0	1	1	1	0	0	0
-57dB		0	1	1	1	0	0	1
-58dB		0	1	1	1	0	1	0
-59dB		0	1	1	1	0	1	1
-60dB		0	1	1	1	1	0	0
-61dB		0	1	1	1	1	0	1
-62dB		0	1	1	1	1	1	0
-63dB		0	1	1	1	1	1	1
-64dB		1	0	0	0	0	0	0
-65dB		1	0	0	0	0	0	1
-66dB		1	0	0	0	0	1	0
-67dB		1	0	0	0	0	1	1
-68dB		1	0	0	0	1	0	0
-69dB		1	0	0	0	1	0	1
-70dB		1	0	0	0	1	1	0
-71dB		1	0	0	0	1	1	1
-72dB		1	0	0	1	0	0	0
-73dB		1	0	0	1	0	0	1
-74dB		1	0	0	1	0	1	0
-75dB		1	0	0	1	0	1	1
-76dB		1	0	0	1	1	0	0
-77dB		1	0	0	1	1	0	1
-78dB		1	0	0	1	1	1	0
-79dB		1	0	0	1	1	1	1
-80dB		1	0	1	0	0	0	0
-81dB		1	0	1	0	0	0	1
-82dB		1	0	1	0	0	1	0

ATT		D0b	D1b	D2b	D3b	D4b	D5b	D6b
	Lch	D0b	D1b	D2b	D3b	D4b	D5b	D6b
	SLch	D0c	D1c	D2c	D3c	D4c	D5c	D6c
	Rch	D7b	D8b	D9b	D10b	D11b	D12b	D13b
	SRch	D7c	D8c	D9c	D10c	D11c	D12c	D13c
	Cch	D14b	D15b	D16b	D17b	D18b	D19b	D20b
	SWch	D14c	D15c	D16c	D17c	D18c	D19c	D20c
-83dB		1	0	1	0	0	1	1
-84dB		1	0	1	0	1	0	0
-85dB		1	0	1	0	1	0	1
-86dB		1	0	1	0	1	1	0
-87dB		1	0	1	0	1	1	1
-88dB		1	0	1	1	0	0	0
-89dB		1	0	1	1	0	0	1
-90dB		1	0	1	1	0	1	0
-91dB		1	0	1	1	0	1	1
-92dB		1	0	1	1	1	0	0
-93dB		1	0	1	1	1	0	1
-94dB		1	0	1	1	1	1	0
-95dB		1	0	1	1	1	1	1
-96dB		1	1	0	0	0	0	0
-97dB		1	1	0	0	0	0	1
-98dB		1	1	0	0	0	1	0
-99dB		1	1	0	0	0	1	1
-∞ dB		1	1	1	1	0	0	0

Note : Please don't input except specification data.

Electrical Characteristics

Unless otherwise noted, Ta=25°C, AVCC=7V, AVEE=-7V, DVDD=3.3V, f=1kHz, Volume=0dB,
Input Selector=IN1, Input ATT=0dB, Input Gain Control=0dB, Output Gain Control=0dB,
FL/FR Volume Input=Bypass, Multi Input Selector=Multi IN1 setting

(1) Power supply characteristics

Symbol	Parameter	Test condition	Limits			Unit
			min	typ	max	
Analog positive power circuit current	AIcc	With AVCC=7V and AVEE=-7V Pin31 pin current, when no signal is provided	—	50	70	mA
Analog negative power Circuit current	AIee	With AVCC=7V and AVEE=-7V Pin67 pin current, when no signal is provided	-70	-50	—	mA
Digital power circuit current	DIdd	With DVDD=3.3V, Pin30 pin current, when no signal is provided	—	3	6	mA

(2) Input/Output characteristics (OVER ALL)

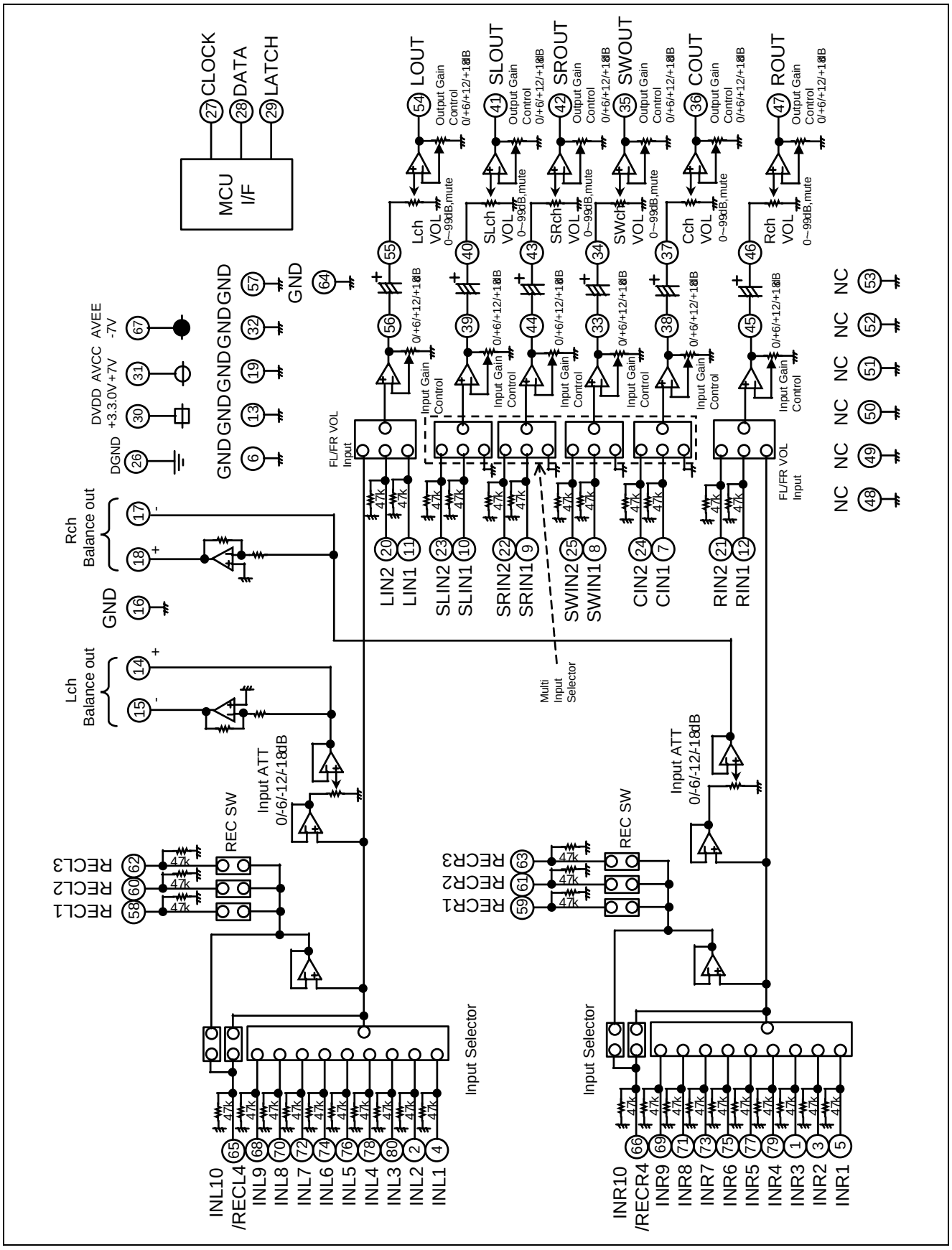
Symbol	Parameter	Test condition		Limits min	Limits typ	Limits max	Unit
Input resistance	Rin	1 to 5,65,66,68 to 80pin When each selector chooses a terminal concerned.		35	47	65	kΩ
Maximum output voltage	VOM	(4,5,7,8,9,10)pin input, (54,47,36,35,42,41)pin output, THD=1%, RL=10kΩ Output Gain Control=+12dB setting		3.6	4.2	—	Vrms
Pass gain	Gv	(4,5,7,8,9,10)pin input, (54,47,36,35,42,41)pin output, Vi=0.3Vrms,FLAT		-2.0	0	2.0	dB
Distortion	THD1	(4,5,7,8,9,10)pin input, (54,47,36,35,42,41)pin output, BW:400Hz to 30kHz, f=1kHz, Vo=0.3Vrms, RL=10kΩ		—	0.005	0.05	%
	THD2	(4,5,7,8,9,10)pin input,(54,47,36,35,42,41)pin output, BW: 400Hz to 30kHz, f=1kHz, Vo=2Vrms, RL=10kΩ		—	0.03	0.1	%
Channels balance	CBAL	(4,5)pin input, (54,47)pin output, Vi=0.3Vrms, JIS-A		-0.5	0	0.5	dB
Output noise voltage	Vono (VOL=-∞dB)	JIS-A, (4,5,7,8,9,10)pin: Rg=0Ω, (54,47,36,35,42, 41)pin output, Volume=-∞dB setting	Output Gain Control=0dB	—	1.5	6	μVrms
			Output Gain Control=+12dB	—	9	20	μVrms
	Vono (VOL=0dB)	JIS-A, (4,5,7,8,9,10)pin: Rg=0Ω, (54,47,36,35,42, 41)pin output, Volume=0dB setting	Output Gain Control=0dB	—	2.5	8	μVrms
			Output Gain Control=+12dB	—	12	25	μVrms
	Vonobal (Balance out)	JIS-A, (4,5)pin:Rg=0Ω, (14,15,17,18)pin output		—	5	10	μVrms
Input/Multi selector channel separation	CS1	< Input selector > (54,47)pin output, Vo=1Vrms, Rg=0Ω, RL=10kΩ, JIS-A		—	-90	-70	dB
	CS2	< Multi channel selector > (35,36,41,42,47,54)pin output, Vo=1Vrms, Rg=0Ω, RL=10kΩ, JIS-A, FL/FR VOL Input=Multi input		—	-90	-70	dB

Symbol	Parameter	Test condition	Limits			Unit
			min	typ	max	
Cross talk between channels	CT1 (FL/FR)	(4,5)pin input, (47,54)pin output, Vo=1Vrms, Rg=0Ω, RL=10kΩ, JIS-A	—	-90	-70	dB
	CT2 (Multi Input)	(7,8,9,10,11,12)pin input, (35,36,41,42,47,54)pin output, Vo=1Vrms, Rg=0Ω, RL=10kΩ, JIS-A, FL/FR VOL Input=Multi input	—	-90	-70	dB

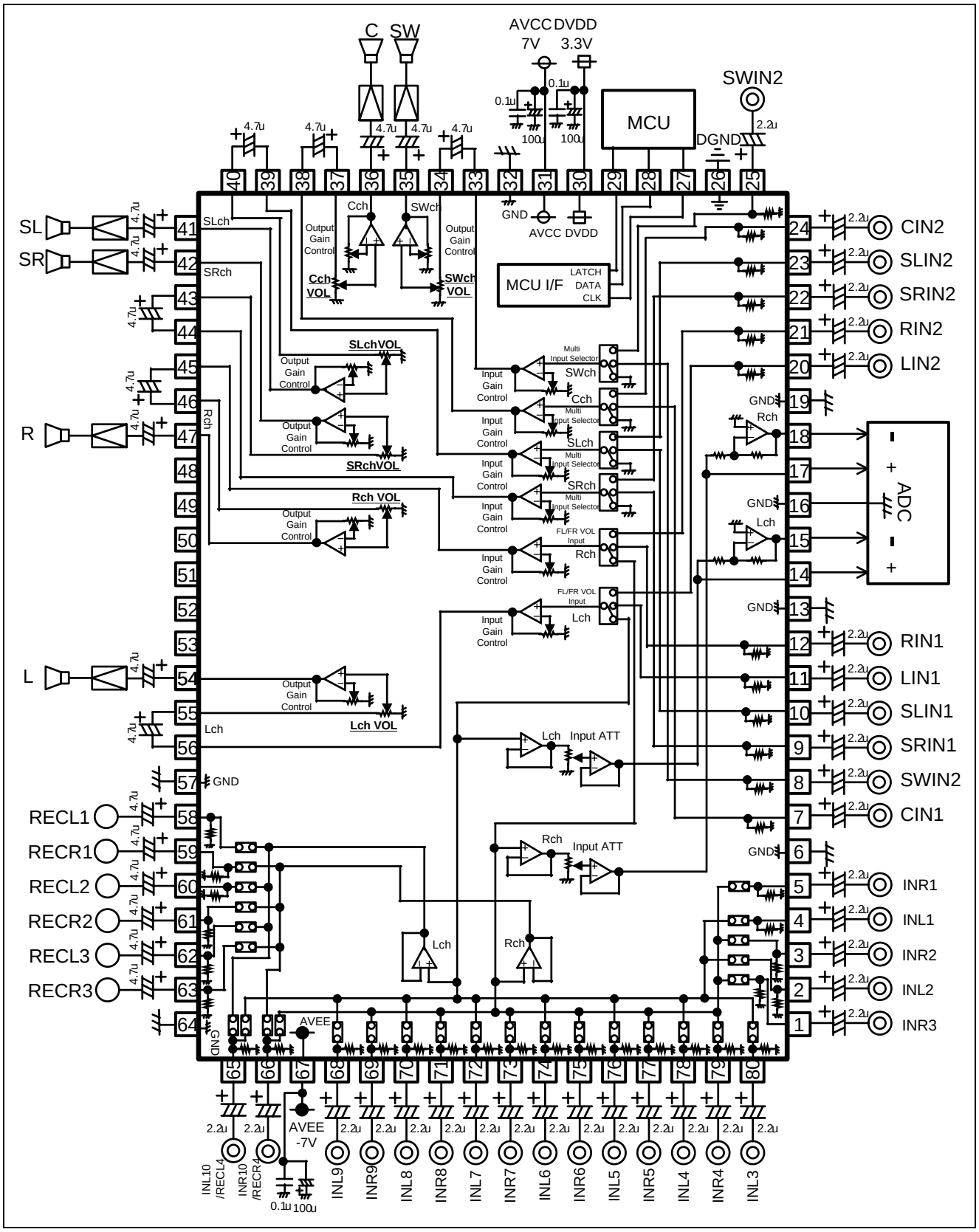
(3) 6 channel Volume characteristics

Symbol	Parameter	Test condition	Limits			Unit
			min	typ	max	
Maximum attenuation	ATTmax	(35,36,41,42,47,54)pin output, Vi=2Vrms,JIS-A,VOL=-∞	—	-100	-95	dB
Volume gain Between channels	Dvol	35,36,41,42,47,54)pin output, Volume=0dB setting	-0.5	0	+0.5	dB

Internal Block Diagram



Application Example



Package Dimensions

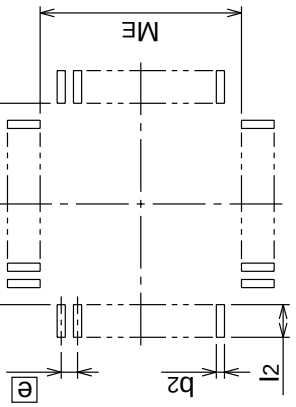
Plastic 80pin 14X20mm body QFP

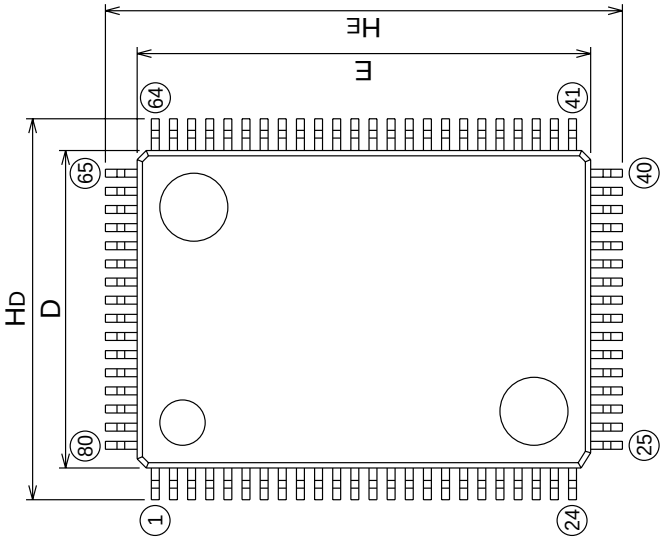
80P6N-A (MMP)

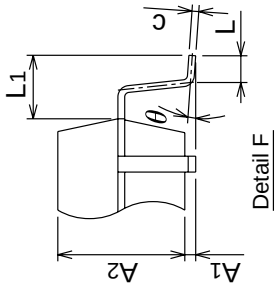
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	—	1.58	Alloy 42

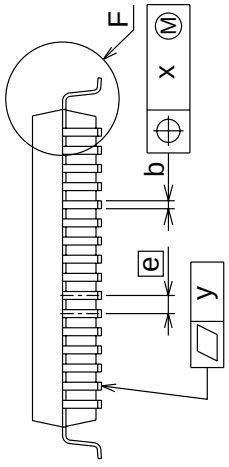
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A_1	0	0.1	0.2
A_2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.8	—
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	—	1.4	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.5	—
l_2	1.3	—	—
M_D	—	14.6	—
M_E	—	20.6	—

Recommended Mount Pad









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