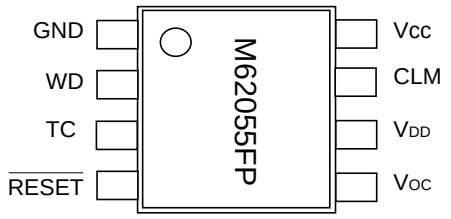
M62055FP

3V POWER SUPPLY with WATCHDOG TIMER

GENERAL DESCRIPTION

M62055FP is a 3V power supply featuring a watchdog timer function for a microcontroller system.
It can be a power source of 3V ± 5% by utilizing the reference voltage and amplifier.
It can also generate a reset pulse for the applied systems during power-on, moreover it includes the watchdog timer for a self diagnostics of the system, which can prevent system erroneous functions.

PIN CONFIGURATION(TOP VIEW)



Outline 8P2S

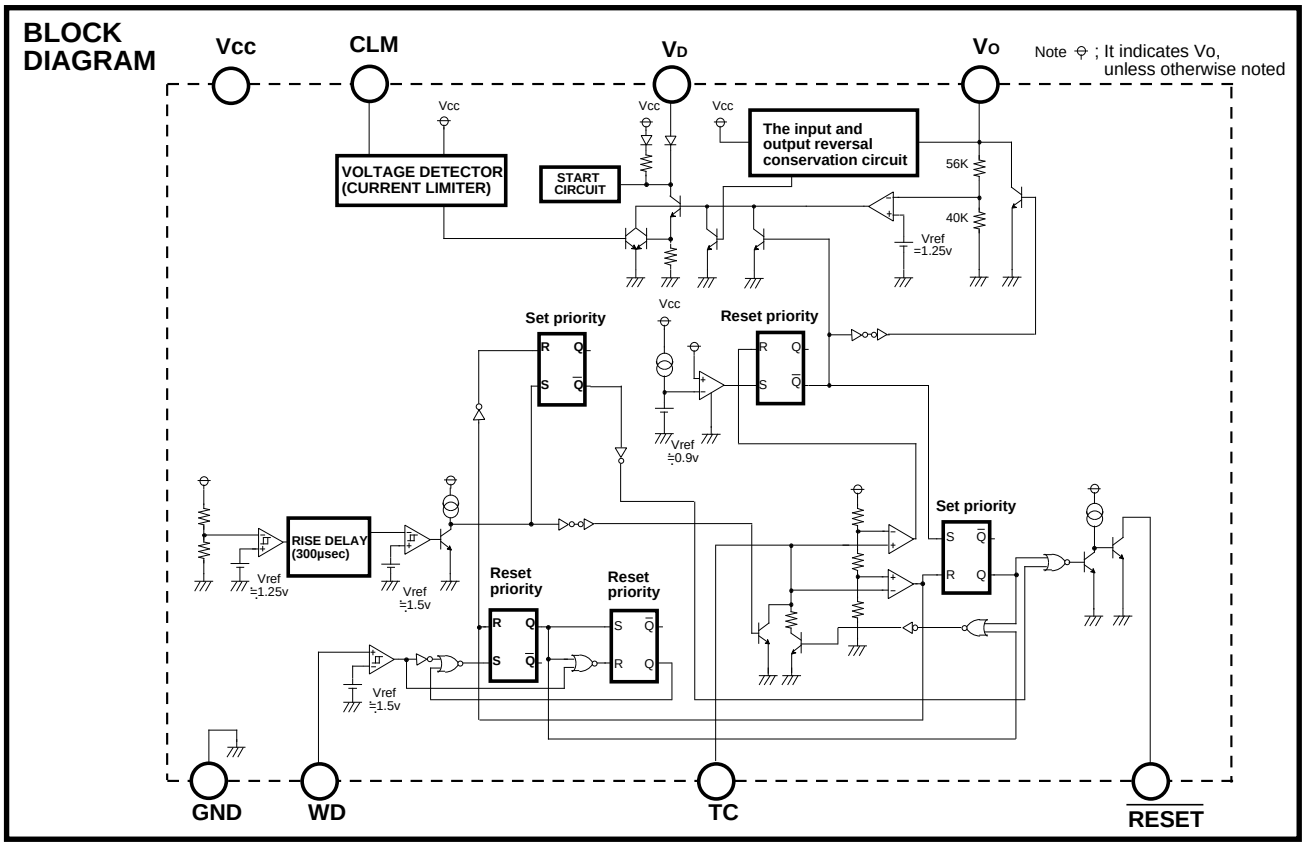
FEATURES

- **Power-on reset**
- **Watchdock timer**
- **High accuracy voltage source of 3V ±5% (max)**
- **Overcurrent protection circuit**
- **The voltage detection accuracy of ±5% (max)**
- **Output power (Vo) cutoff function at erroneous conditions**
- **Backward voltage protection circuits for inputs and outputs**

APPLICATION

Handy information terminal equipment, CD-ROM, Portable audio equipment.

BLOCK DIAGRAM



Pin Functional description

pin number	symbol	Functional description
1	GND	Ground
2	WD	Input for watchdock timer.
3	TC	Setting up reset timer and watchdock timer.
4	$\overline{\text{RESET}}$	Reset signal output
5	VO	Feedback to a power supply for a MCU.
6	VD	Controlling the stability of an output voltage with a PNP transistor connected externally.
7	CLM	Current limiting
8	Vcc	Power supply voltage

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, Unless otherwise noted)

symbol	Parameter		conditions	Ratings	Unit
Vcc	supply voltage			13	V
VRM	Reset pin	Output voltage		10	V
IRM		Output current		10	mA
V_{WDM}	Watchdock pin input voltage			3	V
Kθ	Thermal derating		Ta ≥ 25°C	4.0	mW/°C
Topr	Operating temperature			- 20 ~ + 75	°C
Tstg	Storage temperature			- 55 ~ + 150	°C

ELECTRICAL CHARACTERISTICS (Vcc=5.0V,Ta=25°C, Unless otherwise noted)

(1) DC CHARACTERISTICS

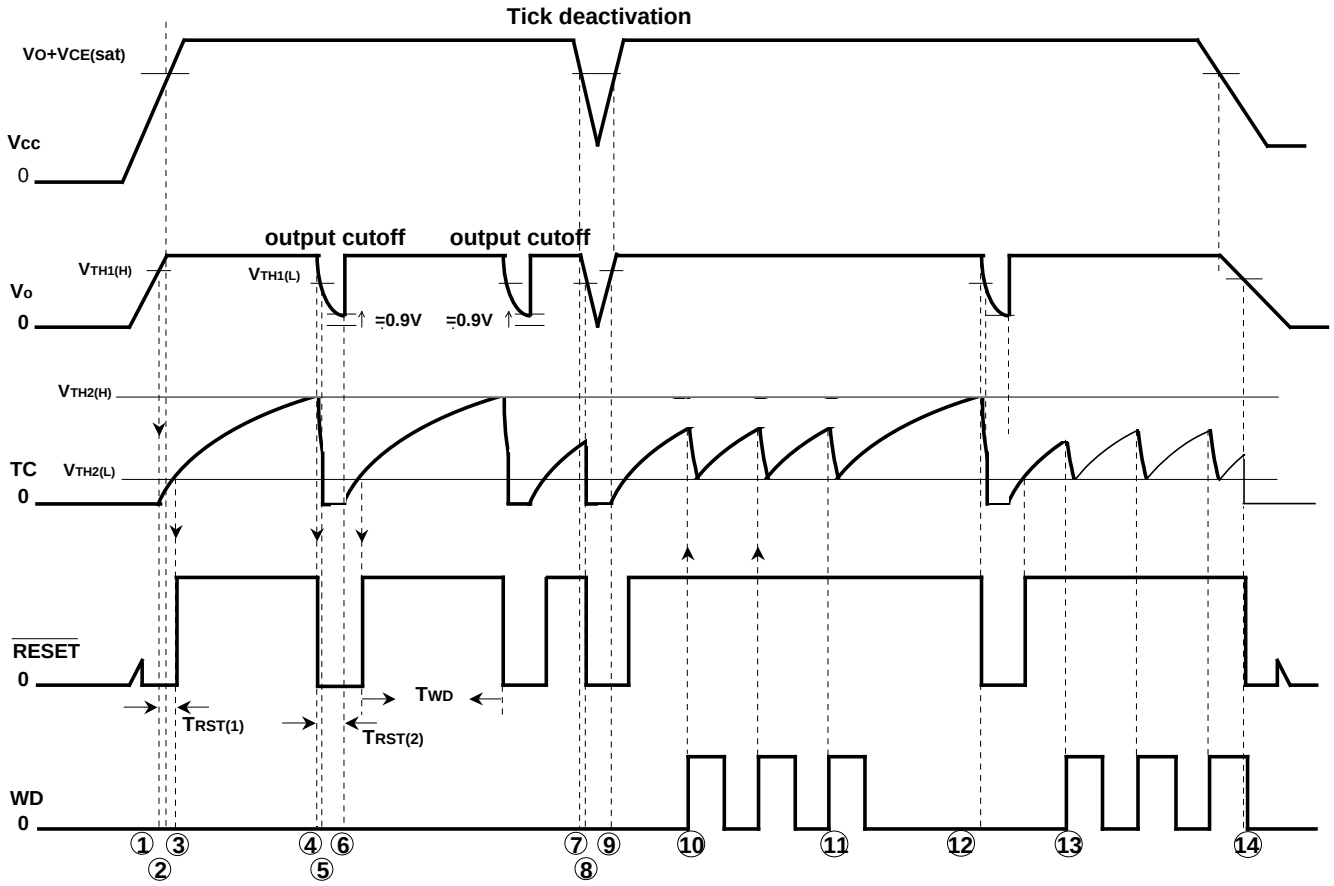
symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Battery• back up• regulator						
V_{CC}	supply voltage		3.5		13	V
I_{CC}	Circuitry current			650	950	µA
V_O	Output voltage		2.85	3.0	3.15	V
I_{Bmax}	Bias current			10		mA
I_{BSC}	Listing short-circuit bias current			1.5		mA
Reg-in	Input voltage regulation	Vcc=3.5V~13V		0.02	0.25	%/V
Reg-lo	Loading voltage regulation	Io=10mA~100mA		1	25	mV
$\Delta Vo/\Delta T$	Output voltage thermal coefficient			0.02		%/T
V_{THCLM}	CLM threshold voltage		180	200	220	mV
Reset, watch dock timer						
$V_{TH1(H)}$	Vo detection voltage		2.68	2.82	2.96	V
$V_{TH1(L)}$			2.58	2.72	2.86	V
ΔV_{TH1}				0.1		V
$V_{OL(RST)}$	Output voltage (Reset pin)	Isink=4mA		0.2	0.4	V
Ileak	Output leakage current (Reset pin)				5	µA
$V_{TH2(H)}$	Watchdock timer threshold voltage		2.28	2.4	2.52	V
$V_{TH2(L)}$			0.95	1.0	1.05	V
I_{WD}	WD input current	VIN=3V			1	µA
$V_{TH(WD)}$	WD input threshold voltage			1.5		V
I_{tco}	TC output current	VIN=0.8V			1	µA
I_{tc1}	TC input current	VIN=2.4V		2.0		mA
I_{tc2}		In the output cutoff transmission mode	8.0			mA
V_{CCMIN}	Vcc min operating voltage	*1			2.0	V

Note *1; The Vcc minimum operating voltage at which the $\overline{\text{RESET}}$ output is Low

(2) AC CHARACTERISTICS (Vcc=5.0V,Ta=25°C, Unless otherwise noted)

symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{WD}	Watch dock timer	C=0.1µF,R1=10KΩ	0.5	1.2	1.7	mS
$t_{RST(1)}$	Reset timer (1)	C=0.1µF,R1=10KΩ		0.7		mS
$t_{RST(2)}$	Reset timer (2)	CO=10µF, R1=10KΩ, IL=0	0.1		2.0	mS

FUNCTIONAL DESCRIPTION



① : When Vo rises to 0.5 V, $\overline{\text{RESET}}$ becomes low. Then, charging to a capacitor C connected to TC will be started at the Vo of 2.82V($V_{TH1(H)}$).

② : When V_{CC} rises to 3V+V_{CE}(sat), Vo becomes stable.

③④: When TC voltage rises to 1V($V_{TH2(L)}$) , $\overline{\text{RESET}}$ becomes high. When it rises to 2.4V ($V_{TH2(H)}$) further, the capacitor C is switched to discharge and $\overline{\text{RESET}}$ becomes low.

⑤ : At the same time of a change-over to the discharge from the capacitor C, Vo is intercepted.
Then,TC will be discharged completely at Vo of 2.72V($V_{TH1\ (L)}$).

⑥ : Vo returns to 3V right after it has fallen down to 0.9 V.
$\overline{\text{RESET}}$ repeats above operation till a normal clock signal is input to WD pin.

⑦⑧⑨ : In the case of a sudden power interruption, Vo falls down according to a decrease of V_{CC}. When it falls down to 2.72V, the capacitor C is discharged and $\overline{\text{RESET}}$ will be low.
In the case of a reversion from the power interruption, Vo rises according to a increase of V_{CC}. When it rises to 2.82V, the charging to the capacitor C is started and $\overline{\text{RESET}}$ will be high right after TC voltage reaches 1V.

⑩⑪ : In the case a clock signal for discharging the capacitor C is applied to pin WD before TC voltage reaches to 2.4V, a reset signal to $\overline{\text{RESET}}$ is canceled.

⑫⑬ : In the case an abnormal clock signal is input, TC repeats charging / discharging alternately between 1 V and 2.4 V, so that $\overline{\text{RESET}}$ also repeats high / low till a normal clock signal is input.

⑭ : When Vo falls down to 2.72 V, $\overline{\text{RESET}}$ becomes Low.

DESCRIPTION of TERMS

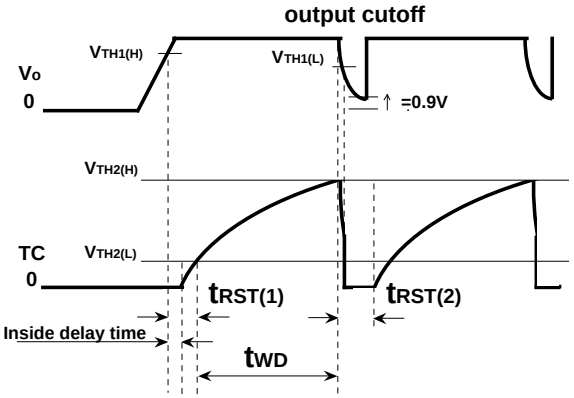
$t_{RST(1)}$ Time from when TC begins to charge until it reaches to $V_{TH2(L)}$.

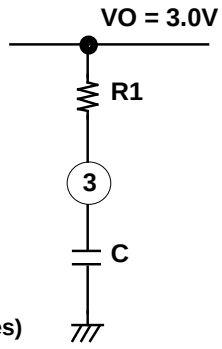
t_{WD} Time from when TC is $V_{TH2(L)}$ until it reaches to $V_{TH2(H)}$.

$t_{RST(2)}$ Time from when TC is $V_{TH2(H)}$ until TC starts charging.

1. Pin③ (TC pin) Charging and discharging time .

When an error is occurred in WD input, TC waveform is as shown below.





$t_{RST(1)} = 0.406 \cdot C \cdot R_1 + 300\mu s$ *1

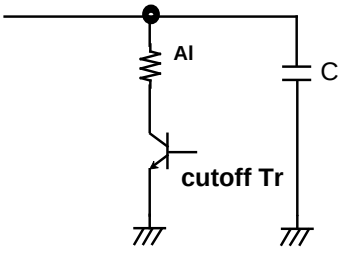
$t_{WD} = 1.2 \cdot C \cdot R_1$ (Charging time)

*1 : Inside delay time (Typical values)

The following formula can be obtained because $t_{RST(2)}$ is equal to the duration of Vo cutoff.

$$t_{RST(2)} = C \cdot R^{*3} \cdot \ln\left(\frac{3}{0.9}\right) + 300\mu s^{*2}$$

$$= 40 \cdot C + 300\mu s^{*2}$$

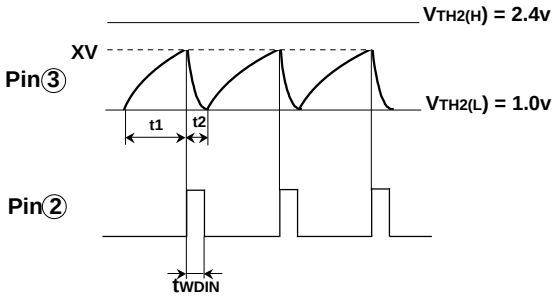


*2 : Inside delay time (Typical values)

*3 : R = Internal resistance

2. Pin② (WD pin) Input frequency, input pulse width, charge/discharge time .

When input of② WD is normal, TC waveform ③ is as shown below.



$$t_1 = C \cdot R_1 \cdot \ln\frac{2}{3-X}$$

$$t_2 = 1000 \cdot C \cdot R1 \cdot \ln\frac{X\left(\frac{R_1}{1000} + 1\right) - 3}{\frac{R_1}{1000} - 2}$$

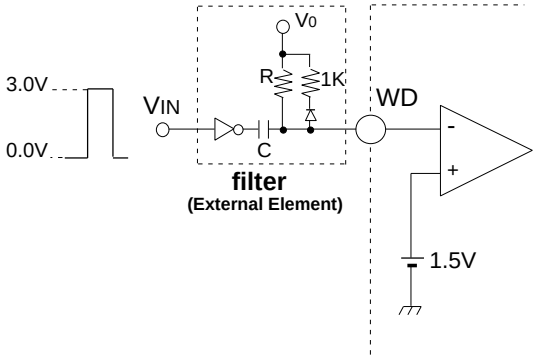
Conditions of an input to pin② (WD pin)

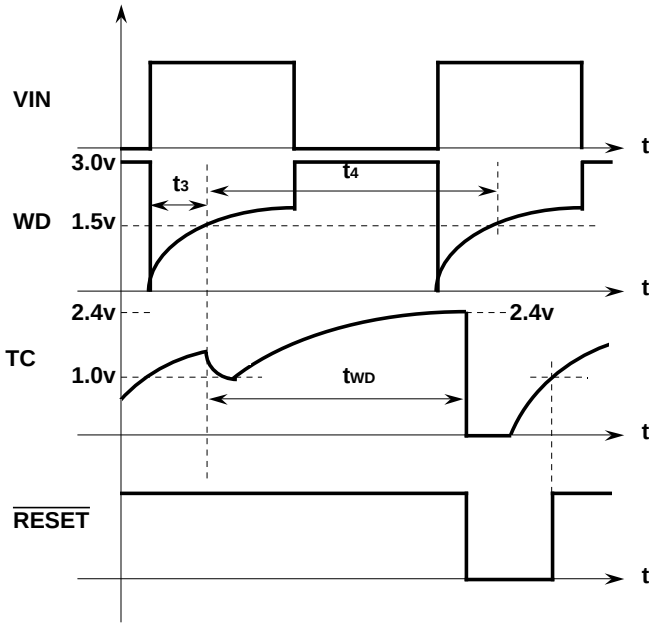
(1) Input period should be t_{WD} or less.
(Pin discharge is completed before the arrival of VTH2(H) = 2.4 V)

$$\frac{1}{1.2 \cdot C \cdot R_1} < f$$

(2) Input pulse width t_{WDIN} should be t_2 or less.

3. Relationship between the input pulse width and the low pass filter





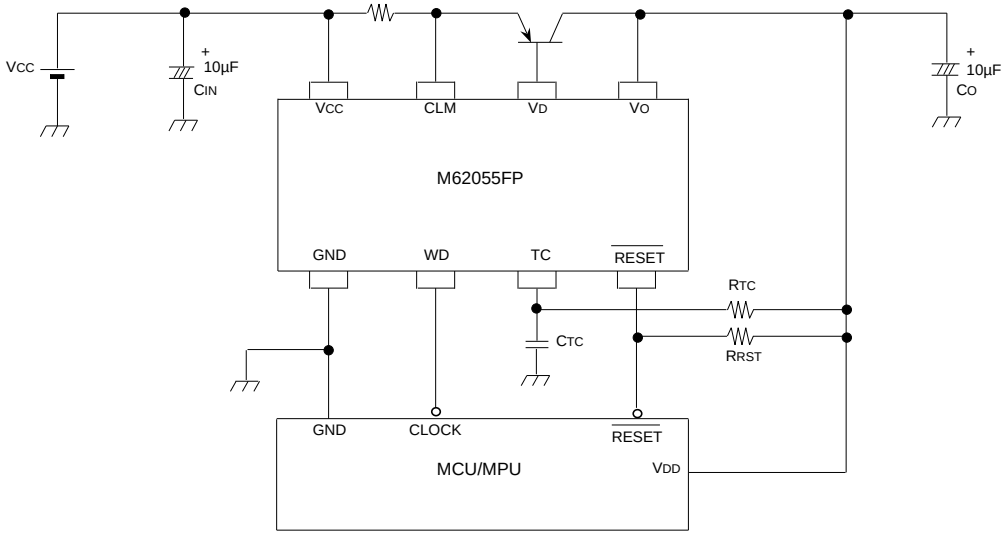
Addition of a low pass filter makes input waveform dull. An input pulse width and CR of a low pass filter is determined referring to the right figure.

$$t_3 = -C \cdot R \cdot \ln \frac{1.5v}{V_{IN}}$$

$\overline{\text{RESET}}$ is output in the case of $t_4 > t_{WD}$.

If t3 is too long, the TC waveform changes as shown in the diagram above.
t3 is set as follows; t_{WDIN} (3 µs) or more and t_2 (charging time) or less.
(t2 is a discharge time while an input is normal)

APPLICATION



Note : h_{FE} of the external PNP transistor, 100 to 300 is recommended.