M62352AGP

8BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

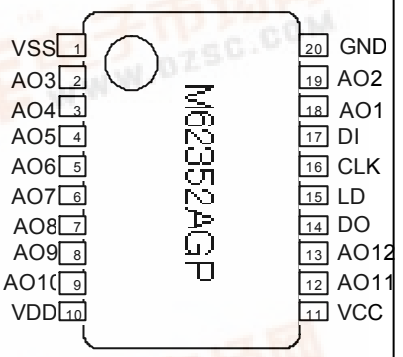
DESCRIPTION

M62352A is a CMOS structured semiconductor integrated ciruict integrating 12 channels of built-in D-A converters with high performance buffer operational amplifierf or each channel output.

3-wire serial interface (DI,CLK,LD) method is used for the taransfer format of digital data to allow connection with microcomputer with minimum wiring Do terminal is provided to allow cascading serial use.

Built-in buffer operational amplifiers are designed to operate or full-swing in the whole voltage range from Vcc to GND for each input/output. And their higher stability for capacitive load perfectly fits in to the use for electronic volume (VCA) or the replacement for semi-variable resistor for tuning.

Pin configuration(Top View)



Outline 20P2E-A

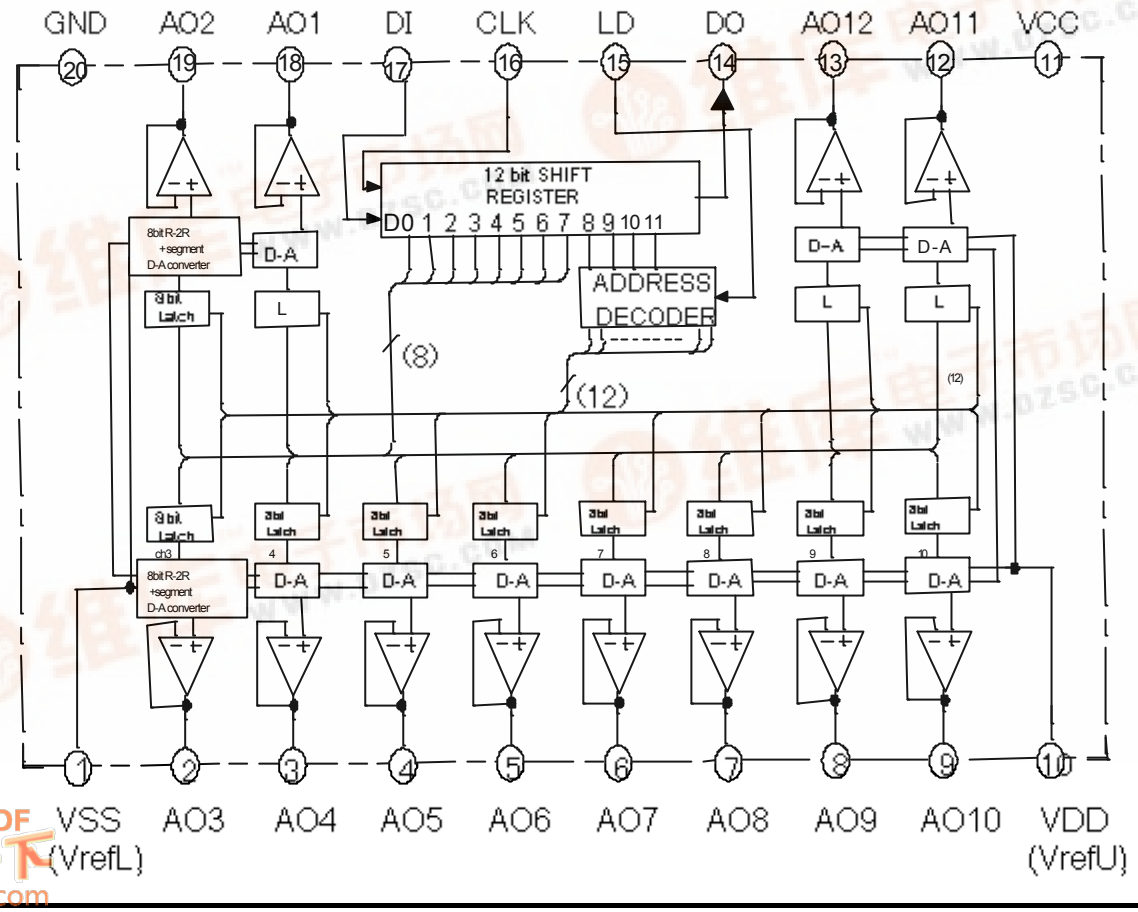
FEATURES

- 12 bit serial data input (3 wire serial data transfer method, DI, CLK, LD)
- Corresponds to TTL input for digital input (VINH ≥ 2V, VINL ≤ 0.8V)
- R-2R + segment method high performance 12 channel 8 bit D-A converters
- 12ch buffer operational amplifiers opperating in the whole voltage range from Vcc to GND
- Buffer operational amplifiers with high oscillation stability for capacitive load

APPLICATION

Adjustment or control of industrial or home-use electronic equipments such as VTR camera, VTR set, TV, and CRT display.

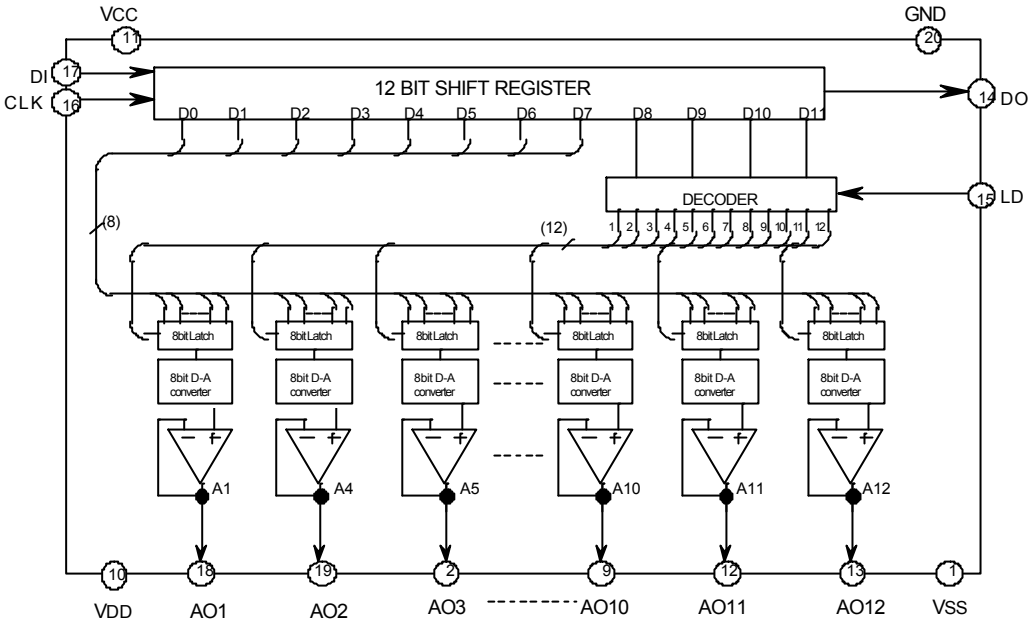
BLOCK DIAGRAM



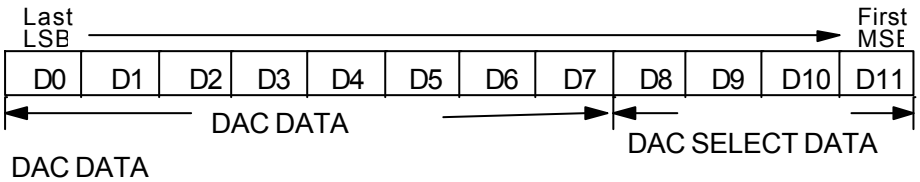
EXPLANATION OF TERMINALS

Pin No.	symbol	Function
17	DI	Serial data input terminal.12bit serial data is input to this terminal.
14	DO	Serial data output terminal.Serial data of 12bit shift register is output from this terminal.
16	CLK	Serial clock input terminal.Input signal from DI terminal is input to 12bit shift register upon the rise of shift clock.
15	LD	Data is loaded to register when 'H' is input to LD terminal.
18	AO1	8bit D-A converter output terminal. Built-in buffer amp.is connected to VCC. D-A converted voltage between VDD and VSS is output to each terminal.
19	AO2	
2	AO3	
3	AO4	
4	AO5	
5	AO6	
6	AO7	
7	AO8	
8	AO9	
9	AO10	
12	AO11	
13	AO12	
11	VCC	Power supply terminal.
20	GND	Digital and Analog common GND
10	VDD	D-A converter High level reference voltage input terminal.
1	VSS	D-A converter Low level reference voltage input terminal.

BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



DIGITAL DATA FORMAT



DAC DATA

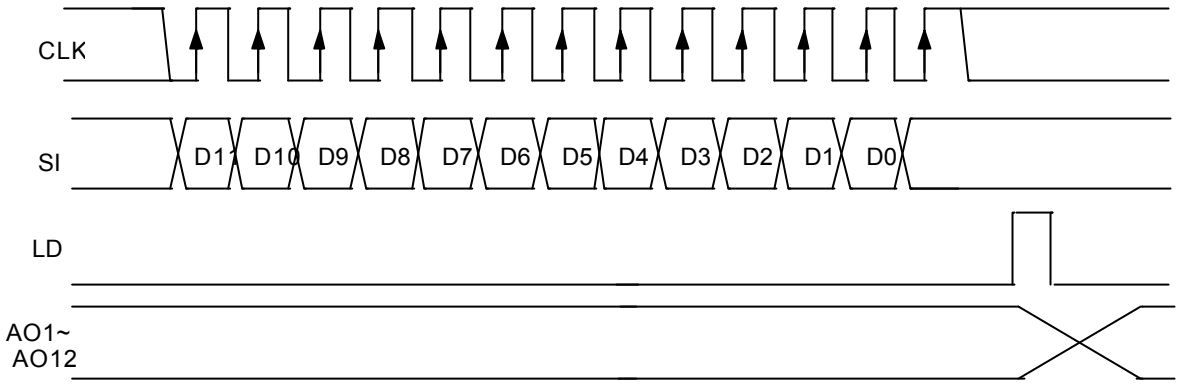
D0	D1	D2	D3	D4	D5	D6	D7	D-A output	
0	0	0	0	0	0	0	0	(VrefU-VrefL)/256 x 1+VrefL[V]	(1LSB)
1	0	0	0	0	0	0	0	(VrefU-VrefL)/256 x 2+VrefL[V]	(2LSB)
0	1	0	0	0	0	0	0	(VrefU-VrefL)/256 x 3+VrefL[V]	(3LSB)
1	1	0	0	0	0	1	0	(VrefU-VrefL)/256 x 4+VrefL[V]	(3LSB)
:	:	:	:	:	:	:	:	:	
0	1	1	1	1	1	1	1	(VrefU-VrefL)/256 x 255+VrefL[V]	(255LSB)
1	1	1	1	1	1	1	1	VrefU[V]	(256LSB)

VrefU=V_{DD}
VrefL=V_{SS}

DAC SELECT DATA

D8	D9	D10	D11	DAC SELECTION
0	0	0	0	Don't Care
0	0	0	1	A1select
0	0	1	0	A2select
0	0	1	1	A3select
0	1	0	0	A4select
0	1	0	1	A5select
0	1	1	0	A6select
0	1	1	1	A7select
1	0	0	0	A8select
1	0	0	1	A9select
1	0	1	0	A10select
1	0	1	1	A11select
1	1	0	0	A12select
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

TIMING CHART (model)



ABSOLUTE MAXMUM RATING

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		- 0.3 ~ 7.0	V
VDD	D-A converter High levelreference voltage		- 0.3 ~ 7.0	V
VIN	Digital input voltage		- 0.3 ~ VCC+0.3	V
Vout	Output voltage		- 0.3 ~ VCC+0.3	V
Pd	Power dissipation		150	mW
Topr	Operating temperature		- 20 ~ 85	°C
Tstg	Storage temperature		- 40 ~ 125	°C

ELECTRIC CHARACTERISTICS

<Digital part> (VCC, VrefU=5V ± 10% , VCC ≥ VrefU, GND, VrefL=0.0V, Ta=-20 ~ + 85°C unless otherwise specified.)

Symbol	Parameter	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vcc	Supply voltage		4.5	5.0	5.5	V
Icc	Supply current	CLK=1MHz Operation VCC=5V, IAO=0□A	——	1.5	3.5	mA
IILK	Input leak current	VIN=0 ~ VCC	-10	——	10	□A
VIL	Digital input Low voltage		——	——	0.8	V
VIH	Digital input High voltage		2.0	——	——	V
VOL	Digital output Low voltage	IOL= 2.5mA	——	——	0.4	V
VOH	Digital output High voltage	IOH= - 400□A	VCC-0.4	——	——	V

Note: Changes from M62352GP: Digital input voltage corresponds to TTL spec.

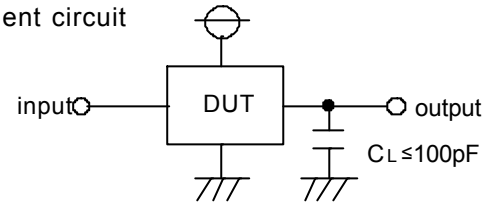
<Analog Part> (VCC, VrefU=5V ± 10% , VCC ≥ VrefU, GND, VrefL=0.0V, Ta=-20 ~ + 85°C unless otherwise specified.)

Symbol	Parameter	Conditions	Ratings			Unit
			MIN	TYP	MAX	
IrefU	Reference voltage pin current	VrefU=5V, VrefL=0V, IAO=0□A Data condition: at Maxmum Current	——	1.4	2.5	mA
VDD (VrefU)	D-A converter High level reference voltage range	The output does not necessarily be the Values within the reference voltage setting range. The output value is determined by the buffer amplifier output voltage range(VAO).	3.5		VCC	V
VSS (VrefL)	D-A converter Low level reference voltage range		GND		VCC -3.5	
VAO	Buffer amplifier output drive range	IAO = ± 100□A	0.1		VCC-0.1	V
		IAO = ± 500□A	0.2		VCC-0.2	
IAO	Buffer amplifier output drive range	Upper side saturation voltage=0.3V Lower side saturation voltage=0.2V	-1		1	mA
SDL	Differential nonlinearity	VrefU = 4.79V VrefL = 0.95V (15mV/LSB) VCC = 5.5V without load(IAO=+0□A)	-1.0		1.0	LSB
SL	Nonlinearity		-1.5		1.5	LSB
Szero	Zero code error		-2.0		2.0	LSB
SFULL	Full scale error		-2.0		2.0	LSB
Co	Output capacitative load				0.1	□F
Ro				5		ohm

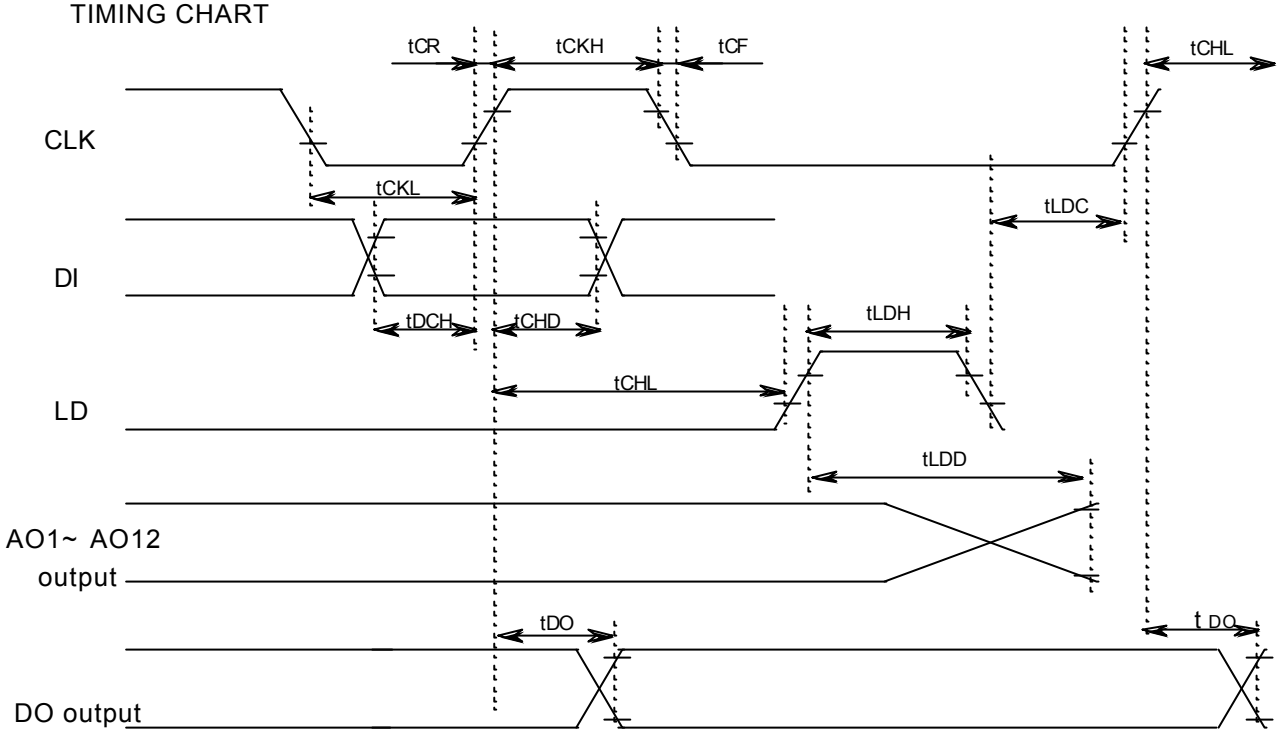
<AC characteristics> (VCC, VrefU=5V ± 10% , VCC ≥ VrefU, GND, VrefL=0.0V, Ta=-20 ~ +85°C unless otherwise specified.)

Symbol	Parameter	Conditions	Ratings			Unit
			MIN	TYP	MAX	
tCKL	Clock "L" puise width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR tCF	Clock rise time Clock fall time				200	ns
tDCH	Data setup time		30			ns
tCHD	Data hold time		60			ns
tCHL	LD setup time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" hold time		100			ns
tDO	Data output delay time	CL≤ 100pF	70		350	ns
tLDD	D-A output settling time	CL≤ 100pF,VAO:0.5 ⇄ 4.5V The time until the output becomes the final value of 1/2 LSB			300	□s

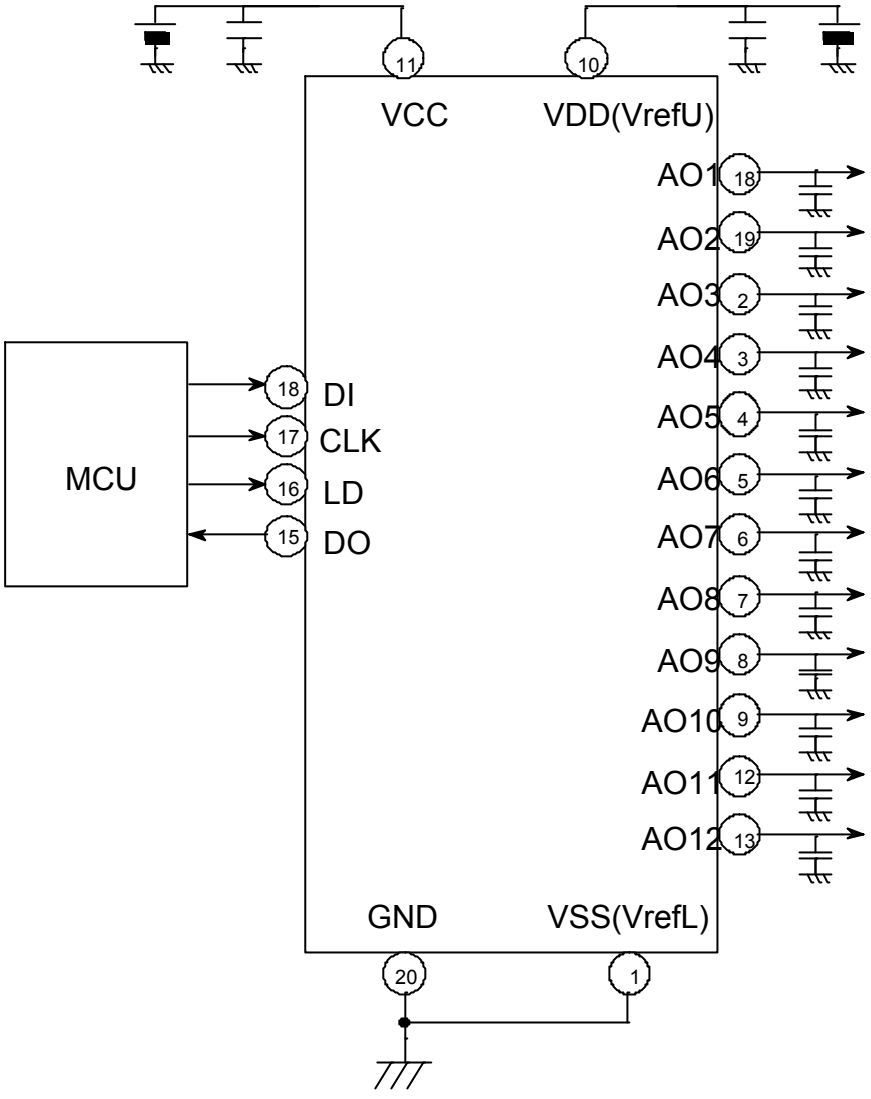
Measurement circuit



TIMING CHART



TYPICAL APPLICATION



Note:

M62352AGP has 3 terminals(VDD, VCC, and VSS) to which constant voltage is to be applied. Ripple voltage or spike noise to these terminals may worsen converting precision or cause erroneous operations. So be sure to use this device by putting cacpacitor between each terminal and GND to get D-A conversion operation stabilized.

Output buffer amplifiers have high oscillation stability against capacitive load. This means that jitters by wirings around output terminals or capcitor between output and GND(0.1uF max.) do not cause any problems with DAC operations.

Connect capacitor(0.1uF or around) between output and GND for protection from spark discharge when this device is used under such high electric field as that for instance of instruments with cathode ray tube.