



查询M655供应商

Integrated Circuit Systems

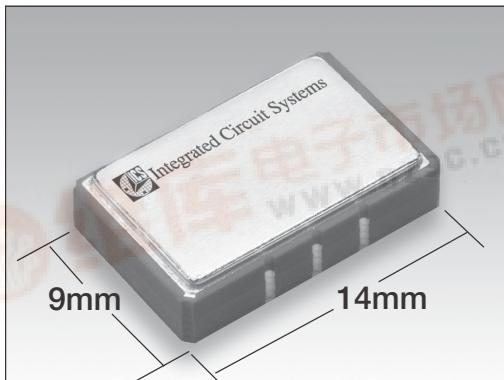
捷多邦，专业PCB打样工厂，24小时加急出货

M655 Series

Performance Specifications

M655 Series

Voltage Controlled SAW Oscillators



FEATURES

- Output Frequencies at 155MHz to 900MHz
- Low Phase Jitter, 0.5psec (rms) typical
- 3.3 Volt Supply Operation
- Complementary Outputs
- Output Disable Feature
- LCC Surface Mount Package (9 x 14mm)

DESCRIPTION

The M655 Series of Voltage Controlled SAW Oscillators is a low cost solution for many Telecom applications. An internal SAW filter provides jitter performance of less than 0.5psec (rms).

This device is specified for an operating temperature range of -40°C to +85°C. A disable feature forces the output into a static condition by applying a logic "0" to the clock enable input. The oscillator is housed in a hermetically-sealed, leadless surface mount package.

The M655 Series of VCOs is available over an output frequency range of 155MHz to 900MHz. The device is most suited for phase-locked loop applications as well as clock and data recovery circuits.

APPLICATION

- Clock Smoothing for OC192/OC48/OC12/OC3
- Clock Smoothing for STS96/STS48/STS12/STS3/STS1
- Frequency Translation
- Clock and Data Retiming

ABSOLUTE MAX RATINGS

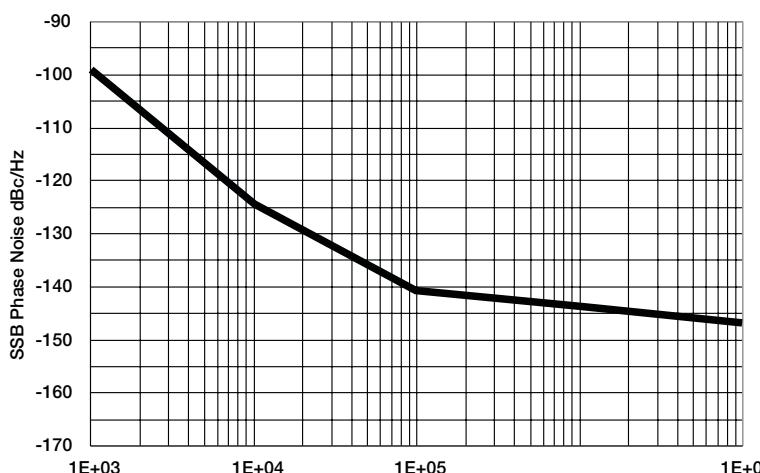
Operating Temp. Range (Case): -40°C to +85°C
Storage Temp. Range (Ambient): -55°C to +125°C
Control Voltage Range: 0 to Vcc
Output Current: 20 mA
Power Supply Voltage (Vcc): 0 to +3.6 Vdc

SPECIFICATIONS

Specifications @ $V_{cc} = +3.3$ Volts, $V_{ee} = 0$ Volts, and $T_a = +25^\circ C$ unless otherwise specified

PARAMETER		Min	Typ	Max	Units
Output Frequency		155		900	MHz
Absolute Pull Range		± 50			ppm
Frequency Stability (-40°C to 85°C)			+25/-150		ppm
Duty Cycle		45		55	%
Spurious Suppression-50		-60			dBc
Linearity			± 6		%
Logic Levels	V_{ol}^1	$V_{cc} - 1.95$		$V_{cc} - 1.63$	Volts
	V_{oh}^2	$V_{cc} - 0.98$		$V_{cc} - 0.75$	Volts
Input Control Voltage (V_c) Range		0		V_{cc}	Volts
VCO Gain			200		ppm/V
V_c Input Impedance		8		12	$K\Omega$
V_c Modulation BW			500		kHz
Clock/Output Enable (Pin 2)		2.0		$V_{cc} + 0.3$	Volts
Clock/Output Disable (Pin 2)		-0.3		0.8	Volts
Output Rise Time			250	400	psec
Output Fall Time			250	400	psec
Jitter @ 155.520MHz offset from carrier 12kHz to 20MHz			0.230		psec rms
Jitter @ 622.080MHz offset from carrier 12kHz to 80MHz			0.458		psec rms
Phase Noise (offset from carrier)					
	100Hz		-65		dBc/Hz
	1kHz		-95		dBc/Hz
	10kHz		-120		dBc/Hz
	100kHz		-140		dBc/Hz
Operating Temperature		-40	25	+85	°C
Supply Current	I_{cc}		80	95	mA
Supply Voltage	V_{cc}	3.2	3.3	3.4	V

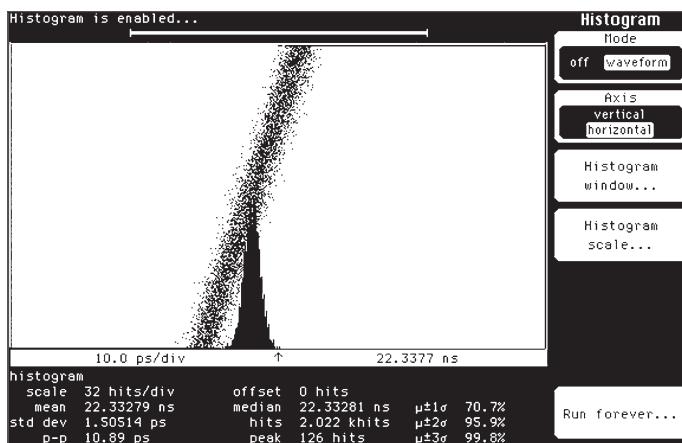
Notes: 1. Output levels are standard 10K ECL and are fully 100K ECL compatible.
 2. Transition times are measured from 20% to 80% of a full 10K ECL level swing.

Phase Noise


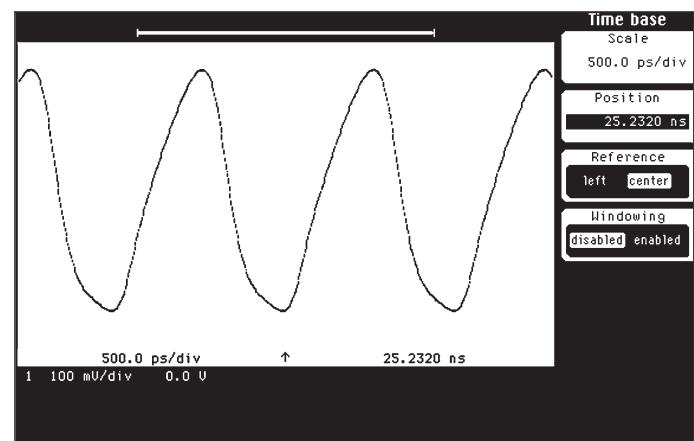


SPECIFICATIONS

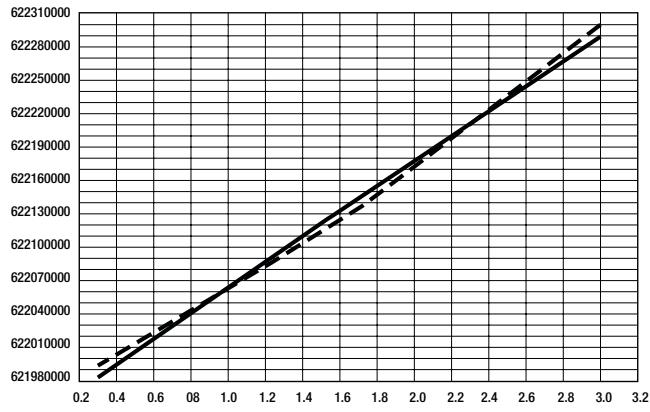
Jitter



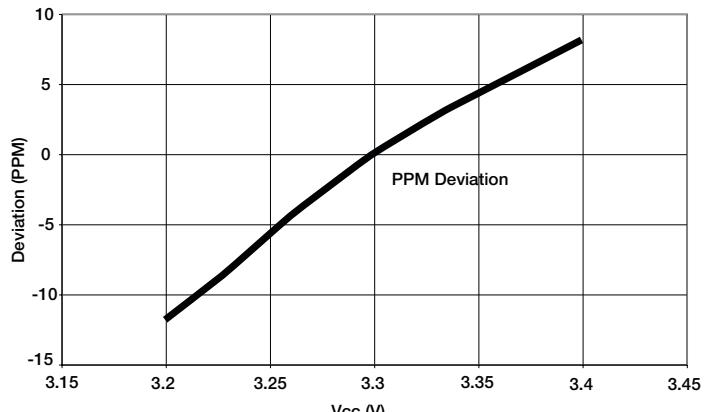
Output



Typical Linearity

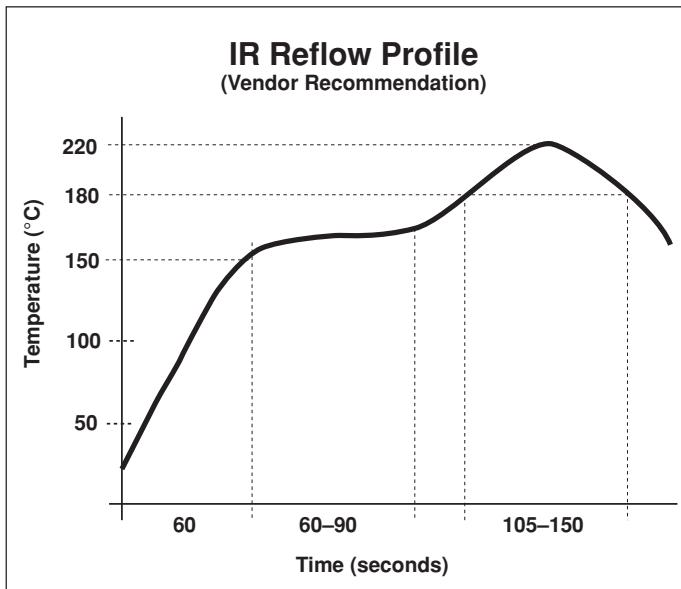


Typical Frequency Pushing





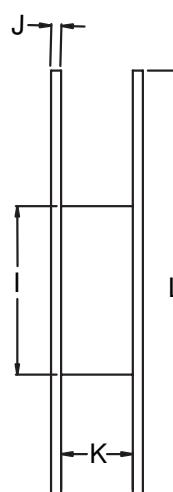
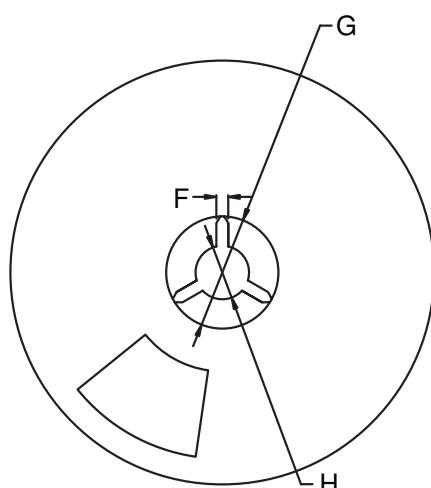
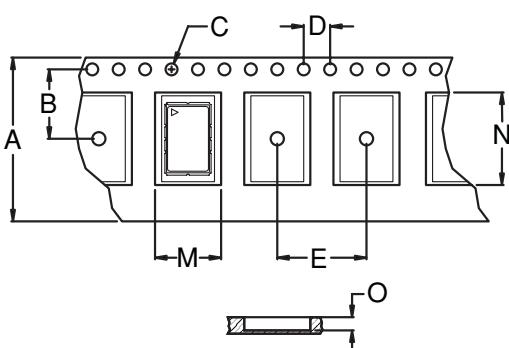
IR REFLOW PROFILE



Micro Networks has subjected their VCSO component to various reflow profiles and test conditions for optimum substrate mounting performance. The conditions suggested here are recommended temperature settings for the VCSO device during the reflow processes. The best case condition for the device is a slow ramp up to prevent thermal shock before reaching reflow temperatures of Sn/Pb flux activated solder with a melting point of 183 degree Celsius. The M655 device should not see temperatures above 183 degrees Celsius for an extended periods beyond 60 seconds. Maximum peak temperature for the device should not exceed 220 degrees Celsius for longer than 20 seconds.

Micro Networks has designed the M655 device as a sealed unit. The package is 100% tested for seal defects. Aqueous, solvent, or other wash type cleaning methods is acceptable for this device.

TAPE & REEL



TAPE & REEL DIMENSIONS

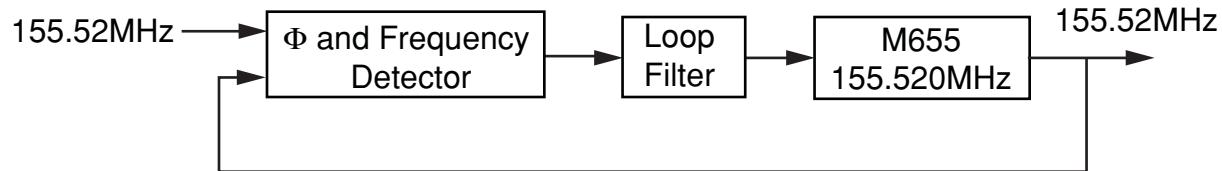
TAPE	MM	REEL	MM
A	24	F	1.78
B	11.5	G	21
C	1.5	H	13
D	4	I	100
E	12	J	5
M	9.2	K	25
N	14.5	L	330
O	3.7		

No. per Reel: 300 Max

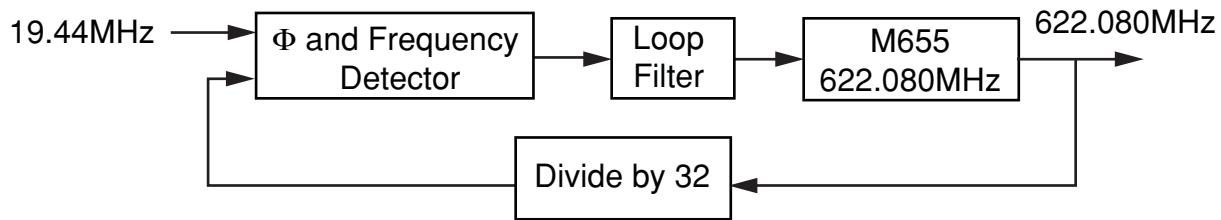


APPLICATIONS

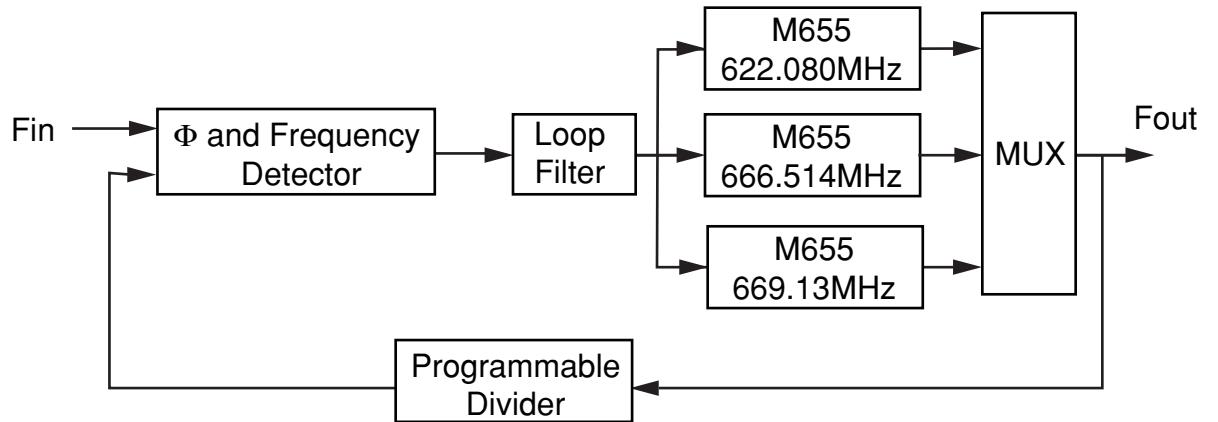
Jitter Attenuator



Frequency Translator

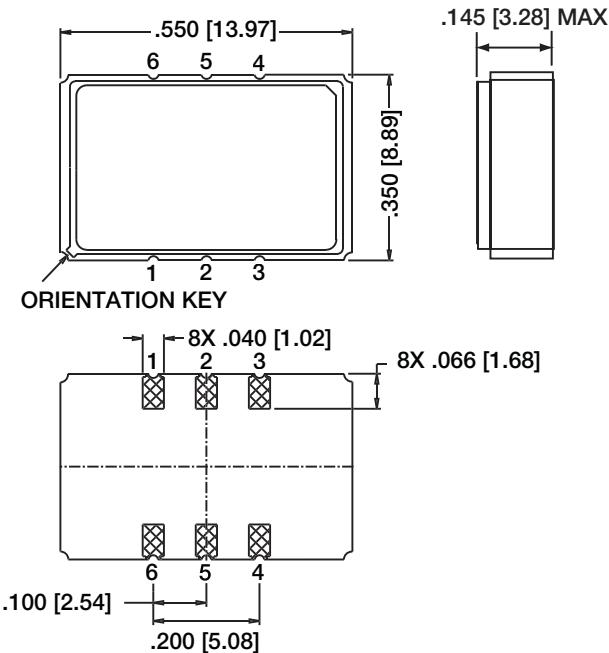


Multi-rate FEC Clock Generator





MECHANICAL DIMENSIONS & PIN CONFIGURATION



Pin No.	Function
1	V_t
2	CE
3	GND
4	C_{out}
5	nC_{out}
6	V_{cc}

ORDERING INFORMATION

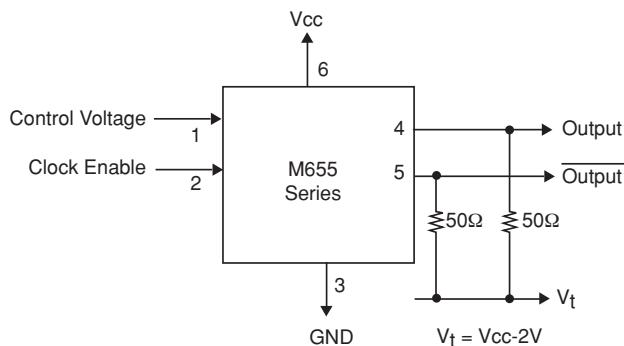
Part Number **M655P 622.0800**

P for PECL Operation

Specify frequency in MHz xxx.xxxx
(eg. 155.5200MHz, 311.0400MHz,
622.0800MHz, 666.5140MHz)

Absolute Pull Range
Blank = ± 50 ppm
 ± 100 ppm available for certain frequencies.
Consult factory.

BLOCK DIAGRAM



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

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