M66281FP

5120 x 8-BIT x 2 LINE MEMORY

DESCRIPTION

The M66281FP is high speed line memory that uses high performance silicon gate CMOS process technology and adopts the FIFO (First In First Out) structure consisting of 5120 words x 8 bits x 2.

Since memory is available to simultaneously output 1 line delay and 2 line delay data, the M66281FP is optimal for the compensation of data of multiple lines.

FEATURES

- Memory configuration 5120 words x 8 bits x 2 (dynamic memory)
- High speed cycle 25 ns (Min.)
- High speed access 18 ns (Max.)
- Output hold 3 ns (Min.)
- Reading and writing operations can be completely carried out independently and asynchronously.
- Variable length delay bit
- Input/output TTL direct connection allowable
- Output 3 states
- Q00 – Q07 1 line delay
- Q10 – Q17 2 line delay

APPLICATION

- Digital copying machine, laser beam printer, high speed facsimile, etc.

FUNCTION

When write enable input WEB is set to "L", the contents of data inputs D0 to D7 are written into memory only for 1 line delay data in synchronization with a rising edge of write clock input WCK to perform writing operation. When this is the case, the write address counter of memory only for 1 line delay data is incremented simultaneously.

When WEB is set to "H", the writing operation is inhibited and the write address counter of memory only for 1 line delay data stops.

When write reset input WRESB is set to "L", the write address counter of memory only for 1 line delay data is initialized.

When read enable input REB is set to "L", the contents of memory only for 1 line delay data are output to data outputs Q00 to Q07 and the contents of memory only for 2 line delay data are output to Q10 to Q17 in synchronization with a rising edge of read clock input RCK to perform reading operation.

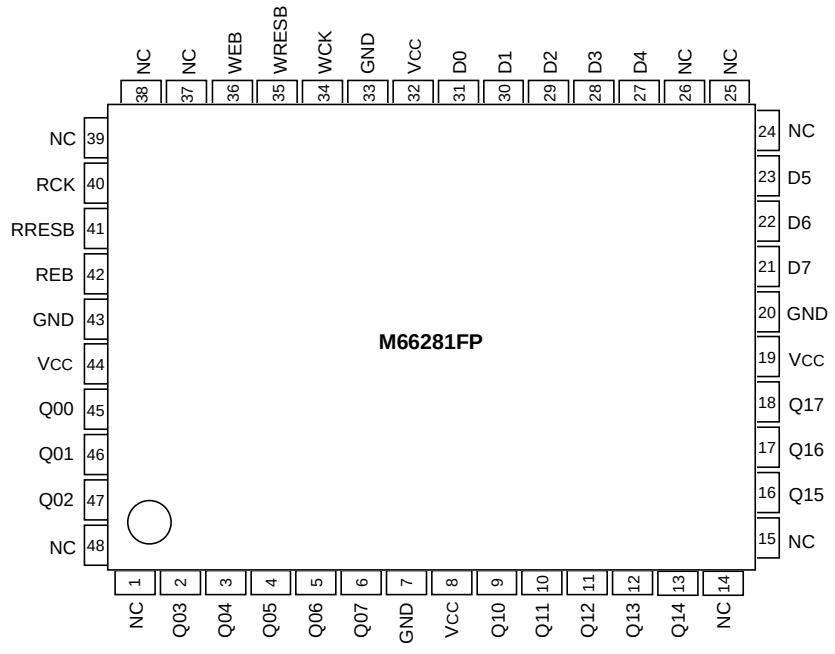
When this is the case, the read address counters of memory only for 1 line delay data and memory only for 2 line delay data are incremented simultaneously.

In addition, data of Q00 to Q07 is written into memory only for 2 line delay data in synchronization with a rising edge of RCK. When this is the case, the write address counter of memory only for 2 line delay data is then incremented.

When REB is set to "H", operation for reading data from memory only for 1 line delay and from memory only for 2 line delay data is inhibited and the read address counter of each memory stops. Outputs Q00 to Q07 and Q10 to Q17 are placed in a high impedance state. In addition, the write address counter of memory only for 2 line delay data then stops.

When read reset input RRESB is set to "L", the read address counters of memory only for 1 line delay data as well as the write address counter and read address counter of memory only for 2 line delay data are then initialized.

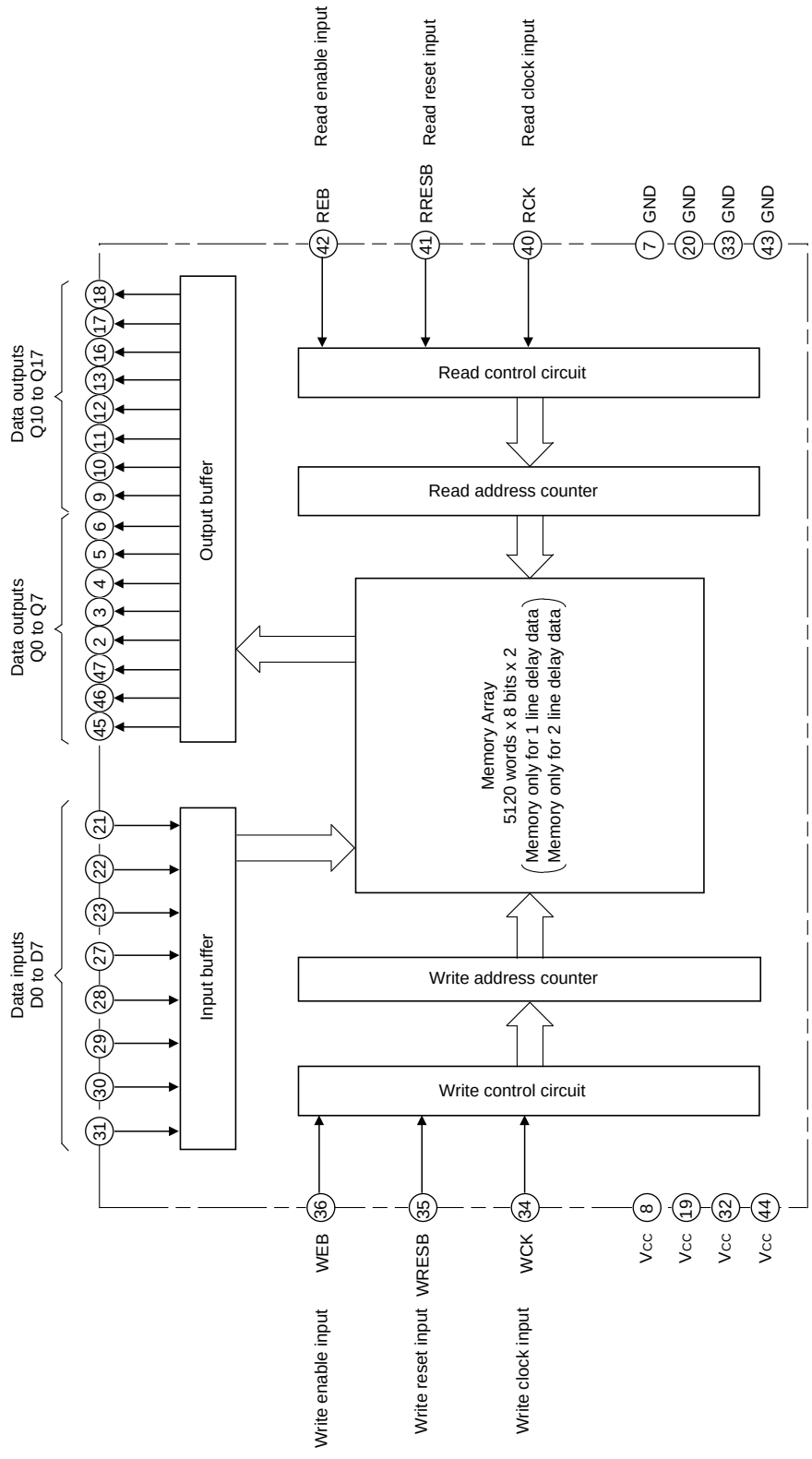
PIN CONFIGURATION (TOP VIEW)



Outline 48P6S-A(QFP)

NC : No connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=0 – 70 °C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	Value based on the GND pin	-0.3 – +4.6	V
V_I	Input voltage		-0.3 – V_{CC}+0.3	V
V_O	Output voltage		-0.3 – V_{CC}+0.3	V
Pd	Power dispersion	Note	540	mW
Tstg	Storage temperature		-55 – 150	°C

Note : Ta=0 – 63˚C. Ta > 63˚C are derated at -9mW/˚C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc	Supply voltage	2.7	3.15	3.6	V
GND	Supply voltage		0		V
Topr	Operating temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (Ta=0 – 70 °C, Vcc=2.7 – 3.6V, GND=0V unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	I_{OH} = -4mA		V_{CC}-0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA				0.4	V
I_{IH}	High-level input current	$V_I = V_{CC}$	WEB, WRESB, WCK, REB, RRESB, RCK, D0 – D7			1.0	μA
I_{IL}	Low-level input current	V_I = GND	WEB, WRESB, WCK, REB, RRESB, RCK, D0 – D7			-1.0	μA
I_{OZH}	Off-state high-level output current	$V_O = V_{CC}$				5.0	μA
I_{OZL}	Off-state low-level output current	V_O = GND				-5.0	μA
I_{CC}	Average supply current during operation	$V_I = V_{CC}$, GND, output open t_{WCK}, t_{RCK} = 25ns				150	mA
C_I	Input capacitance	f = 1MHz				10	pF
C_O	Off-time output capacitance	f = 1MHz				15	pF

SWITCHING CHARACTERISTICS (Ta=0 – 70 °C, Vcc=2.7 – 3.6V, GND=0V unless otherwise noted)

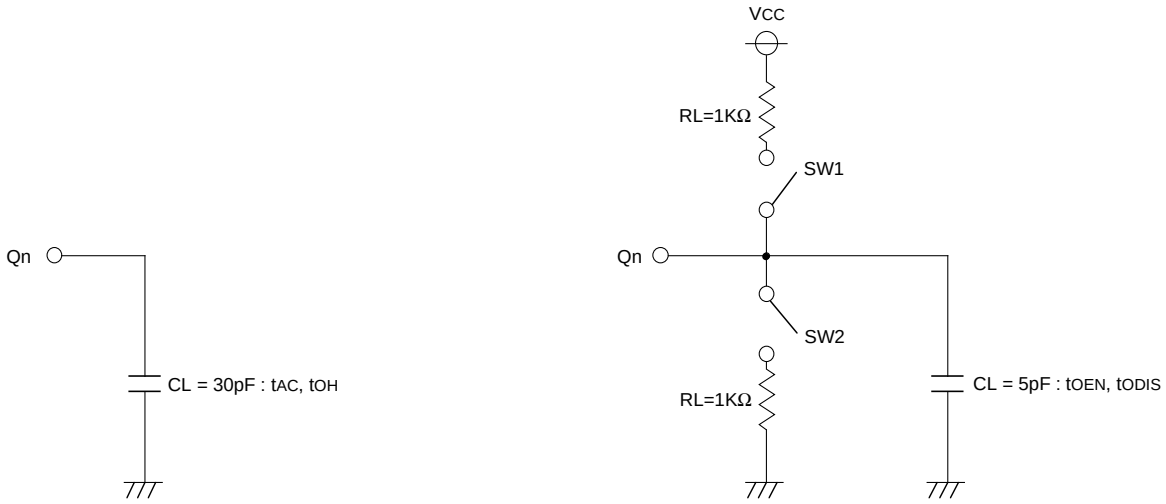
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AC}	Access time			18	ns
t_{OH}	Output hold time	3			ns
t_{OEN}	Output enable time	3		18	ns
t_{ODIS}	Output disable time	3		18	ns

TIMING REQUIREMENTS (Ta=0 – 70 °C, Vcc=2.7 – 3.6V, GND=0V unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WCK}	Write clock (WCK) cycle	25			ns
t_{WCKH}	Write clock (WCK) "H" pulse width	11			ns
t_{WCKL}	Write clock (WCK) "L" pulse width	11			ns
t_{RCK}	Read clock (RCK) cycle	25			ns
t_{RCKH}	Read clock (RCK) "H" pulse width	11			ns
t_{RCKL}	Read clock (RCK) "L" pulse width	11			ns
t_{DS}	Input data set up time for WCK	7			ns
t_{DH}	Input data hold time for WCK	3			ns
t_{RESS}	Reset set up time for WCK/RCK	7			ns
t_{RESH}	Reset hold time for WCK/RCK	3			ns
t_{NRESS}	Reset non-selection set up time for WCK/RCK	7			ns
t_{NRESH}	Reset non-selection hold time for WCK/RCK	3			ns
t_{WES}	WEB set up time for WCK	7			ns
t_{WEH}	WEB hold time for WCK	3			ns
t_{NWES}	WEB non-selection set up time for WCK	7			ns
t_{NWEH}	WEB non-selection hold time for WCK	3			ns
t_{RES}	REB set up time for RCK	7			ns
t_{REH}	REB hold time for RCK	3			ns
t_{NRES}	REB non-selection set up time for RCK	7			ns
t_{NREH}	REB non-selection hold time for RCK	3			ns
t_r, t_f	Input pulse up/down time			20	ns
t_H	Data hold time (Note 1)			20	ms

Note 1: For 1 line access, the following conditions must be satisfied:
WEB high-level period ≤ 20 ms - 5120 • t_{WCK} - WRESB low-level period
REB high-level period ≤ 20 ms - 5120 • t_{RCK} - RRESB low-level period
2: Perform reset operation after turning on power supply.

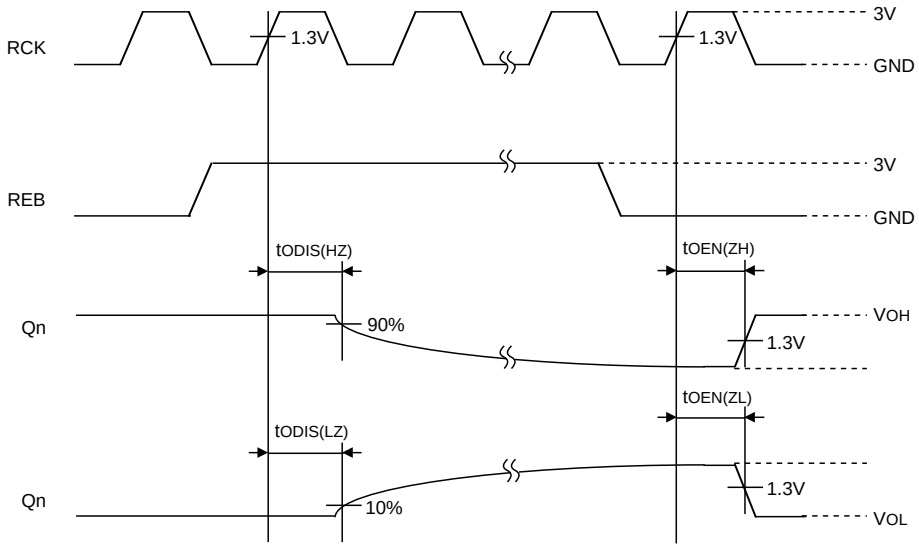
SWITCHING CHARACTERISTICS MEASUREMENT CIRCUIT



Input pulse level : 0 – 3V
Input pulse up/down time : 3 ns
Judging voltage Input : 1.3V
Output : 1.3V(However, tODIS(LZ) is judged with 10% of the output amplitude, while tODIS(HZ) is judged with 90% of the output amplitude.)
Load capacitance CL includes the floating capacity of connected lines and input capacitance of probe.

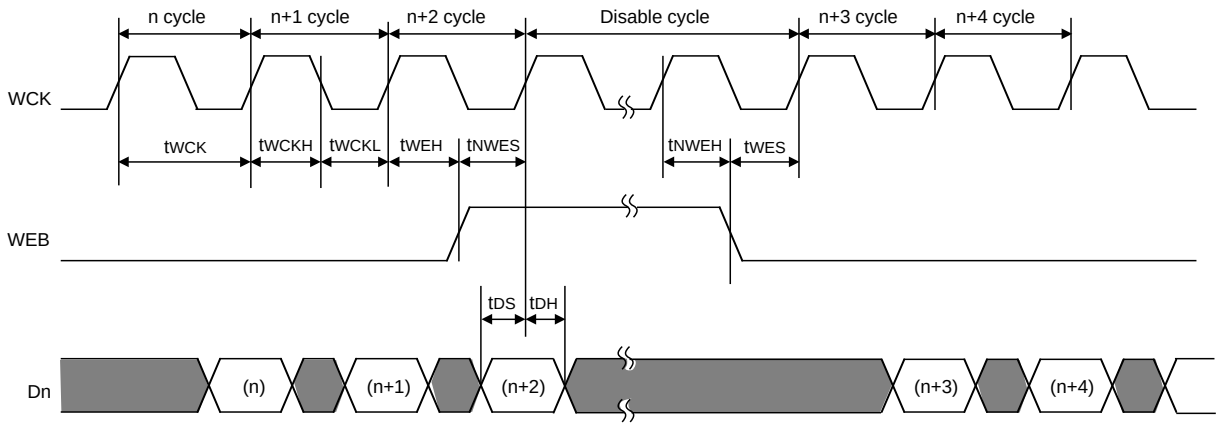
Item	SW1	SW2
tODIS(LZ)	Close	Open
tODIS(HZ)	Open	Close
tOEN(ZL)	Close	Open
tOEN(ZH)	Open	Close

tODIS and tOEN measurement condition



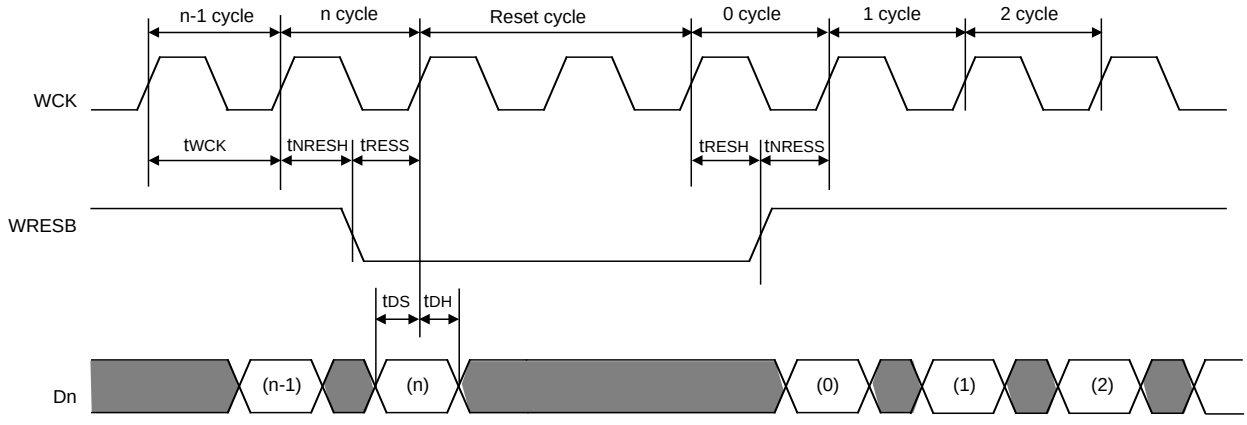
OPERATION TIMING

- Write cycle



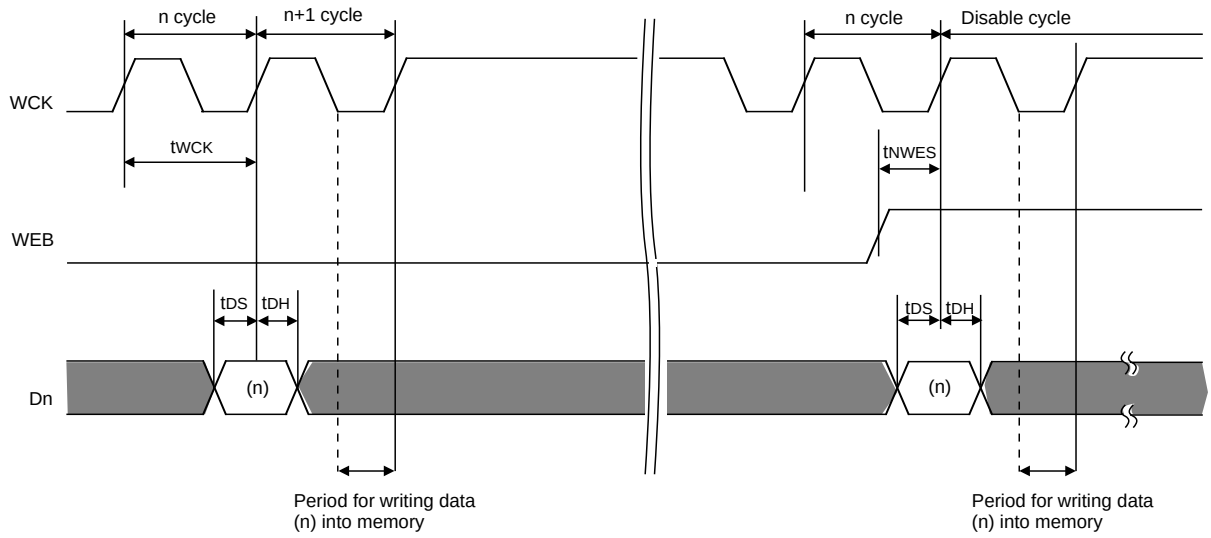
WRESB = "H"

- Write reset cycle



WEB = "L"

• Matters that needs attetion when WCK stops



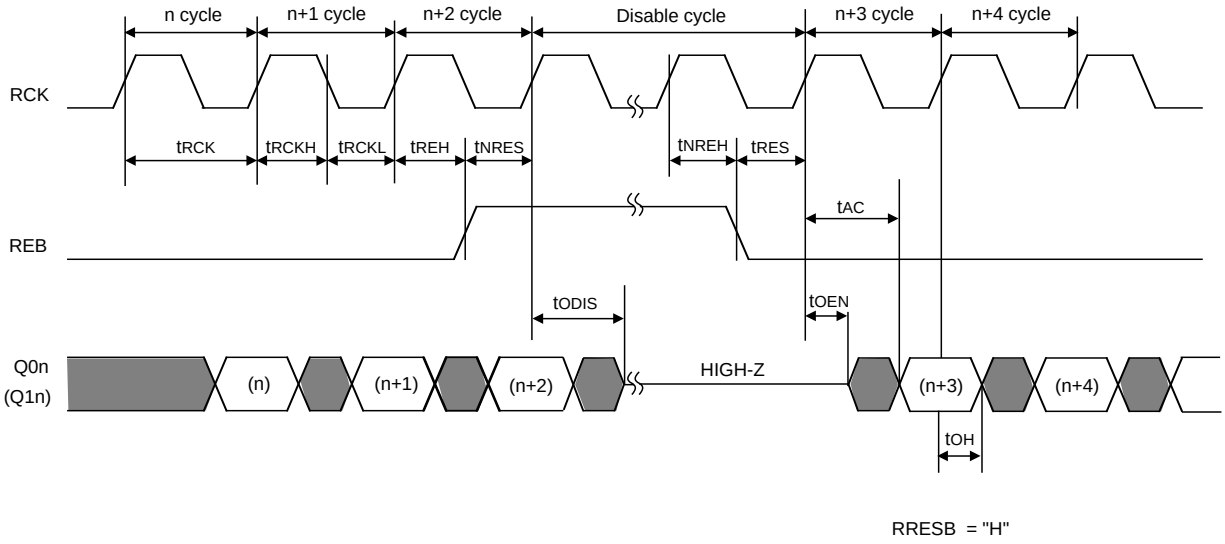
WRESB = "H"

Input data of n cycle is read at the rising edge after WCK of n cycle and writing operation starts in the WCK low-level period of n+1 cycle. The writing operation is complete at the falling edge after n+1 cycle.

To stop reading write data at n cycle, enter WCK before the rising edge after n+1 cycle.

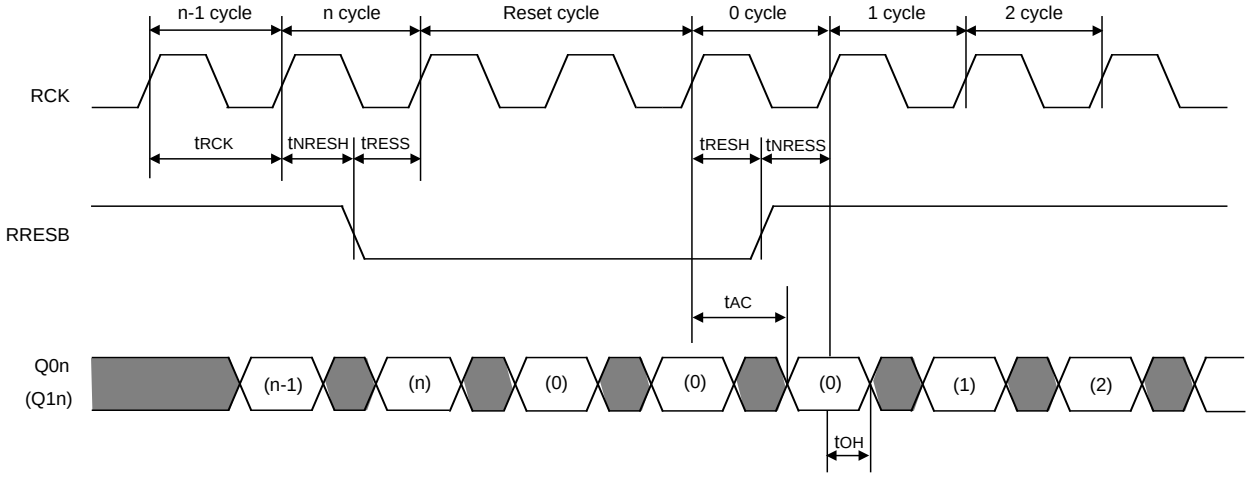
When the cycle next to n cycle is a disable cycle, WCK for a cycle requires to be entered after the disable cycle as well.

• Read cycle



RRESB = "H"

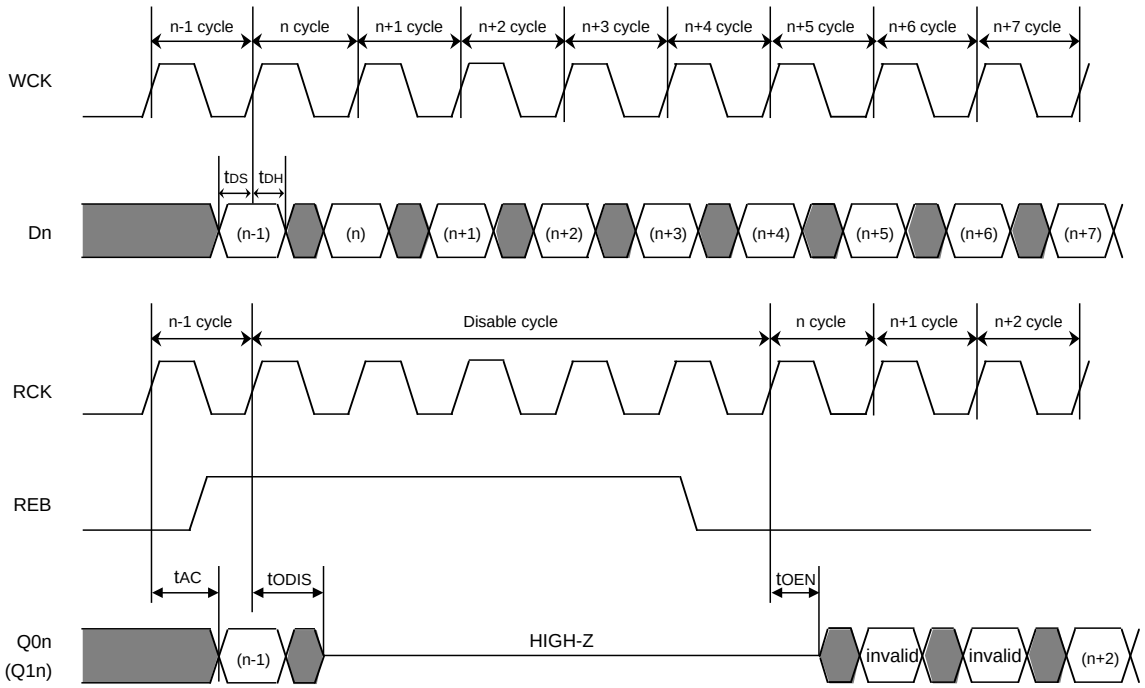
• Read reset cycle



REB = "L"

• Notes on reading of written data in read disable

When writing operation is performed at n cycle and n+1 cycle on the writing side in the read disable period after n-1 cycle on the reading side, output at n cycle and n+1 cycle after read enable is invalid. For output at n+2 cycle and after, however, data written in the read disable period is to be output.

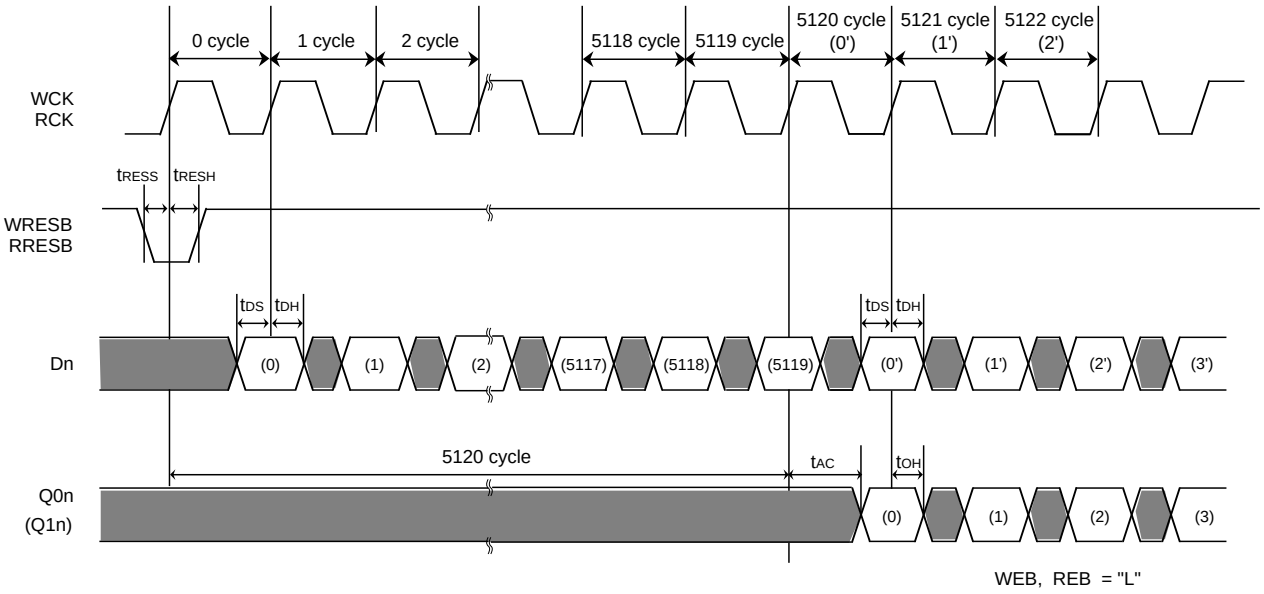


WEB = "L"
WRESB = "H"
RRESB = "H"

VARIABLE LENGTH DELAY BIT

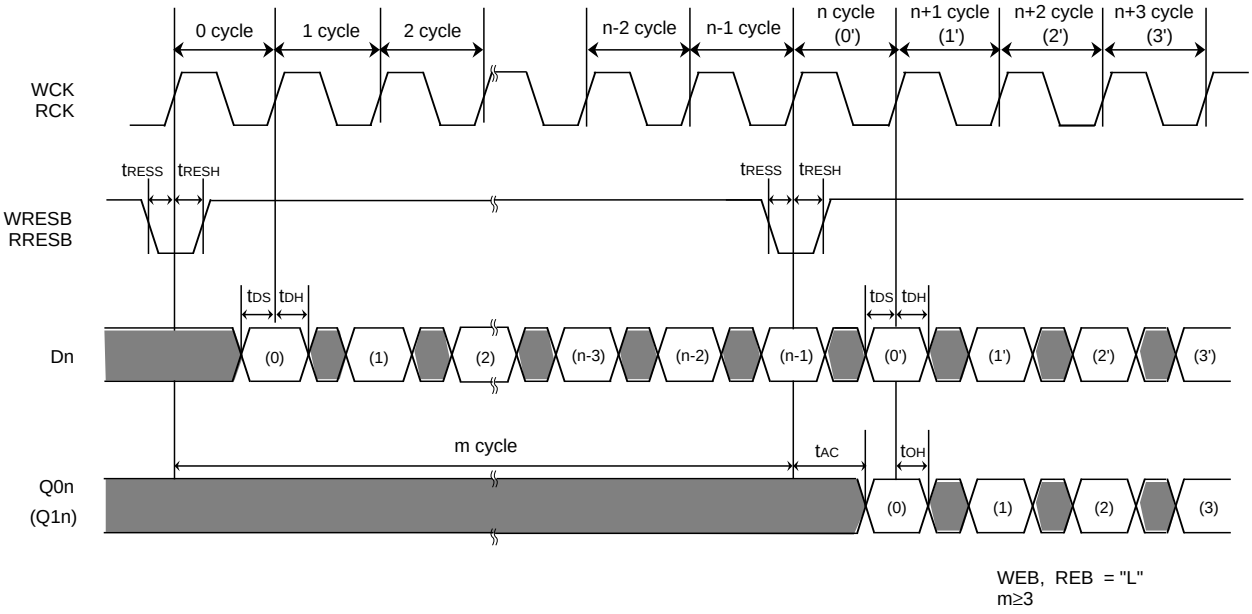
- 1 line (5120 bits) delay

  Input data can be written at the rising edge of WCK after write cycle and output data is read at the rising edge of RCK before read cycle to easily make 1 line delay.



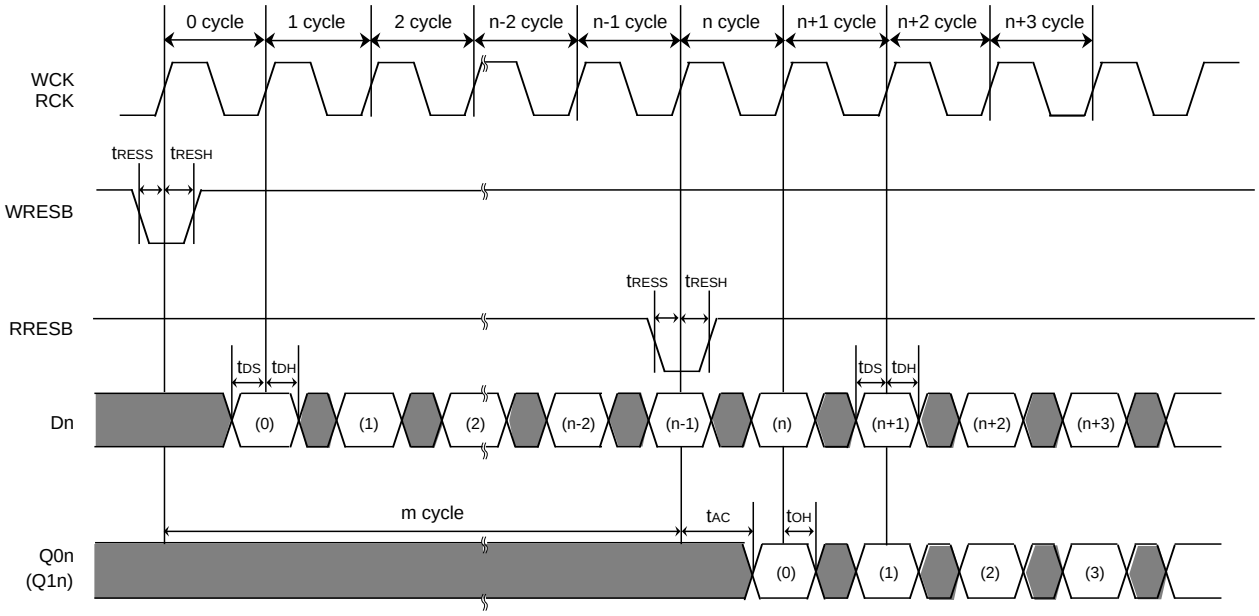
- n-bit delay bit

  (Reset at cycles according to the delay length)



• n-bit delay 2

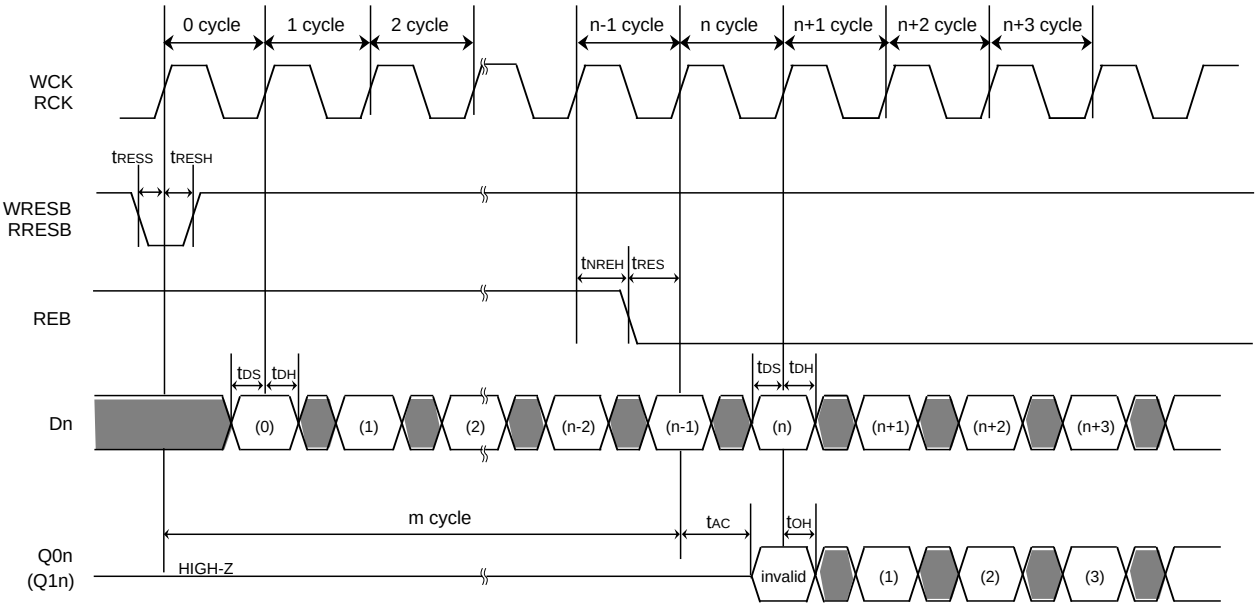
(Slides input timings of WRESB and RRESB at cycles according to the delay length.)



WEB, REB = "L"
m≥3

• n-bit delay 3

(Slides address by disabling REB in the period according to the delay length.)

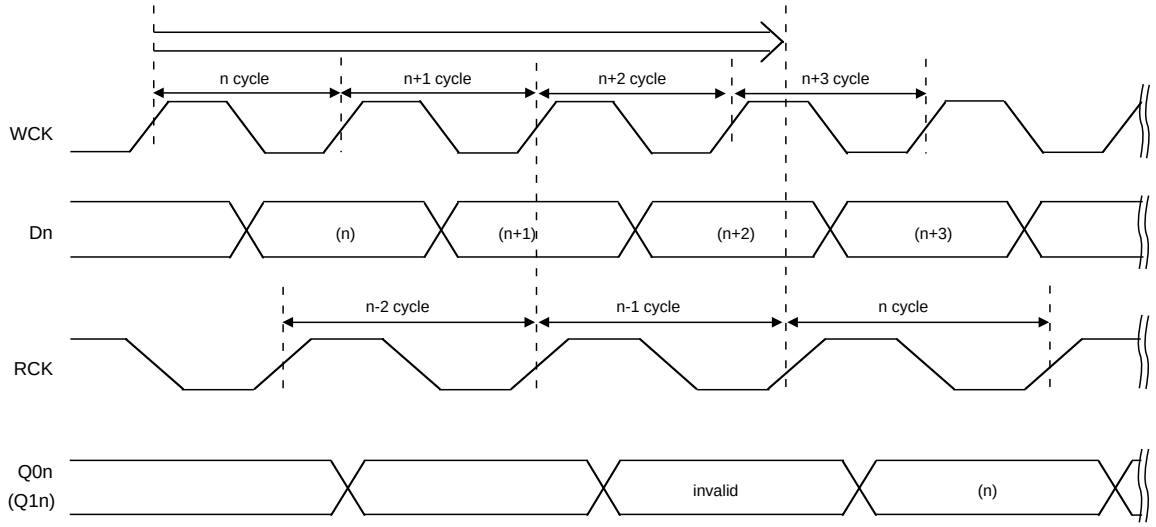


WEB = "L"
m≥3

• Reading shortest n-cycle write data "n"

(Reading side n-2 cycle ends after the end of writing side n+1 cycle.)

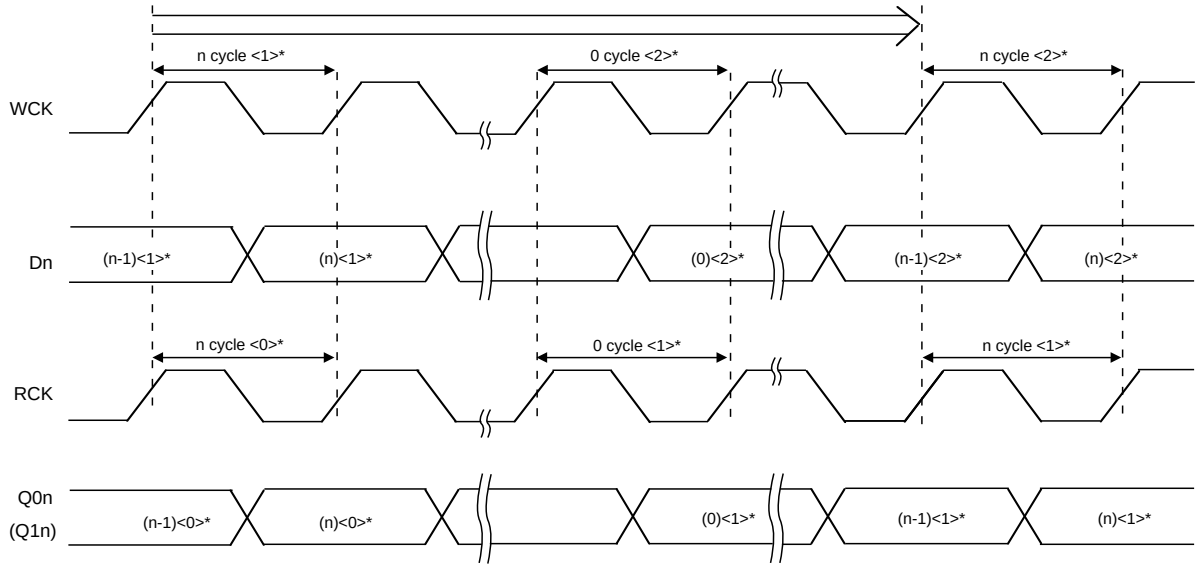
When the reading side n-2 cycle ends before the end of the writing side n+1 cycle, output Qn of n cycle is made invalid.
In the following diagram, end of reading side n-2 cycle and end of writing side n+1 cycle overlap each other. This example can read n cycle data in the shortest time. When this is the case, reading operation at n-1 cycle is invalid.



• Reading longest n-cycle write data "n": 1 line delay

(When writing side n-cycle <2> starts, reading side n cycle <1> then starts.)

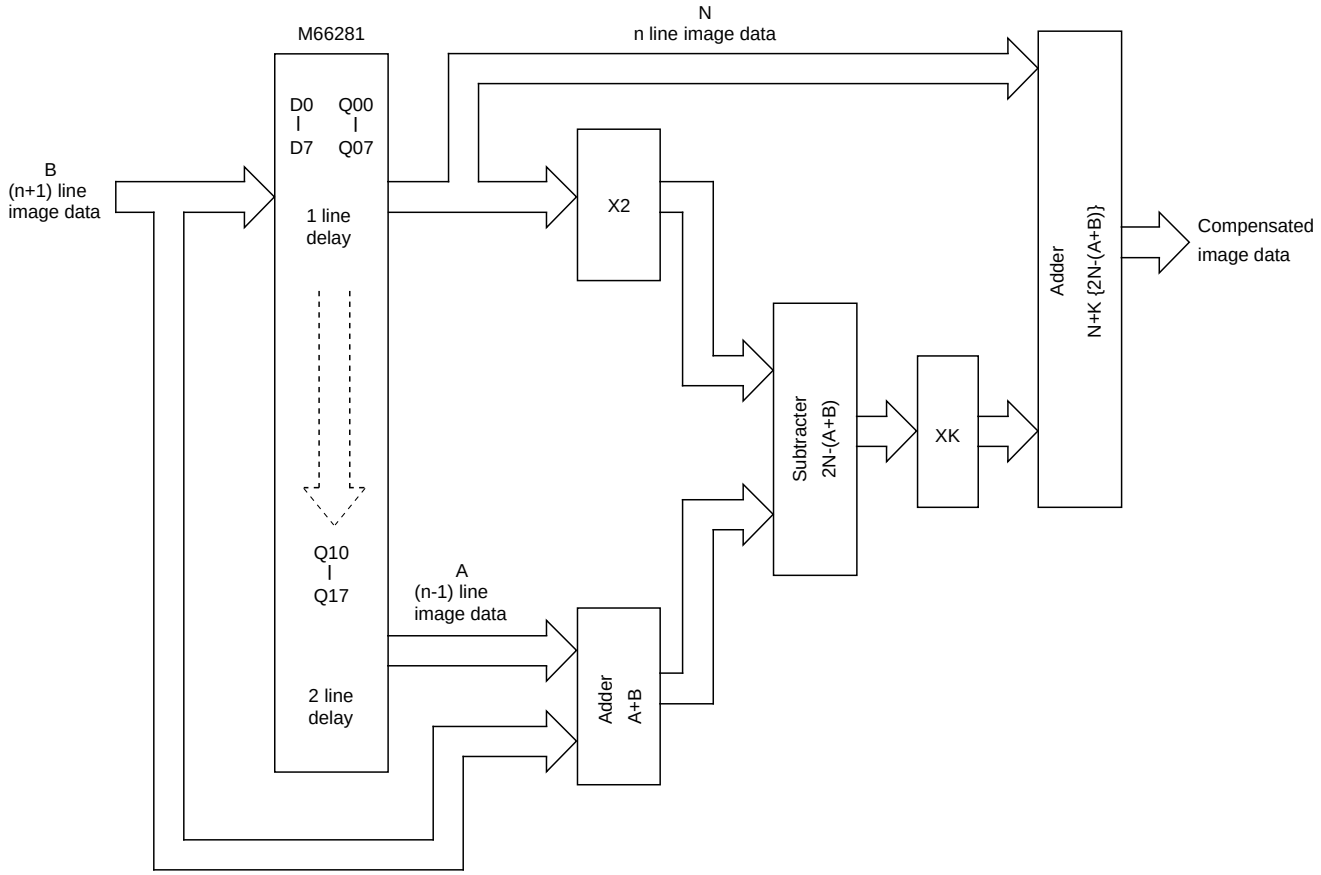
Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1> and the start of writing side n cycle <2>* overlap each other.

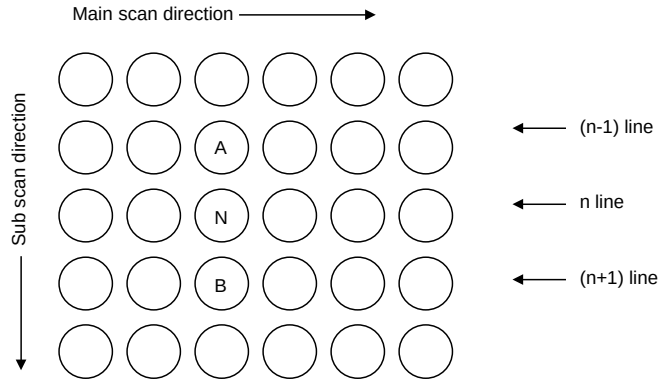


<0>*, <1>* and <2>* indicate value of lines.

APPLICATION EXAMPLE

Sub Scan Resolution Compensation Circuit with Laplacean Filter





N'=N+K { (N-A) + (N-B) }

=N+K { (2N - (A+B) }

K: Laplacean coefficient