M66287FP

262144-word x 8-bit x 3-FIELD MEMORY

DESCRIPTION

The M66287FP is a high-speed field memory with three FIFO (First In First Out) memories of 262144-word x 8-bit configuration (2M bits) which uses high-performance silicon gate CMOS process technology. One of three FIFO memories consists of two FIFO memories of 262144-word x 4-bit (1M bits). Five types of operation can be performed through the following mode settings:

Mode1 : 3-system delay data output by 3-system individual input of 256K-word x 8-bit FIFO
Mode2 : Simultaneous output of 1 to 3-line delay data by 1-system input of 256K-word x 8-bit FIFO
Mode3 : Simultaneous output of 1 to 2-line delay data by 1-system input of 256K-word x 8-bit FIFO and,1-system delay data output by 1-system input of 256K-word x 8-bit FIFO
Mode4 : 2-system delay data output by 2-system individual input of 256K-word x 12-bit FIFO
Mode5 : Simultaneous output of 1 to 2-line delay data by 1-system input of 256K-word x 12-bit FIFO

The above-mentioned function is most suitable for image data correction across multiple fields. Because three pieces of 2M-bit FIFO are contained in one chip, a low power consumption of a set can be realized.

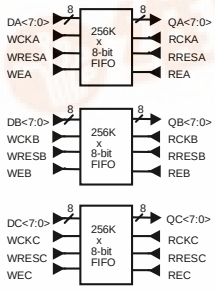
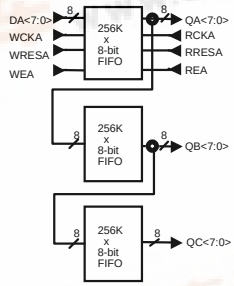
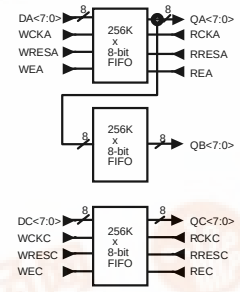
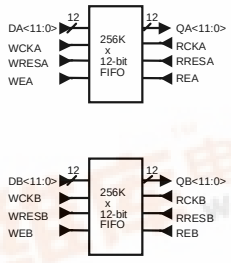
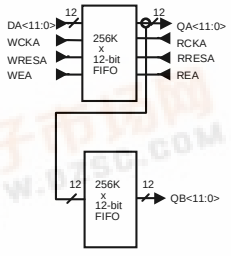
FEATURES

- Memory configuration — The total memory capacity is 6M bits (static memory).
  The following two types of memory configurations can be selected.
  262144-word x 8-bit x 3-line configuration
  262144-word x 12-bit x 2-line configuration
- High - speed cycle — 16.6 ns (Min.)
- High - speed access — 13.0 ns (Max.)
- Output hold — 2.0 ns (Min.)
- Supply voltage — Internal = 1.8 V ± 0.18 V
  I/O = 3.3 V ± 0.3 V
- Variable length delay bit
- Five modes can be selected
- Write and read function can be operated completely independently and asynchronously
- Output — 3 states
- Package — 100pin QFP (100P6Q-A)

APPLICATION

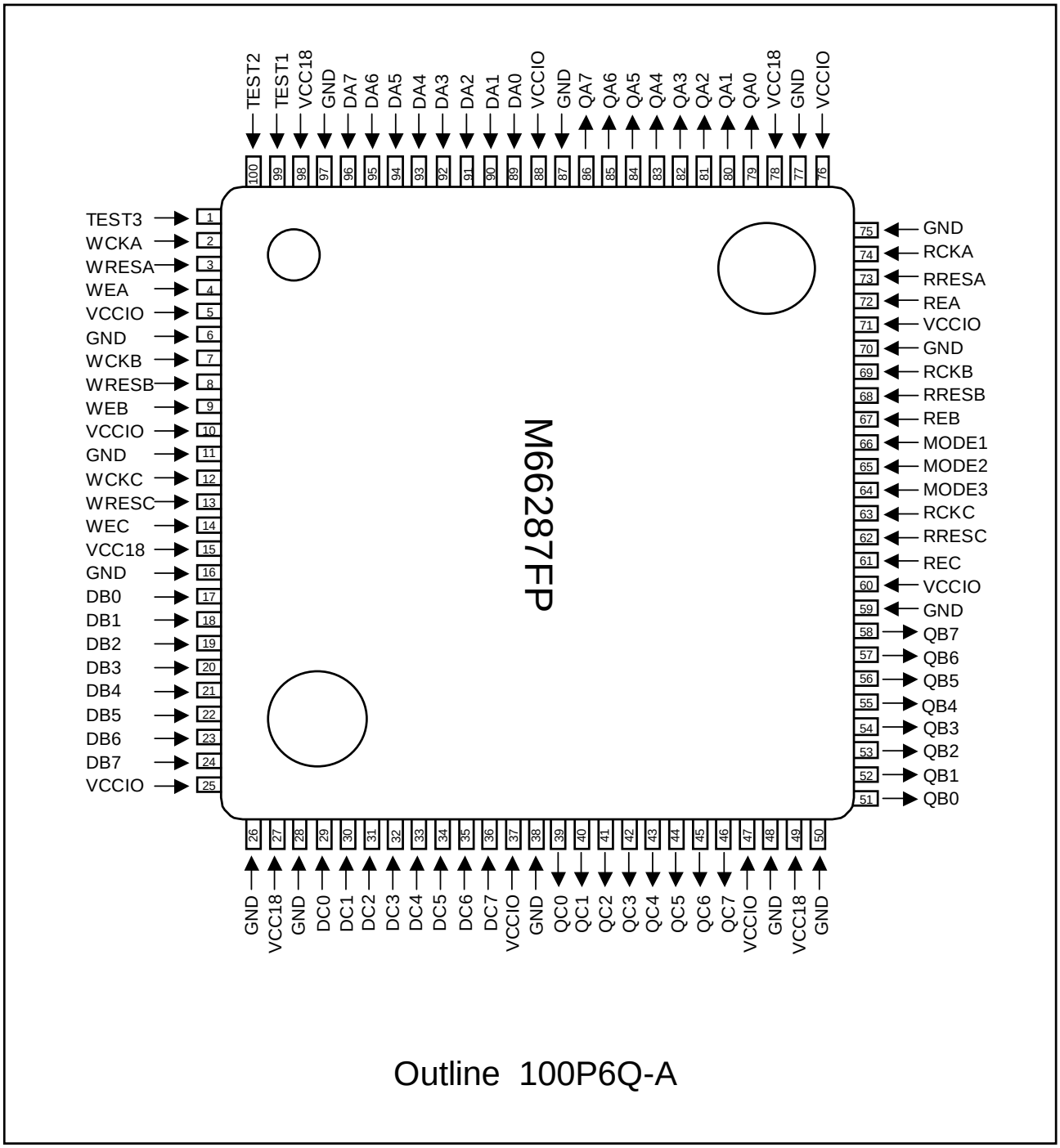
W-CDMA base station, Digital PPC, Digital television, VTR and so on.

MODE DESCRIPTIONS DRAWING

2M-bit x 3 configuration 8-bit bus I/F			3M-bit x 2 configuration 12-bit bus I/F	
MODE 1	MODE 2	MODE 3	MODE 4	MODE 5
				
The three pieces of 256K-word x 8-bit FIFO can be operated completely independently.	The three pieces of 256K-word x 8-bit FIFO are cascade-connected. Write and read operation of FIFO after the 2nd line is controlled by the read system pin of the 1st line.	The two pieces of 256K-word x 8-bit FIFO are cascade-connected and, a piece of 256K-word x 8-bit FIFO can be operated completely independently. Write and read operation of FIFO at the 2nd line is controlled by the read system pin of the 1st line.	The two pieces of 256K-word x 12-bit FIFO can be operated completely independently.	The two pieces of 256K-word x 12-bit FIFO are cascade-connected. Write and read operation of FIFO at the 2nd line is controlled by the read system pin of the 1st line.

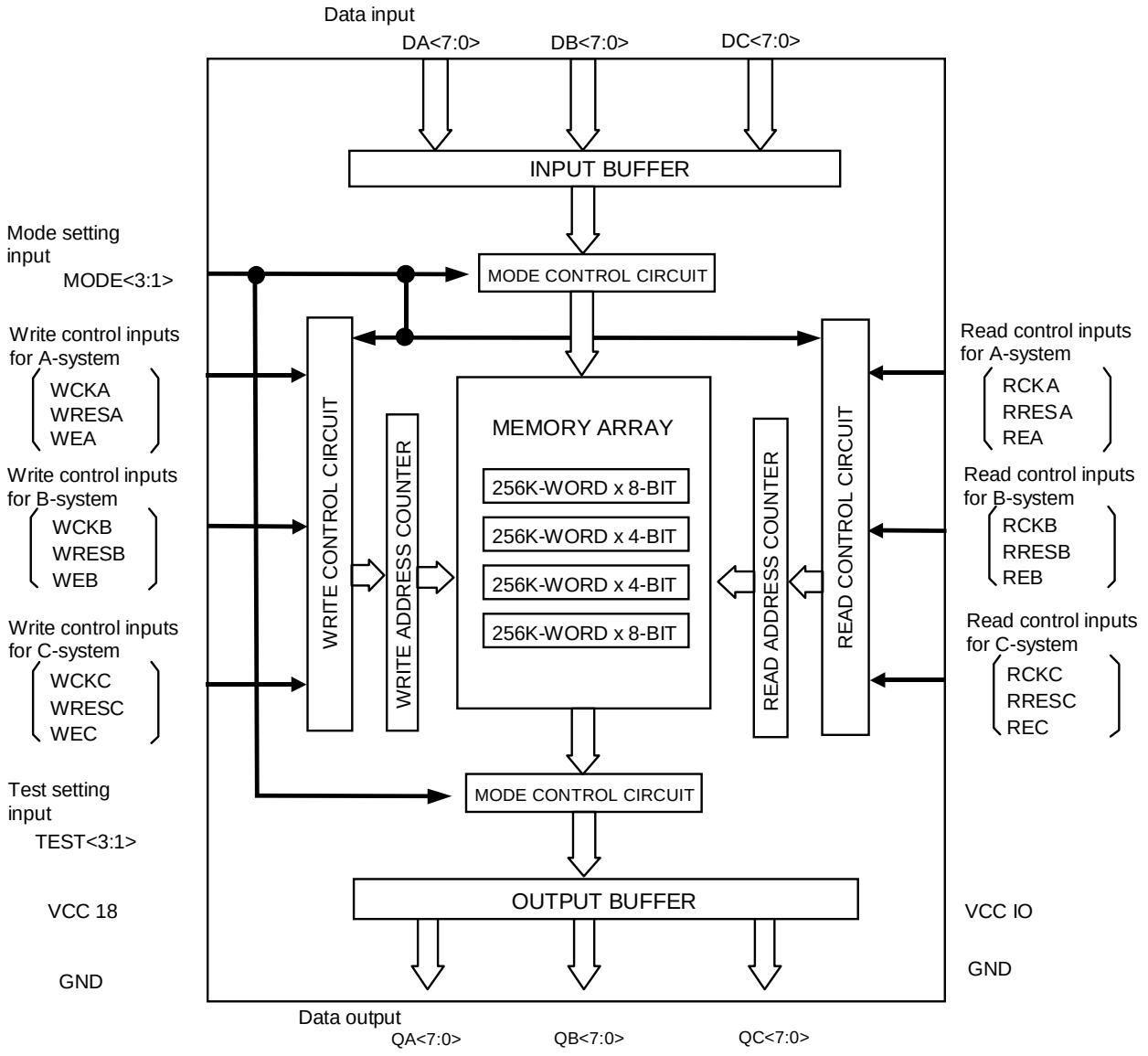
Note: Please refer to "Pin Assignment Table" in "MODE 4 and MODE 5 OPERATION DESCRIPTIONS" for assignment of external pins, Dx<11:0> and Qx<11:0> when used in 12-bit bus interface.

PIN CONFIGURATION (TOP VIEW)



Outline 100P6Q-A

BLOCK DIAGRAM



PIN FUNCTION DESCRIPTIONS

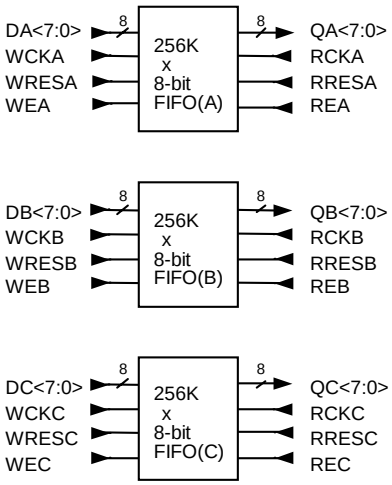
Pin name	Name	Input / output	Function
WCKA WCKB WCKC	Write clock input	Input	They are write clock inputs. WCKA is a write clock for the A-system, WCKB for the B-system and WCKC for the C-system.
WEA WEB WEC	Write enable input	Input	They are write enable control inputs. When they are "L", a write enable status is provided. WEA is a write enable for the A-system, WEB for the B-system and WEC for the C-system.
WRESA WRESB WRESC	Write reset input	Input	They are reset inputs to initialize a write address counter of internal FIFO. When they are "L", a write reset status is provided. WRESA is a write reset for the A-system, WRESB for the B-system and WRESC for the C-system.
RCKA RCKB RCKC	Read clock input	Input	They are read clock inputs. RCKA is a read clock for the A-system, RCKB for the B-system and RCKC for the C-system.
REA REB REC	Read enable input	Input	They are read enable control inputs. When they are "L", a read enable status is provided. REA is a read enable for the A-system, REB for the B-system and REC for the C-system.
RRESA RRESB RRESC	Read reset input	Input	They are reset inputs to initialize a read address counter of internal FIFO. When they are "L", a read reset status is provided. RRESA is a read reset for the A-system, RRESB for the B-system and RRESC for the C-system.
DA<7:0> DB<7:0> DC<7:0>	Data input	Input	They are 8-bit data input bus. DA<7:0> is a data input bus for the A-system, DB<7:0> for the B-system and DC<7:0> for the C-system.
QA<7:0> QB<7:0> QC<7:0>	Data output	Output	They are 8-bit data output bus. QA<7:0> is a data output bus for the A-system, QB<7:0> for the B-system and QC<7:0> for the C-system.
MODE<3:1>	Mode setting input	Input	They are pins for setting operation mode. Setting is refer to MODE SET-table.
TEST<3:1>	Test setting input	Input	They are pins for test. Setting of TEST1 depends on the rising time of the 1.8 V system power supply. For further details, refer to page 11. TEST2 and TEST3 should be fixed at "L".
VCCIO	Power supply pin for I/O	-	This is a 3.3 V power supply pin for I/O.
VCC18	Power supply pin for internal circuit	-	This is a 1.8 V power supply pin for internal circuit.
GND	Ground pin	-	This is a ground pin.

MODE SET

MODE<3:1> should be set to “L” or “H” as shown below according to the five modes to be used.

MODE 3	MODE 2	MODE 1	Operation mode
L	L	L	MODE 1
L	L	H	MODE 2
L	H	L	MODE 3
L	H	H	MODE 4
H	L	L	MODE 5
other than those above			MODE 1

MODE 1 OPERATION DESCRIPTIONS



<Mode 1>

In mode 1, three FIFO memories with 8-bit data bus can be controlled completely individually. Taking FIFO (A) as an example, the operation of FIFO memory is described below. The operation of FIFO (B) and FIFO (C) are the same as that of FIFO (A).

When write enable input WEA is "L", the contents of data input DA<7:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented.

When WEA is "H", writing into FIFO (A) is disabled and the write address counter of FIFO (A) is stopped.

When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

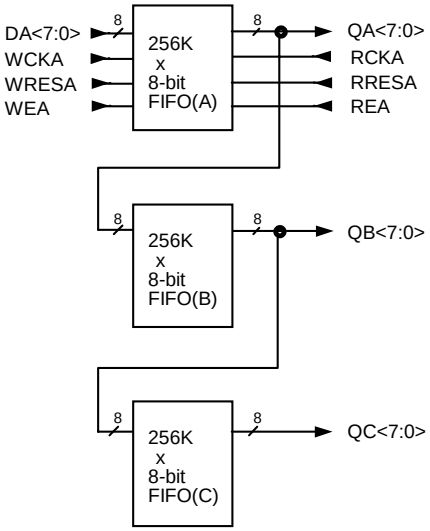
When read enable input REA is "L", the contents of FIFO (A) are outputted to data output QA<7:0> in synchronization with the rising of read clock input RCKA. At this time, the read address counter of FIFO (A) is incremented.

When REA is "H", reading from FIFO (A) is disabled and the read address counter of FIFO (A) is stopped. Also QA<7:0> become high impedance state.

When read reset input RRESA is "L", the read address counter of FIFO (A) is initialized.

Note : The three pieces of 256K-word x 8-bit FIFO can be operated completely independently.

MODE 2 OPERATION DESCRIPTIONS



<Mode 2>

In mode 2, three FIFO memories with 8-bit data bus are cascade-connected and it is possible to generate delay data for 3-lines without external wiring.

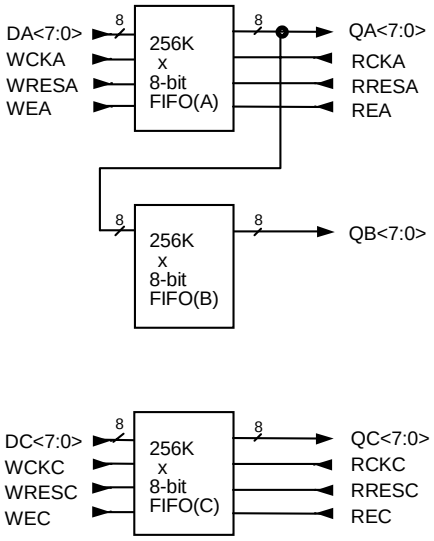
When write enable input WEA is "L", the contents of data input DA<7:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented.
When WEA is "H", writing into FIFO (A) is disabled and the write address counter of FIFO (A) is stopped.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A), FIFO (B) and FIFO (C) are outputted to each QA<7:0>, QB<7:0>, QC<7:0> in synchronization with the rising of read clock input RCKA. At this time, the read address counters of all FIFOs are incremented.
Also the data of the upper FIFO is written into the lower FIFO in synchronization with the rising of RCKA. At this time, the write address counters of FIFO (B) and FIFO (C) are incremented simultaneously.
When REA is "H", reading from FIFO (A), FIFO (B) and FIFO (C) is disabled and the read address counter of each FIFO is stopped. Also all data outputs become high impedance state. And writing into FIFO (B) and FIFO (C) is disabled and the write address counters of FIFO (B) and FIFO (C) are stopped.
When read reset input RRESA is "L", the read address counter of FIFO (A) and the write address counters/read address counters of FIFO (B) and FIFO (C) are initialized.

And, in mode 2, all pins for the A-system, QB<7:0> and QC<7:0> are only used. Therefore the write/read control pins for the B-system and C-sytsem, DB<7:0> and DC<7:0> should be fixed at "L" or "H".

Note : The three pieces of 256K-word x 8-bit FIFO are cascade-connected, and a line delay data can be made easily. Write and read operation of FIFO after the 2nd line is controlled by the read system pin of the 1st line.

MODE 3 OPERATION DESCRIPTIONS



<Mode 3>

In mode 3, two FIFO memories with 8-bit data bus are cascade-connected and the other FIFO memory with an 8-bit data bus is configured completely independently. This makes it possible to generate delay data for 2-lines without external wiring and to control the other independent one FIFO memory.

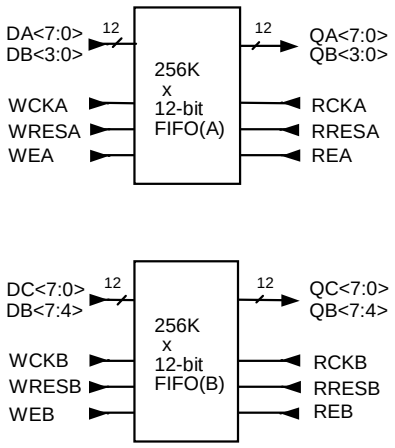
When write enable input WEA is "L", the contents of data input DA<7:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented.
When WEA is "H", writing into FIFO (A) is disabled and the write address counter of FIFO (A) is stopped.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A) and FIFO (B) are outputted to each QA<7:0> and QB<7:0> in synchronization with the rising of read clock input RCKA. At this time, the read address counters of FIFO (A) and FIFO (B) are incremented.
Also the data of FIFO (A) is written into FIFO (B) in synchronization with the rising of RCKA. At this time, the write address counter of FIFO (B) is incremented simultaneously.
When REA is "H", reading from FIFO (A) and FIFO (B) is disabled and the read address counter of each FIFO is stopped. Also QA<7:0> and QB<7:0> become high impedance state. And writing into FIFO (B) is disabled and the write address counter of FIFO (B) is stopped.
When read reset input RRESA is "L", the read address counter of FIFO (A) and the write address counter/read address counter of FIFO (B) are initialized.

The operation of FIFO (C) is the same as that of mode 1.
And, in mode 3, all pins for the A-system and C-system, and QB<7:0> are only used. Therefore the write/read control pins for the B-system and DB<7:0> should be fixed at "L" or "H".

Note : The two pieces of 256K-word x 8-bit FIFO are cascade-connected and, a piece of 256K-word x 8-bit FIFO can be operated completely independently.
Write and read operation of FIFO at the 2nd line is controlled by the read system pin of the 1st line.

MODE 4 OPERATION DESCRIPTIONS



<Mode 4>

In mode 4, two FIFO memories with 12-bit data bus can be controlled completely individually. Taking FIFO (A) as an example, the operation of FIFO memory is described below. The operation of FIFO (B) is the same as that of FIFO (A).

When write enable input WEA is "L", the contents of data input DA<7:0> and DB<3:0>are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented.
When WEA is "H", writing into FIFO (A) is disabled and the write address counter of FIFO (A) is stopped.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A) are outputted to data output QA<7:0> and QB<3:0> in synchronization with the rising of read clock input RCKA. At this time, the read address counter of FIFO (A) is incremented. When REA is "H", reading from FIFO (A) is disabled and the read address counter of FIFO (A) is stopped. Also QA<7:0> and QB<3:0> become high impedance state.
When read reset input RRESA is "L", the read address counter of FIFO (A) is initialized.

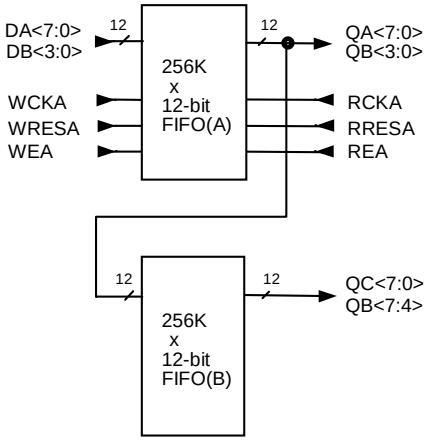
Also, set the 12-bit I/O buses of FIFO (A) and FIFO (B) as shown in the table below.
In mode 4, all pins for the A-system and B-system, DC<7:0> and QC<7:0> are only used. Therefore the write/read control pins for the C-system should be fixed at "L" or "H".

External pin name	**Data input bus of FIFO (A)**	**External pin name**	**Data output bus of FIFO (A)**
DA<7>	11-bit	QA<7>	11-bit
DA<6>	10-bit	QA<6>	10-bit
DA<5>	9-bit	QA<5>	9-bit
DA<4>	8-bit	QA<4>	8-bit
DA<3>	7-bit	QA<3>	7-bit
DA<2>	6-bit	QA<2>	6-bit
DA<1>	5-bit	QA<1>	5-bit
DA<0>	4-bit	QA<0>	4-bit
DB<3>	3-bit	QB<3>	3-bit
DB<2>	2-bit	QB<2>	2-bit
DB<1>	1-bit	QB<1>	1-bit
DB<0>	0-bit	QB<0>	0-bit

External pin name	**Data input bus of FIFO (B)**	**External pin name**	**Data output bus of FIFO (B)**
DC<7>	11-bit	QC<7>	11-bit
DC<6>	10-bit	QC<6>	10-bit
DC<5>	9-bit	QC<5>	9-bit
DC<4>	8-bit	QC<4>	8-bit
DC<3>	7-bit	QC<3>	7-bit
DC<2>	6-bit	QC<2>	6-bit
DC<1>	5-bit	QC<1>	5-bit
DC<0>	4-bit	QC<0>	4-bit
DB<7>	3-bit	QB<7>	3-bit
DB<6>	2-bit	QB<6>	2-bit
DB<5>	1-bit	QB<5>	1-bit
DB<4>	0-bit	QB<4>	0-bit

Note : The two pieces of 256K-word x 12-bit FIFO can be operated completely independently.

MODE 5 OPERATION DESCRIPTIONS



<Mode 5>

In mode 5, two FIFO memories with 12-bit data bus are cascade-connected and it is possible to generate delay data for 2-lines without external wiring.

When write enable input WEA is "L", the contents of data input DA<7:0> and DB<3:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented.

When WEA is "H", writing into FIFO (A) is disabled and the write address counter of FIFO (A) is stopped.

When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A) and FIFO (B) are outputted to each QA<7:0>, QB<3:0> and QC<7:0> and QB<7:4> in synchronization with the rising of read clock input RCKA. At this time, the read address counters of FIFO (A) and FIFO (B) are incremented.

Also the data of FIFO (A) is written into FIFO (B) in synchronization with the rising of RCKA. At this time, the write address counter of FIFO (B) is incremented simultaneously.

When REA is "H", reading from FIFO (A) and FIFO (B) is disabled and the read address counter of each FIFO is stopped. Also all data outputs become high impedance state. And writing into FIFO (B) is disabled and the write address counter of FIFO (B) is stopped.

When read reset input RRESA is "L", the read address counter of FIFO (A) and the write address counter/read address counter of FIFO (B) are initialized.

Also, set the 12-bit I/O buses of FIFO (A) and FIFO (B) as shown in the table below.

In mode 5, all pins for the A-system, DB<3:0>, QB<7:0> and QC<7:0> are only used. Therefore the write/read control pins for the B-system and the C-system, DB<7:4> and DC<7:0> should be fixed at "L" or "H".

External pin name	**Data input bus of FIFO (A)**	**External pin name**	**Data output bus of FIFO (A)**	**External pin name**	**Data output bus of FIFO (B)**
DA<7>	11-bit	QA<7>	11-bit	QC<7>	11-bit
DA<6>	10-bit	QA<6>	10-bit	QC<6>	10-bit
DA<5>	9-bit	QA<5>	9-bit	QC<5>	9-bit
DA<4>	8-bit	QA<4>	8-bit	QC<4>	8-bit
DA<3>	7-bit	QA<3>	7-bit	QC<3>	7-bit
DA<2>	6-bit	QA<2>	6-bit	QC<2>	6-bit
DA<1>	5-bit	QA<1>	5-bit	QC<1>	5-bit
DA<0>	4-bit	QA<0>	4-bit	QC<0>	4-bit
DB<3>	3-bit	QB<3>	3-bit	QB<7>	3-bit
DB<2>	2-bit	QB<2>	2-bit	QB<6>	2-bit
DB<1>	1-bit	QB<1>	1-bit	QB<5>	1-bit
DB<0>	0-bit	QB<0>	0-bit	QB<4>	0-bit

Note : The two pieces of 256K-word x 12-bit FIFO are cascade-connected, and a line delay data can be made easily. Write and read operation of FIFO at the 2nd line is controlled by the read system pin of the 1st line.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}18$	Supply voltage (1.8 V power supply)	A value based on GND	-0.3~+2.5	V
$V_{CC}IO$	Supply voltage (3.3 V power supply)		-0.3~+3.8	V
V_I	Input voltage		-0.3~V_{CC}IO+0.3	V
V_O	Output voltage		-0.3~V_{CC}IO+0.3	V
P_d	Maximum power dissipation	Ta = 70 °C	800	mW
T_{stg}	Storage temperature		-55~150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{CC}18$	Supply voltage for internal circuit (1.8 V power supply)	A value based on GND	1.62	1.8	1.98	V
$V_{CC}IO$	Supply voltage for I/O (3.3 V power supply)		3.0	3.3	3.6	V
T_{opr}	Operating ambient temperature		0		70	°C

DC CHARACTERISTICS

(Ta = 0 ~ 70°C, Vcc18 = 1.8 ± 0.18 V, VccIO = 3.3 ± 0.3 V, GND = 0 V, unless otherwise noted)

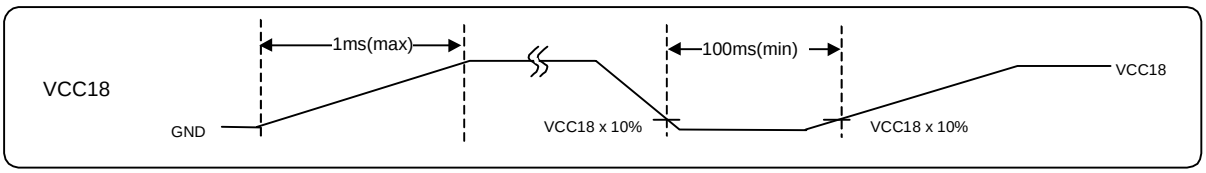
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	"H" input voltage	A value based on GND	0.8 x VccIO			V
V_{IL}	"L" input voltage				0.2 x VccIO	V
V_{OH}	"H" output voltage	I_{OH} = -4mA	VccIO - 0.4			V
V_{OL}	"L" output voltage	I_{OL} = 4mA			0.4	V
I_{IH}	"H" input current	V_I = V_{CC}IO			10	µA
I_{IL}	"L" input current	V_I = GND			-10	µA
I_{OZH}	Off state "H" output current	V_O = V_{CC}IO			10	µA
I_{OZL}	Off state "L" output current	V_O = GND			-10	µA
$I_{CC}18$	Operating mean current dissipation (1.8 V)	$V_{CC}18$ = 1.8 V ± 0.18 V $V_{CC}IO$ = 3.3 V ± 0.3 V			135	mA
$I_{CC}IO$	Operating mean current dissipation (3.3 V)	V_I = repeat "H" and "L" Output open tWCK = tRCK = 16.6 ns			145	mA
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Off state output capacitance	f = 1 MHz			15	pF

POWER - ON

After power-on, this IC initializes some circuits of internal FIFO (1.8 V), using the built-in power-on reset circuit.
This power-on reset is performed by using the $V_{CC}18$ = 1.8 V system power supply.
Either of the following conditions (1) or (2) should be met according to the power-on time of the $V_{CC}18$.

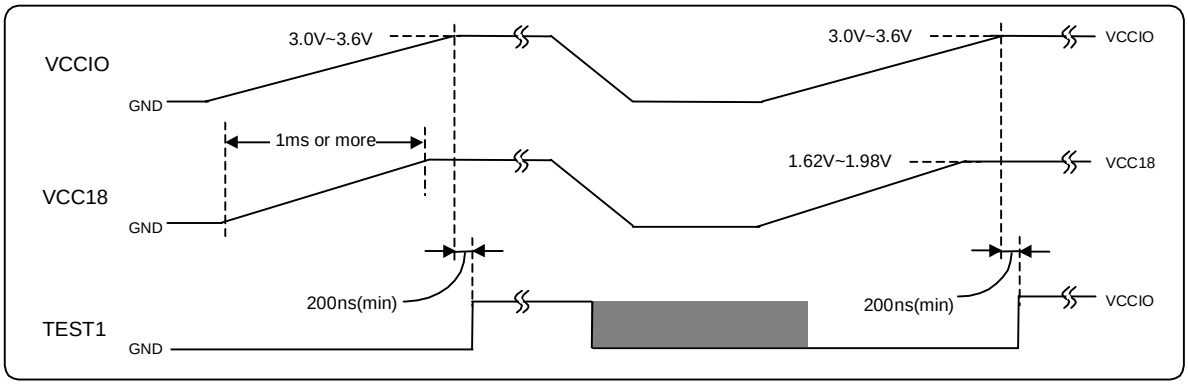
(1) When the power-on time of the $V_{CC}1.8$ is 1 msec or less:

Some circuits of internal FIFO are initialized by the built-in power-on reset circuit. No restriction is imposed on the power-on sequence between $V_{CC}18$ and $V_{CC}IO$ = 3.3 V system power supply. When powering on again after power-on, provide an interval of 100 ms or more for the $V_{CC}18$. At this time, the TEST1 (pin 99) pin should be fixed at "L".



(2) When the power-on time of the $V_{CC}18$ is more than 1 msec:

Some circuits of internal FIFO should be initialized by the TEST1 (pin 99) pin.
Input a initialize reset pulse of 200 ns or more after the power supplies ($V_{CC}IO$, $V_{CC}18$) reach to the V_{CC} level.
There is no problem even if reaching to the V_{CC} level on which power supply.



Note : Some circuits of internal FIFO can be initialized by the TEST1 pin even if the power-on time of the $V_{CC}18$ is 1 msec or less.

Note : Important matter;

Provide write reset cycles and read reset cycles of 100 cycles or more, respectively after the VCC reaches to the specified voltage after power-on.

When inputting a reset pulse using the TEST1 (pin 99) pin, provide write reset cycles and read reset cycles of 100 cycles or more, respectively after inputting a reset pulse at power-on.

There is no problem in this reset operation if a total of 100 cycles or more is achieved, even if discontinuous reset input is made.

TIMING REQUIREMENTS

(Ta = 0 ~ 70°C, $V_{CC}18$ = 1.8 ± 0.18 V, $V_{CC}IO$ = 3.3 ± 0.3 V, GND = 0 V, unless otherwise noted)

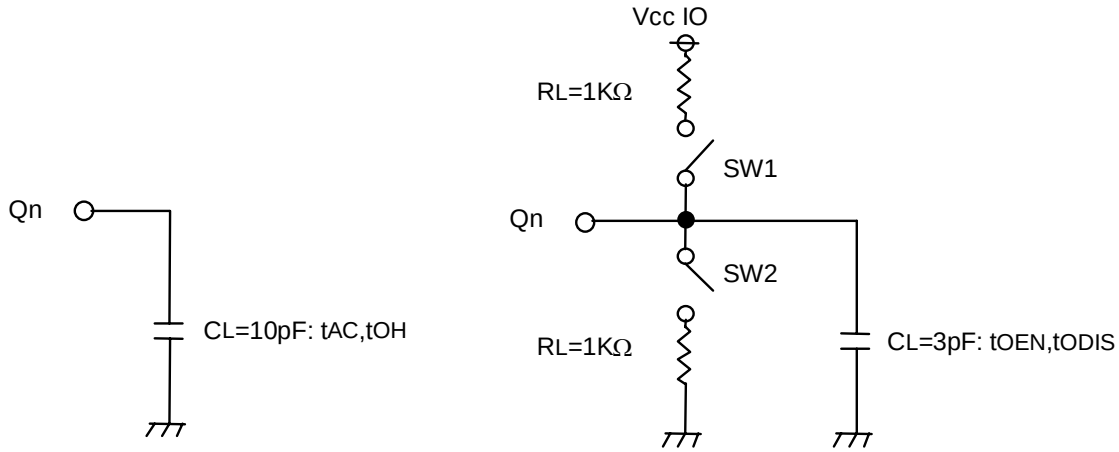
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WCK}	Write clock (WCK) cycle	16.6			ns
t_{WCKH}	Write clock (WCK) "H" pulse width	6.5			ns
t_{WCKL}	Write clock (WCK) "L" pulse width	6.5			ns
t_{RCK}	Read clock (RCK) cycle	16.6			ns
t_{RCKH}	Read clock (RCK) "H" pulse width	6.5			ns
t_{RCKL}	Read clock (RCK) "L" pulse width	6.5			ns
t_{DS}	Input data setup time to WCK	3.5			ns
t_{DH}	Input data hold time to WCK	2			ns
t_{RESS}	Reset setup time to WCK or RCK	3.5			ns
t_{RESH}	Reset hold time to WCK or RCK	2			ns
t_{NRESS}	Reset nonselect setup time to WCK or RCK	3.5			ns
t_{NRESH}	Reset nonselect hold time to WCK or RCK	2			ns
t_{WES}	Write enable setup time to WCK	3.5			ns
t_{WEH}	Write enable hold time to WCK	2			ns
t_{NWES}	Write enable nonselect setup time to WCK	3.5			ns
t_{NWEH}	Write enable nonselect hold time to WCK	2			ns
t_{RES}	Read enable setup time to RCK	3.5			ns
t_{REH}	Read enable hold time to RCK	2			ns
t_{NRES}	Read enable nonselect setup time to RCK	3.5			ns
t_{NREH}	Read enable nonselect hold time to RCK	2			ns
t_r, t_f	Input pulse rise/fall time			3	ns

SWITCHING CHARACTERISTICS

(Ta = 0 ~ 70°C, $V_{CC}18$ = 1.8 ± 0.18 V, $V_{CC}IO$ = 3.3 ± 0.3 V, GND = 0 V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AC}	Output access time to RCK			13	ns
t_{OH}	Output hold time to RCK	2			ns
t_{OEN}	Output enable time to RCK	2		13	ns
t_{ODIS}	Output disable time to RCK	2		13	ns

SWITCHING CHARACTERISTICS MEASUREMENT CIRCUIT



Parameter	SW1	SW2
t_{ODIS} (LZ)	Close	Open
t_{ODIS} (HZ)	Open	Close
t_{OEN} (ZL)	Close	Open
t_{OEN} (ZH)	Open	Close

Input pulse level : 0~V_{CC}IO

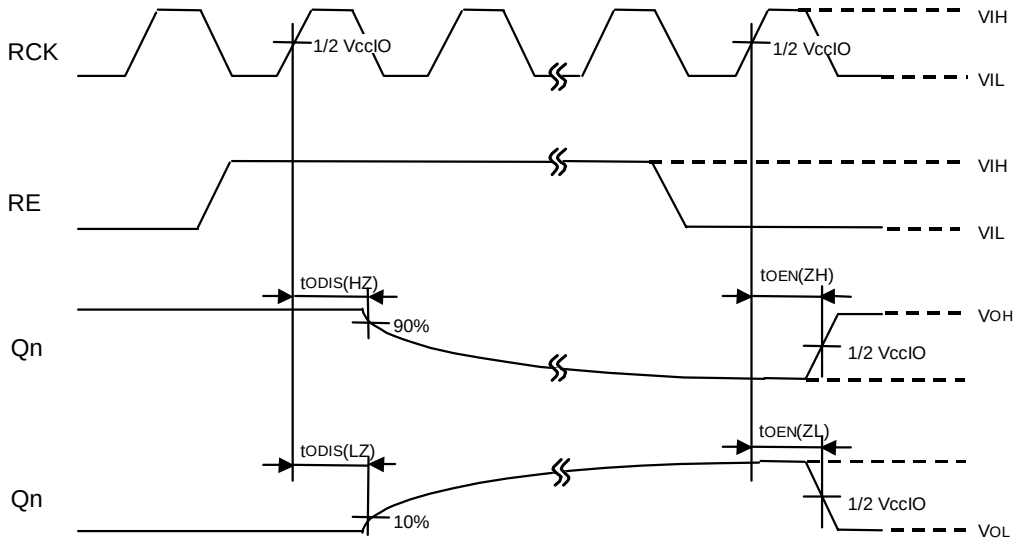
Input pulse rise/fall time : 1 ns

Decision voltage input : 1/2 V_{CC}IO

Decision voltage output : 1/2 V_{CC}IO (However, t_{ODIS} (LZ) is 10% of output amplitude and t_{ODIS} (HZ) is 90% of that for decision).

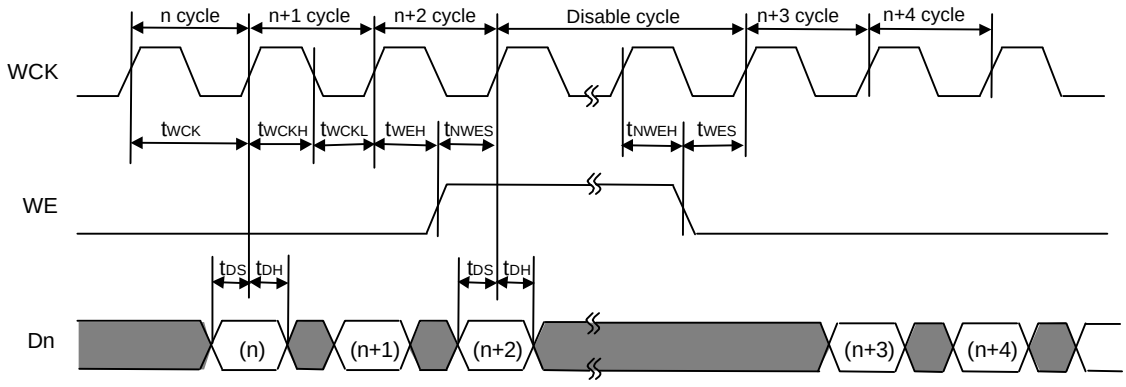
The load capacitance CL includes the floating capacitance of connection and the input capacitance of probe.

t_{ODIS} and t_{OEN} MEASUREMENT CONDITION



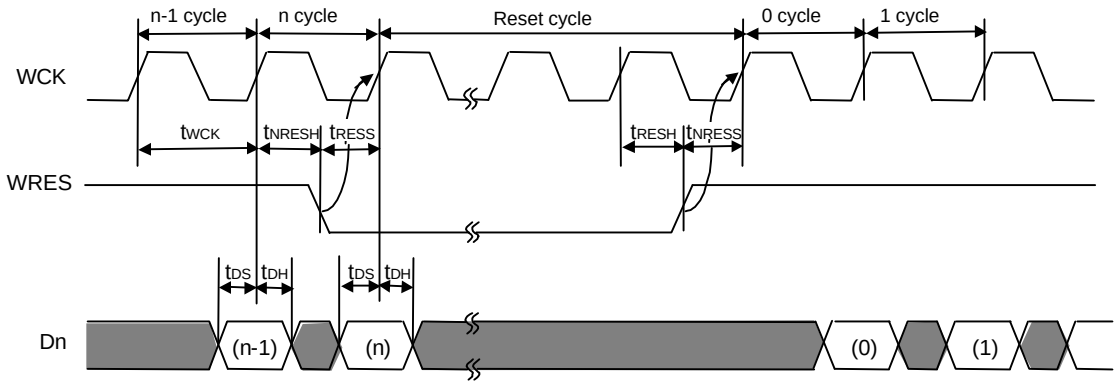
OPERATING TIMING

● WRITE CYCLE



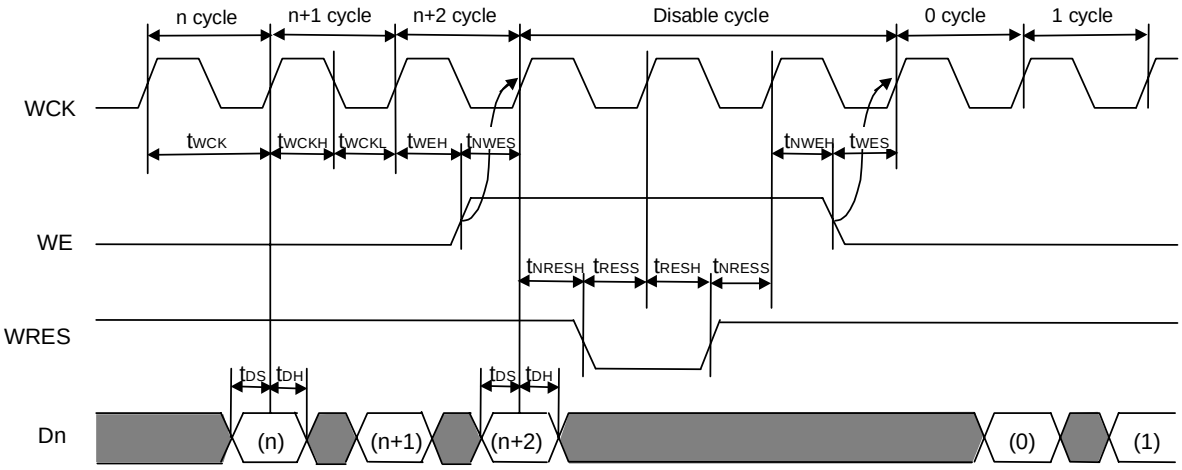
WRES = "H"

● WRITE RESET CYCLE



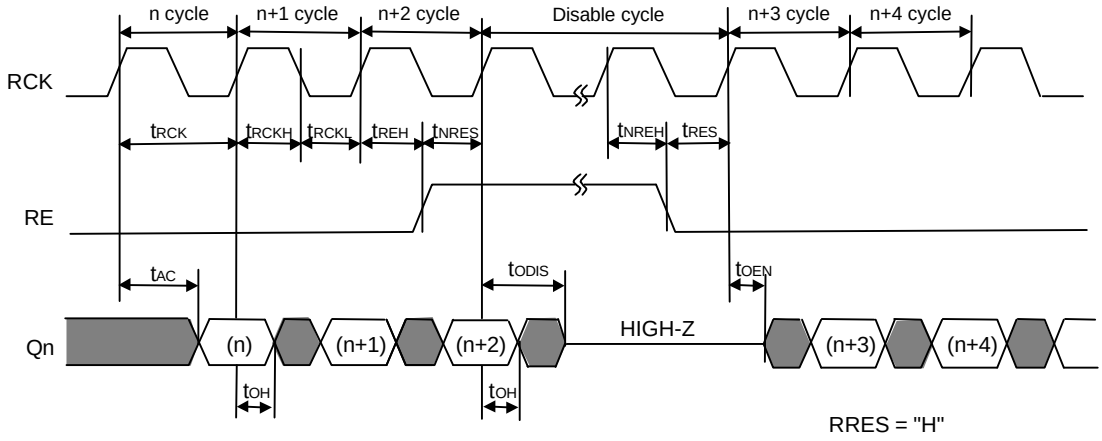
In case of WE = "L"

● **WRITE RESET and WRITE ENABLE COMBINATION CYCLE**

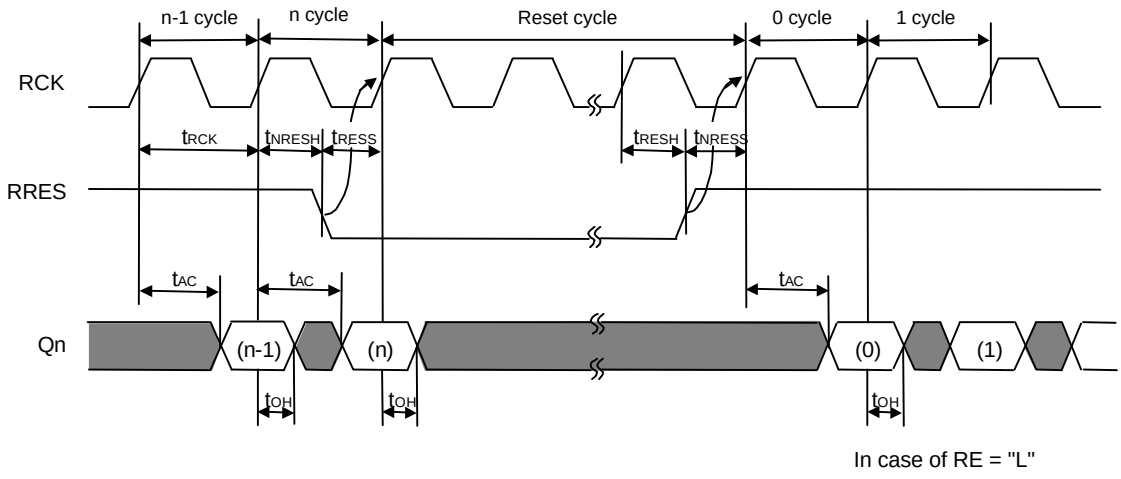


Note : There are no restrictions of WE to WRES.

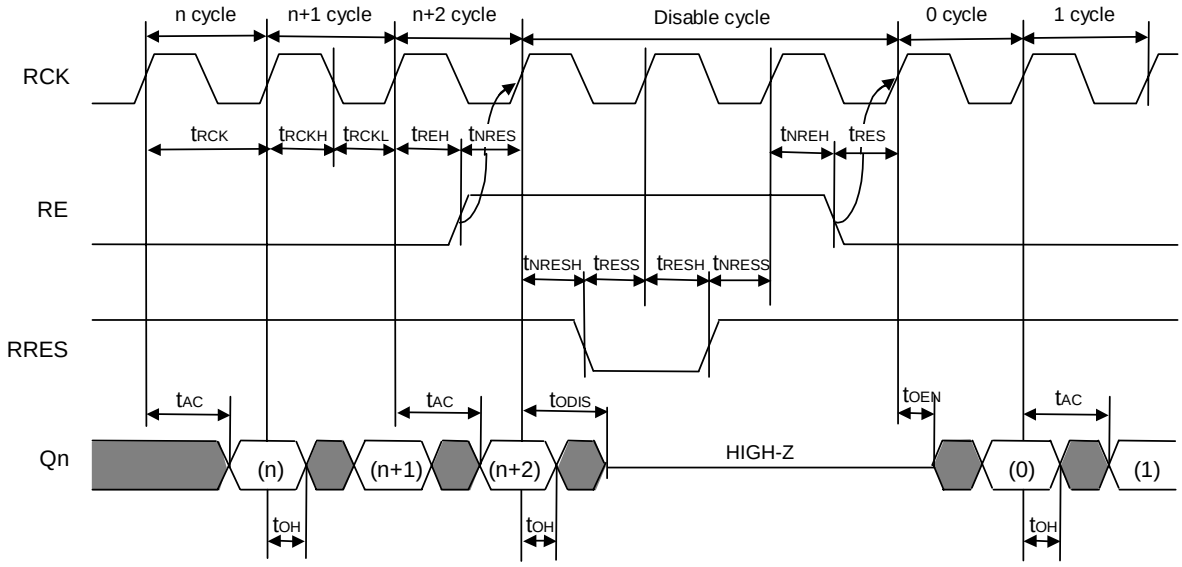
● READ CYCLE



● READ RESET CYCLE



● **READ RESET and READ ENABLE COMBINATION CYCLE**

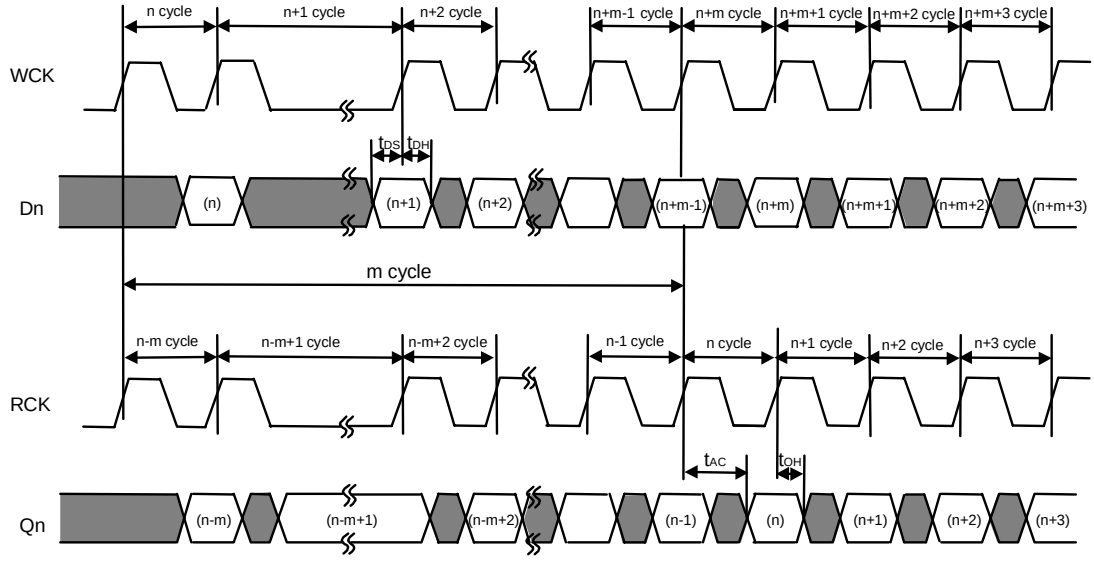


Note : There are no restrictions of RE to RRES.

● ATTENTIONS when WCK and RCK STOP

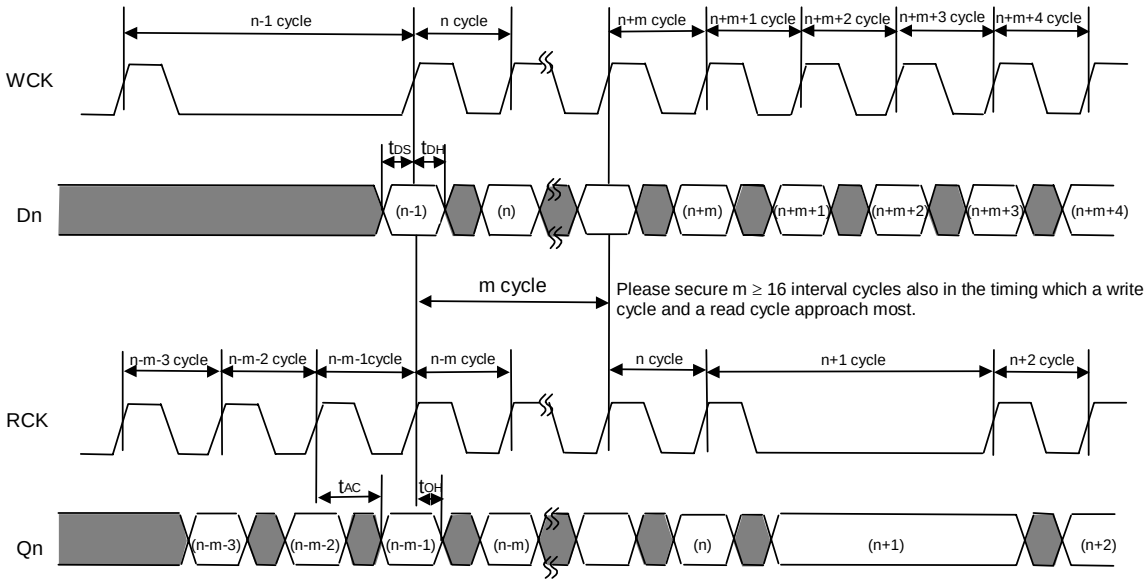
The intervals of 16 cycles or more between a write cycle and a read cycle should be secured, and WCK and RCK should be inputted for 16 cycles or more based on beginning of write n cycle at any timing, when both WCK and RCK or either of both is stopped and the newest data is read after it restarts.
Output data becomes undefined when these restrictions are not filled.

<TIMING 1> When WCK and RCK stop synchronously



m ≥ 16
WRES = "H"
RRES = "H"
WE = "L"
RE = "L"

<TIMING 2> When WCK and RCK stop asynchronously

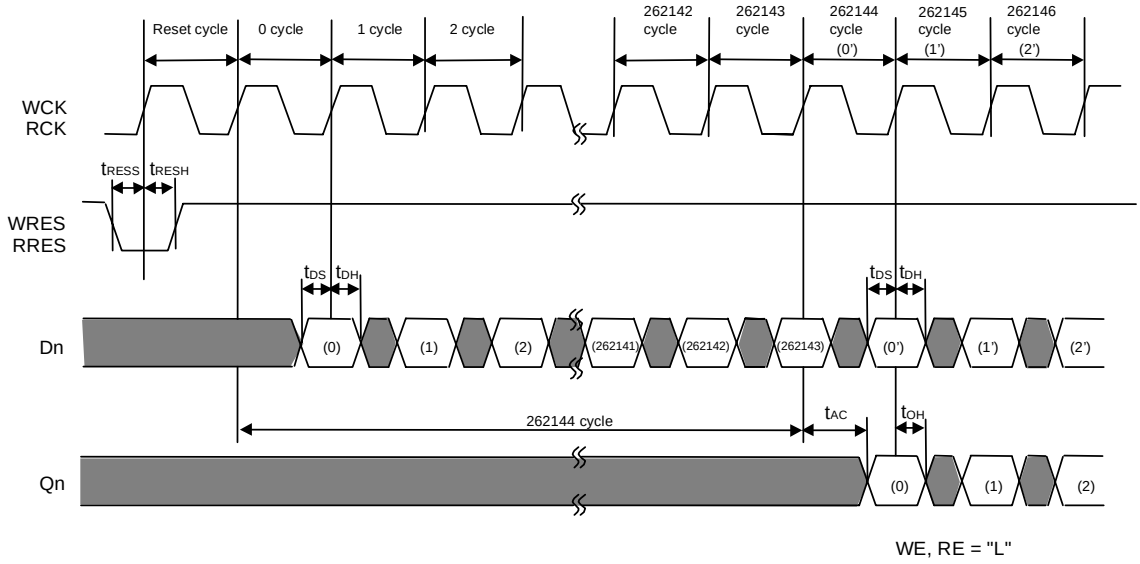


m ≥ 16
WRES = "H"
RRES = "H"
WE = "L"
RE = "L"

VARIABLE LENGTH DELAY BITS

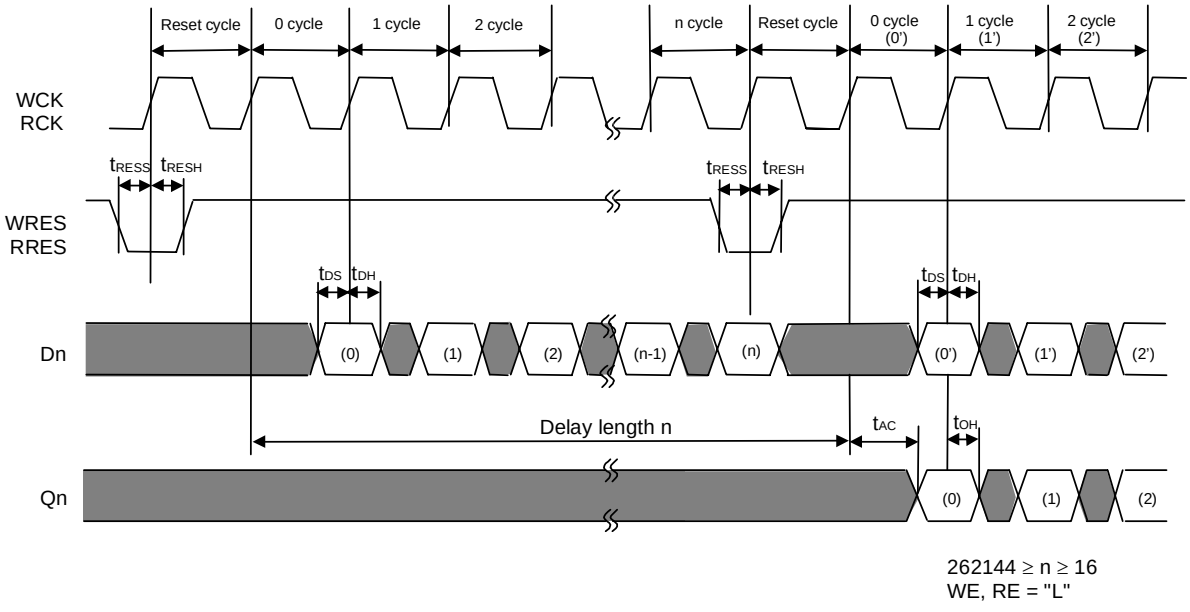
● 1-LINE (262144-BIT) DELAY

In read cycles, an output data is read at the (first) rising edge of RCK start the cycle. In write cycles, an input data is written at the (second) rising edge of WCK end the cycle. So 1-line delay can be made easily according to the control method of the following figure.



● N-BIT DELAY 1

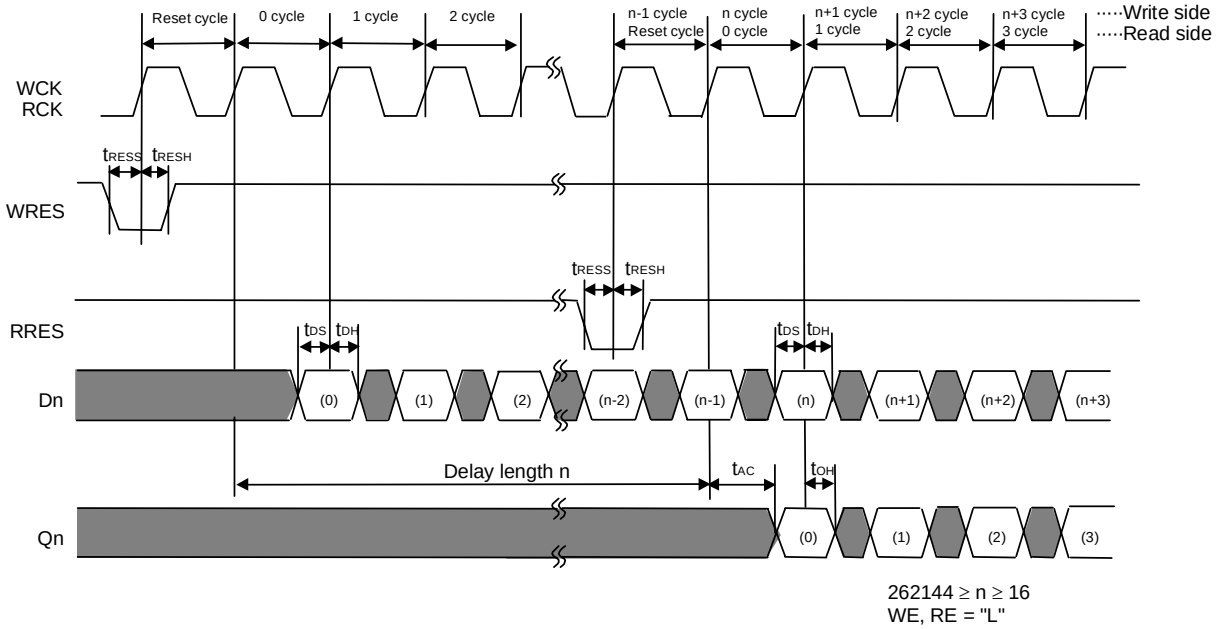
(Reset at a cycle corresponding to delay length)



Note : The intervals of 16 cycles or more between a write cycle and a read cycle should be secured to read data written in a certain cycle.

● **N-BIT DELAY 2**

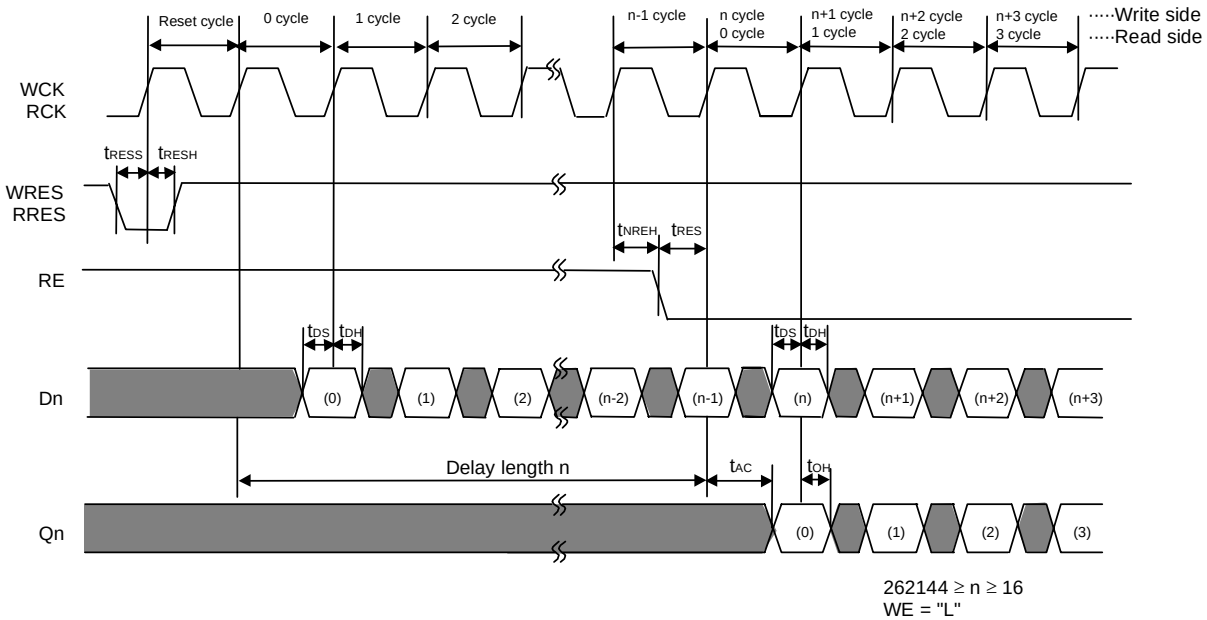
(Sliding timings of WRES and RRES at a cycle corresponding to delay length)



262144 ≥ n ≥ 16
WE, RE = "L"

● **N-BIT DELAY 3**

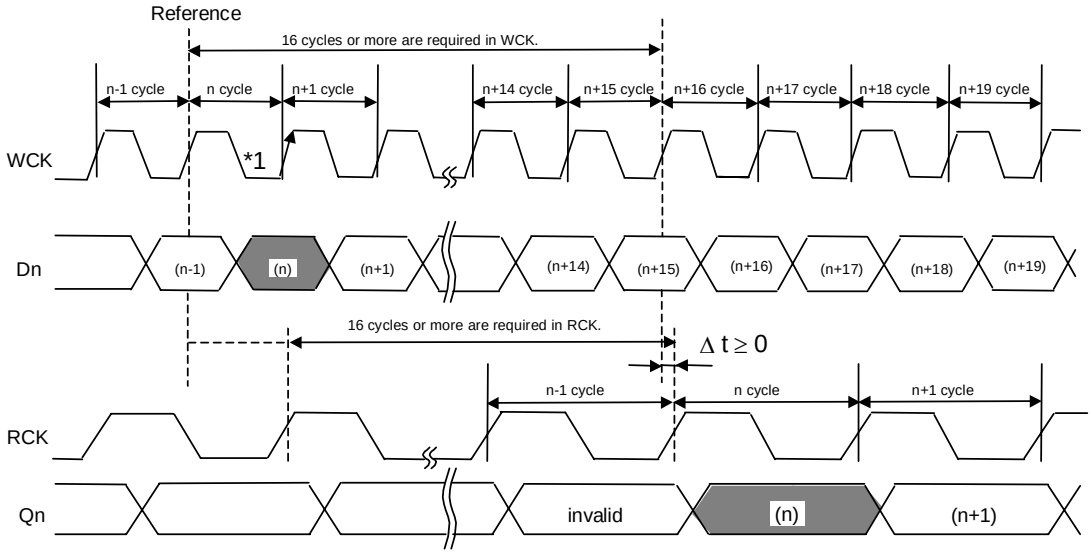
(Sliding address by disabling RE at a cycle corresponding to delay length)



262144 ≥ n ≥ 16
WE = "L"

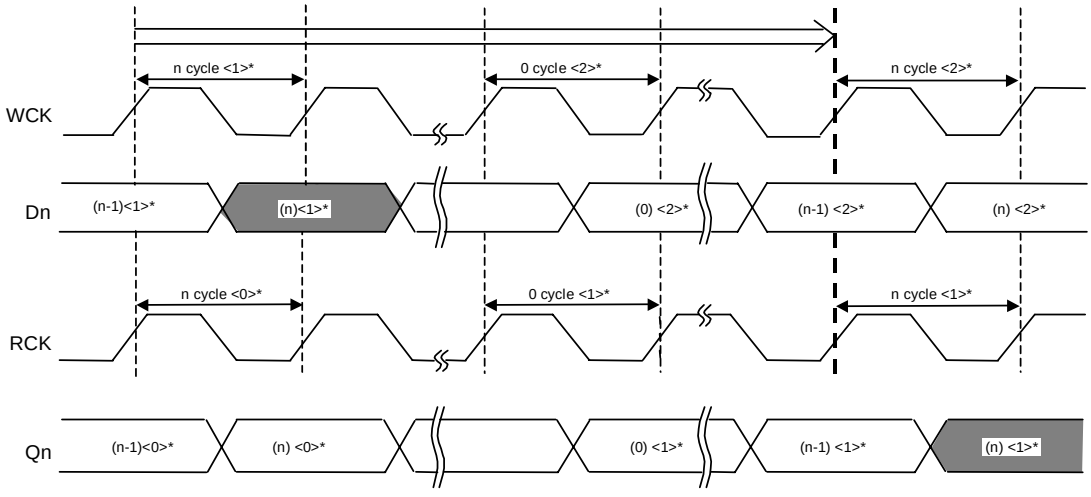
SHORTEST READING of WRITTEN DATA in N CYCLE WHEN WRITE and READ OPERATED ASYNCHRONOUSLY

The intervals of 16 cycles or more between a write cycle and a read cycle should be secured and WCK and RCK should be inputted for 16 cycles or more based on beginning of write n cycle at any timing to read written data (data fetched at the rising edge of WCK shown *1 in the following figure) with n cycles on write side.
On read side, n cycles should be started after the completion of n+15 cycles on write side ($\Delta t \geq 0$ in the following figure).
Output data becomes undefined when these restrictions are not filled.



LONGEST READING of WRITTEN DATA in N CYCLE : 1-LINE DELAY

Data output Qn of n cycle <1>* can be read immediately before until the start of n cycle <1>* on read side and the start of n cycle <2>* on write side over lap each other.



<0>*, <1>* and <2>* indicate a line value.