M66333FP

FACSIMILE IMAGE DATA PROCESSOR

DESCRIPTION

The M66333 is a facsimile image processing controller that converts analog signals that are photoelectrically converted by an image sensor into bi-level signals.
It has image processing functions such as, peak detection, uniformity correction, γ correction, MTF compensation, detector of background and object level, dither control, separation of image data area, error diffusion, scale down, and area specification.
This controller has a built-in 7bits flash type A-D converter and interface circuits to image sensor, analog signal processing circuit, and CODEC (Coder & Decoder) to simplify control of the readout mechanism.

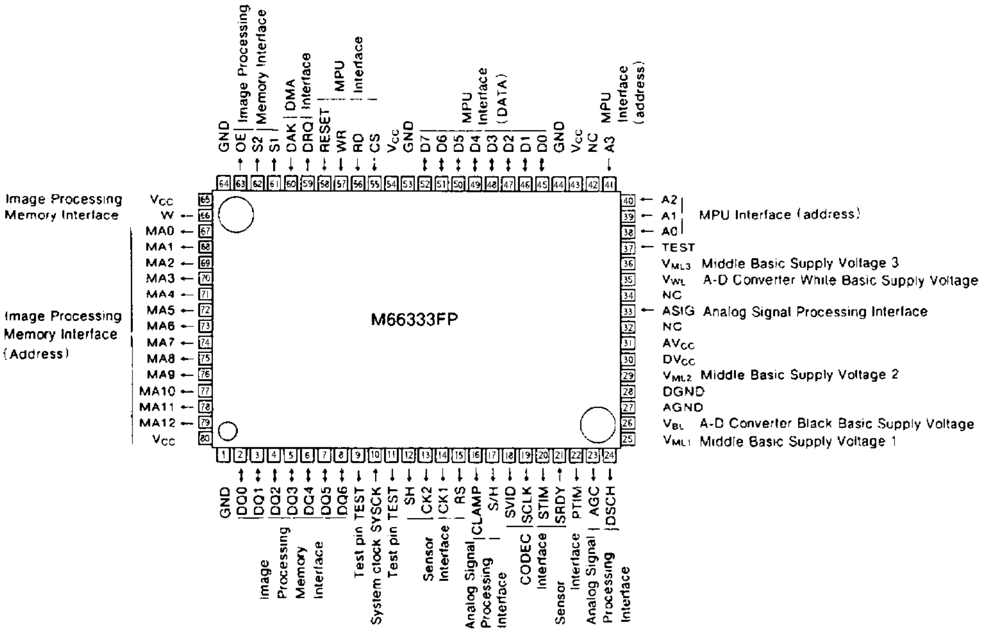
FEATURES

- High Speed Scan·········· MAX 2ms/Line, TYP 5ms/Line
- A3 (8pixels/mm) Line Sensor Attachment
- Image sensor (CCD, CIS) control signal generation
  CCD : SH, CK1, CK2, RS
  Contact sensor (CIS) : SH, CK1 (or CK2)
- Analog signal processing circuit control signal generation
  CLAMP, S/H, AGC, DSCH
- Built-in 7bit Flash A-D Converter
- Bi-level data external output interface
  Serial output (→M66330)
  8-bit MPU bus output with external DMA control signal
- Image Data Processing
  Uniformity Correction (All pixel Correction)
  MTF compensation (2 dimension)
  Detector of background and object level (programmable)
  Pseudo half-tone
    - Dither method (32 levels using 4X8 matrix)
    - Error diffusion (6-bit data processing)
  Separation of image data area (2 dimension)
  Scale Down A3→B4, A3→A4, B4→A4
- 5V Single Power Supply

APPLICATION

Facsimile

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N-A

NC : No Connection

BLOCK DIAGRAM

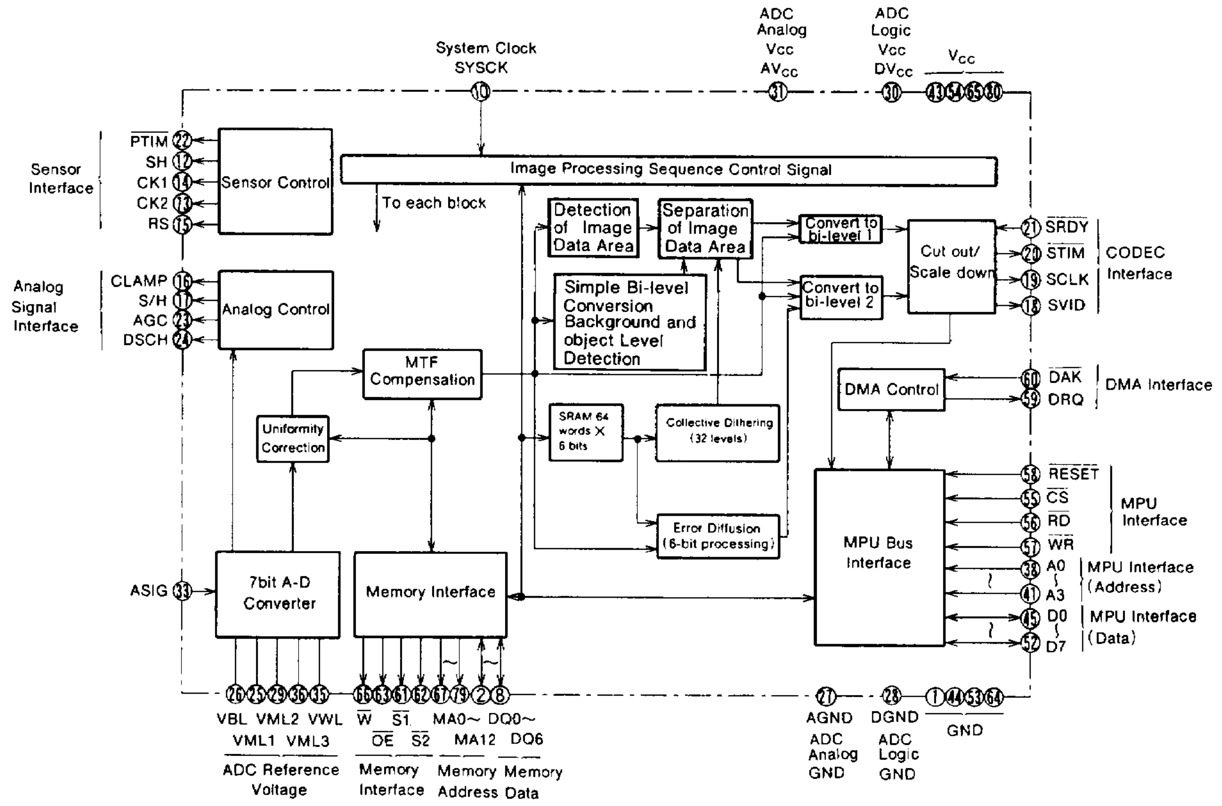


Table 1 Image processing functions

Image Processing Function	Specifications	Remarks
Read Width	• A4, B4, A3	
Resolution	• 8 pixels/mm (primary scanning direction)	
Read speed	• 5ms/line Typ, 2ms/line maximum	• Operated with system clock and PRE_DATA (registers 3, 4)
Uniformity Correction	• White Correction for CCD • White/black Correction for CIS • All pixel correction • Correction range 50%	• External correction memory is used (read/write allowed from MPU)
MTF Compensation	• Laplacian filter circuit before, after, left, and right of target pixel (2 dimension)	• External compensation memory is used
Simple Bi-level Conversion	• Floating threshold method using background and object level detection circuit	
Pseudo half-tone	• Dither method : 32 levels (4X8 matrix)	• Built-in 64 wordsX6 bit SRAM for dither memory (read/write allowed from MPU)
	• Error diffusion : 6-bit data processing (64 levels)	• External error buffer memory is used
Separation of Image Data Area	• Detection by brightness difference of 3X3 pixels in previous, current, and next lines	• Processing memory area is the same as correction memory area
Scale Down	• Selection method • Scale down : A3→B4 set to 13/15, B4→A4 set to 9/11, A3→A4 is set to 12/17	
γ Correction	• Logarithmic correction	• Apply external voltage (resistor connection is also allowed) to A-D converter middle basic supply voltage pins.
Image Sensor Control Signal	• Contact sensor (CIS) and CCD control signal generation	
Analog Signal Processing	• Generate control signals for external CLAMP circuit, sample/hold circuit, and AGC circuit	• Built-in 7-bit flash A-D converter

PIN DESCRIPTIONS

Block	Pin Names	I/O	Description
Sensor Interface	SH	O	CCD : Shift pulse signal to transmit photo charges from the sensor to the transfer unit. CIS : Start signal for the sensor read circuit.
	CK1	O	CCD : Clock pulse signal for sequentially transmitting the transfer unit signal charge of the sensor. CIS : Clock pulse signal for the sensor read circuit shift register.
	CK2	O	Reverse of CK1.
	RS	O	Pulse to reset the voltage of the CCD sensor floating capacitor to initial status.
	$\overline{\mathrm{PTIM}}$	O	Read roller pulse motor control signal.
Analog Circuit Interface	CLAMP	O	CLAMP pulse to set the dark level of the sensor to reference voltage of the digital circuit.
	S/H	O	Sample hold signal to smooth out sensor image signal waveform.
	ASIG	I	Analog signal.
	AGC	O	External AGC circuit gain down signal.
	DSCH	O	External AGC circuit gain up signal.
Memory Interface	$\overline{\mathrm{W}}$	O	External RAM write enable signal.
	$\overline{\mathrm{OE}}$	O	External RAM output enable signal.
	$\overline{\mathrm{S1}}$, $\overline{\mathrm{S2}}$	O	External RAM, ROM chip select signal.
	MA0~12	O	External RAM, ROM address signals. MA0 is LSB.
	DQ0~DQ6	I/O	External RAM, ROM data bus. DQ0 is LSB and DQ6 is MSB.
CODEC Interface	$\overline{\mathrm{SRDY}}$	I	Data transmission ready signal from CODEC.
	$\overline{\mathrm{STIM}}$	O	Data transmisson bound signal for CODEC.
	SCLK	O	Clock signal for transmitting image data to CODEC.
	SVID	O	Serial output of image data to CODEC. "H" : Black, "L" White.
DMA Interface	DRQ	O	DMA request signal to external DMA controller for parallel output of image data through MPU bus.
	$\overline{\mathrm{DAK}}$	I	DMA acknowledge signal from external DMA controller for the above DRQ signal.
Clock	SYSCK	I	System clock input pin.
MPU Interface	$\overline{\mathrm{RESET}}$	I	System reset signal. Resets counter, register, F/F, latch and sets internal memory in standby mode and halts clock generation circuit.
	$\overline{\mathrm{CS}}$	I	Chip select signal used by MPU to access M66333. Set to "H" in operating mode (AGC, UNIF, SCAN).
	$\overline{\mathrm{RD}}$	I	Control signal used by MPU to read data from M66333.
	$\overline{\mathrm{WR}}$	I	Control signal used by MPU to write data to M66333.
	A0~A3	I	Address signals used to access M66333 internal registers.
	D0~D7	I/O	8-bit bidirectional buffer.

PIN DESCRIPTIONS (CONTINUED)

Block	Pin Names	I/O	Description
Other	V_{CC}	—	Plus supply voltage.
	AV_{CC}	—	Plus supply voltage for A-D converter analog units.
	DV_{CC}	—	Plus supply voltage for A-D converter logic units.
	GND	—	GND pin.
	AGND	—	Ground for A-D converter analog units.
	DGND	—	Ground for A-D converter digital units.
	V_{WL}	—	A-D converter white basic supply voltage pin.
	V_{BL}	—	A-D converter black basic supply voltage pin.
	V_{ML1}	—	Middle basic supply voltage pin. $V_{ML1}=(V_{WL}-V_{BL})/4$.
	V_{ML2}	—	Middle basic supply voltage pin. $V_{ML2}=2 \cdot (V_{WL}-V_{BL})/4$.
	V_{ML3}	—	Middle basic supply voltage pin. $V_{ML3}=3 \cdot (V_{WL}-V_{BL})/4$.
	TEST (IN)	—	Test input pin. Fix to "L".
	TEST (OUT)	—	Test output pin. Keep open.

FUNCTIONAL DESCRIPTION

The following items which are necessary to use the image processing functions of the M66333 are described.

(1) Operating mode
(2) Line period and read sequence
(3) Image processing function
(4) Sensor unit/analog signal processing unit interface
(5) CODEC interface
(6) External memory interface
(7) Read/write to dither memory and uniformity correction memory
(8) Image scale down and $\overline{\text{PTIM}}$ signal
(9) Reset
(10) Image quality control using registers

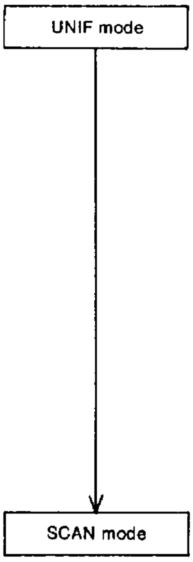
(1) Operating mode

The M66333 performs three basic operations.

- Peak value detection : The peak value of the analog signal output from the recommended analog signal processing circuits shown in Figures 20 to 23 is matched to the white basic supply voltage (V_{WL}) of the M66333 internal A-D converter.
- Uniformity correction data creation : White reference data is created for sensor unit uniformity correction and written to the correction memory.
- Read operation : A document is read and the image is processed to output bi-level data as serial or parallel output.

These three basic operations are performed in the following sequence depending on whether the sensor is CCD or CIS. The sensor is selected with register 0 (SENS).

When the sensor is CCD



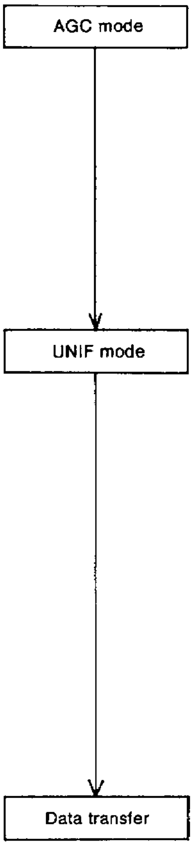
Operation is started by setting the UNIF command in register 0 to "H". If the sensor is CCD, peak detection (16 line period) and white uniformity correction data creation (8 line period) are performed consecutively.

To exit this operating mode, wait 30 line periods (at least 24 lines) from the start and set the UNIF command to "L".

The read operation is started by setting the SCAN command in register 0 to "H". Set the SCAN command to "L" to exit this operating mode.

When the sensor is CIS

(Creation and transmission of uniformity correction data)

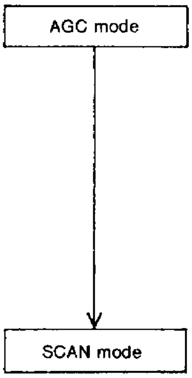


Peak detection is performed for 16 line periods when the AGC command in register 0 is set to "H".
To exit this operating mode, wait 20 line periods (at least 16 lines) from the start and set the AGC command to "L".

This mode is started when the UNIF command in register 0 is set to "H".
When the sensor is CIS, if black correction and white correction are both started with the UNIF command, uniformity correction data creation (8 line period) is started for each correction.
To exit this operating mode, wait 10 line periods (at least 8 lines) from the start and set the UNIF command to "L".

The black and white uniformity correction data created in UNIF mode are transferred to the back-up memory.

(Read opration)

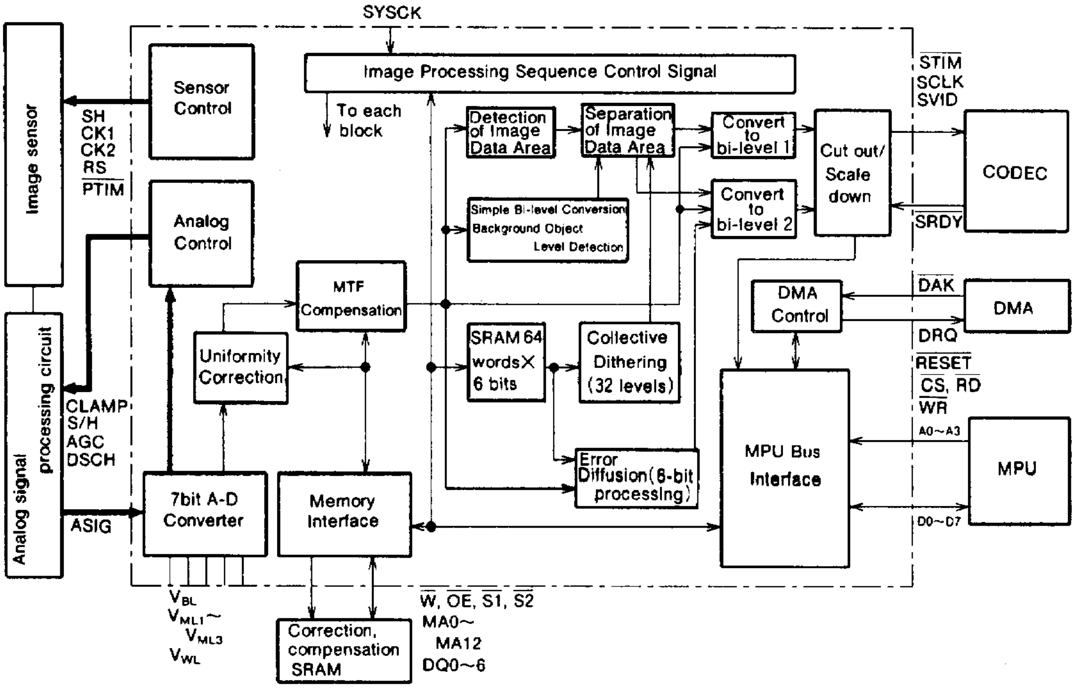


Peak detection is performed for 16 line periods when the AGC command in register 0 is set to "H".
To exit this operating mode, wait 20 line periods (at least 16 lines) from the start and set the AGC command to "L".

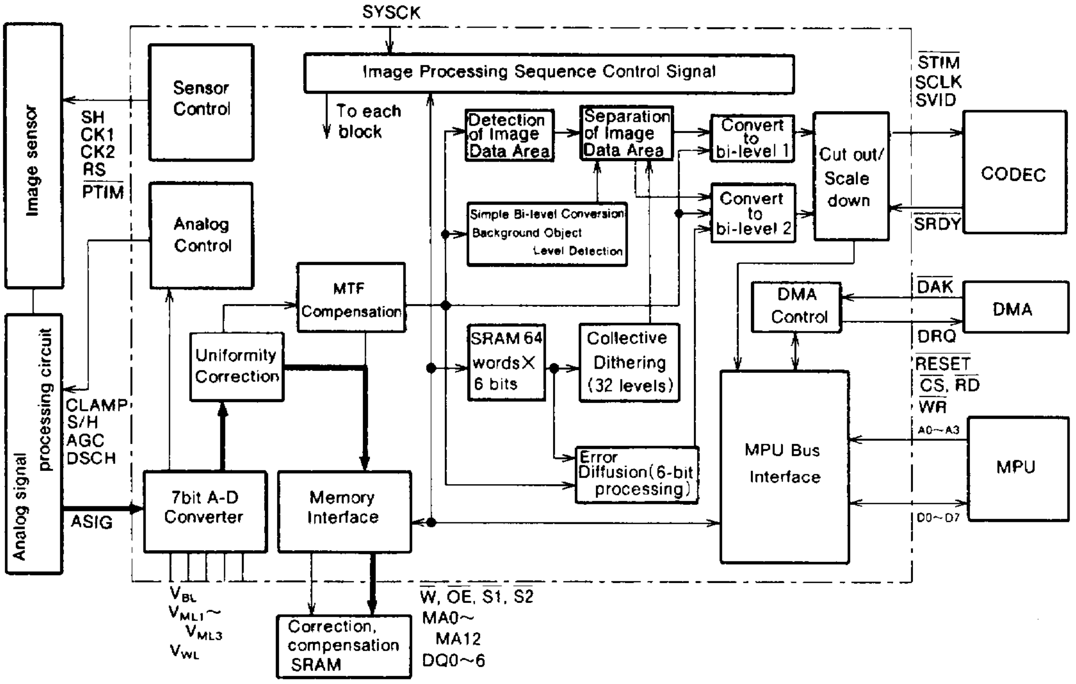
The read operation is started by setting the SCAN command in register 0 to "H". Set the SCAN command to "L" to exit this operating mode.

The signal functions and data flow in each mode are shown on pages 4-167 and 4-168. Flowcharts are shown on pages 4-207 to 4-209.

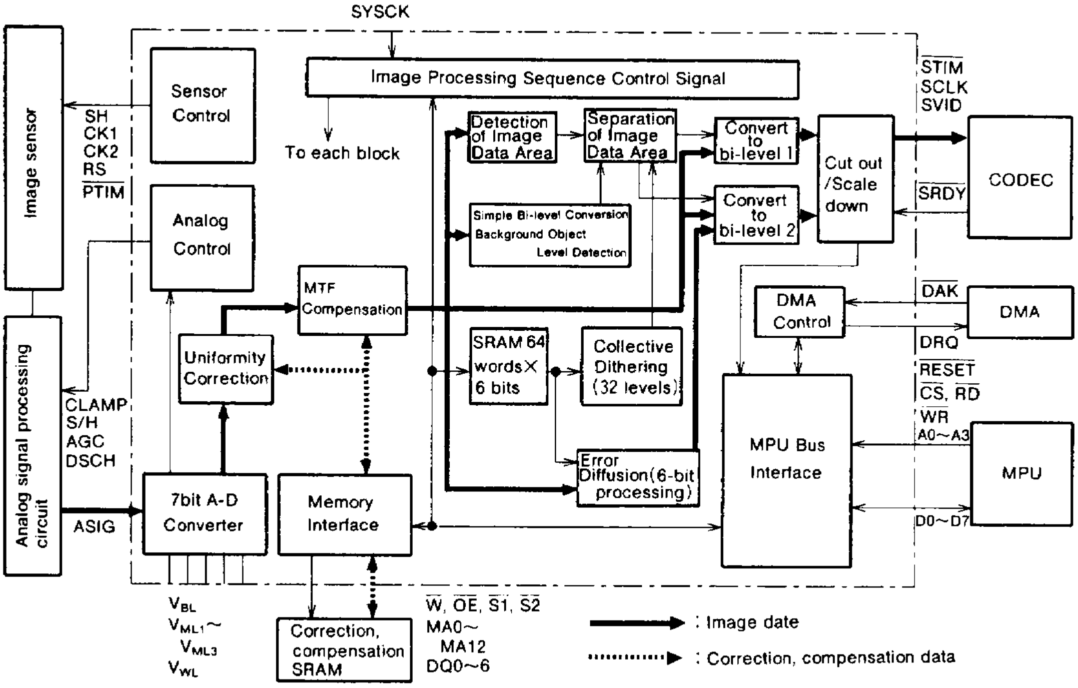
Operation During Peak Detection



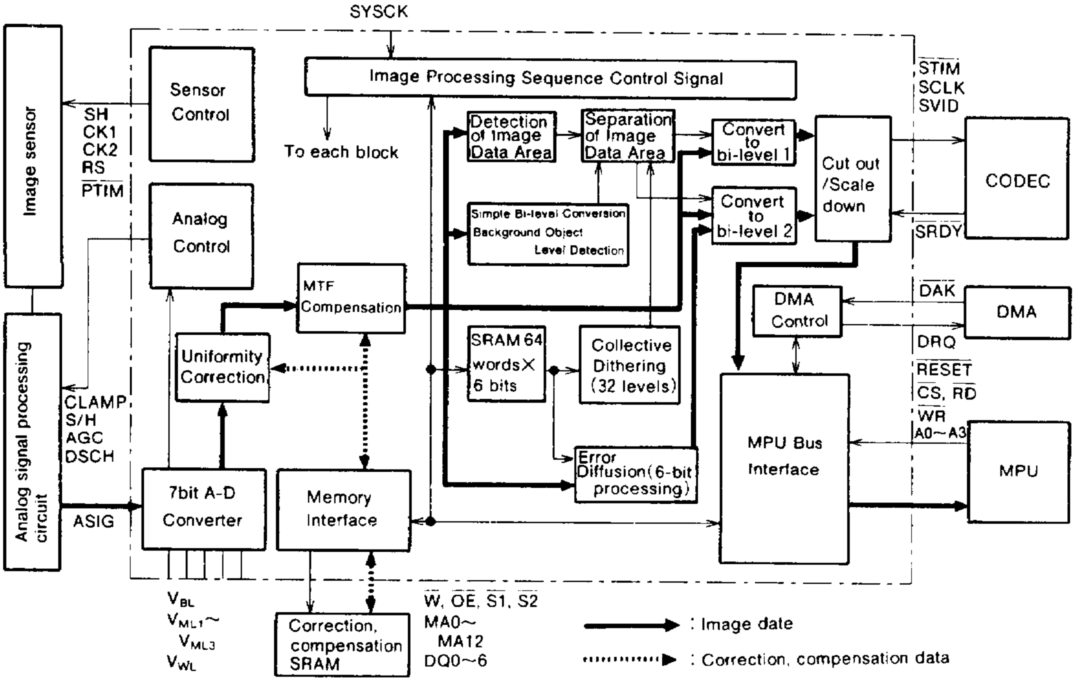
Operation During Peak Detection



Data Flow During Read Operation (for serial output)



Data Flow During Read Operation (for parallel output)



(2) Line period and read sequence

Figure 1 shows the relationship between the M66333 line period and the read sequence.

Figure 2 shows the relationship between the CODEC interface and the read sequence.

- 1 line period (1/ACCK) : Defines the processing time per line for M66333. The line period is determined from the line period counter registers 3 and 4 (PRE_DATA) and pixel transmission clock (ADCK). ADCK is 1/16th of SYSCK.

  1 line period (1/ACCK) [NS]
  =line period counter×pixel transmission clock period [NS]
  =(PRE_DATA+1)×1/ADCK [NS]
  =(PRE_DATA+1)×16/SYSCK [NS]

  The line period counter is counted down with the pixel transmission clock after after loading the PRE_DATA value and generates the following addresses.
- Sensor start pulse (SH) : Image sensor start pulse. The position of the start pulse is determined by the value in register 5 (ST_PL) which is the offset from the uniformity correction range (UNIFG).

  Set ST_PL to the following values according to the type of image sensor.
  CCD : ST_PL=sensor dummy pixel+2
  CIS : ST_PL=2
- Uniformity correction range (UNIFG) : Defines the uniformity correction range. This range corresponds to the sensor width (A3 to A4).

  Refer to Table 2 for the relationship between sensor width and uniformity correction range.
- AGC range (AGCG) : Defines the peak detection range. This range corresponds to the sensor width (A3 to A4).

  Auto gain control is performed for the entire width (solid line) of the sensor in AGC mode and for the range inside the sensor width (dotted line) in SCAN mode.

  Refer to Table 2 for the relationship between sensor width and AGC range.
- Source document read width : Defines the source document read width. If the document width is less than the sensor width, the document should be centered on the sensor because the read range is set from the center of the sensor.

  Refer to Table 3 for the relationship between sensor width and source document read width.
- Pulse motor control signal ($\overline{\text{PTIM}}$) : Generates the pulse motor control signals for the read roller.

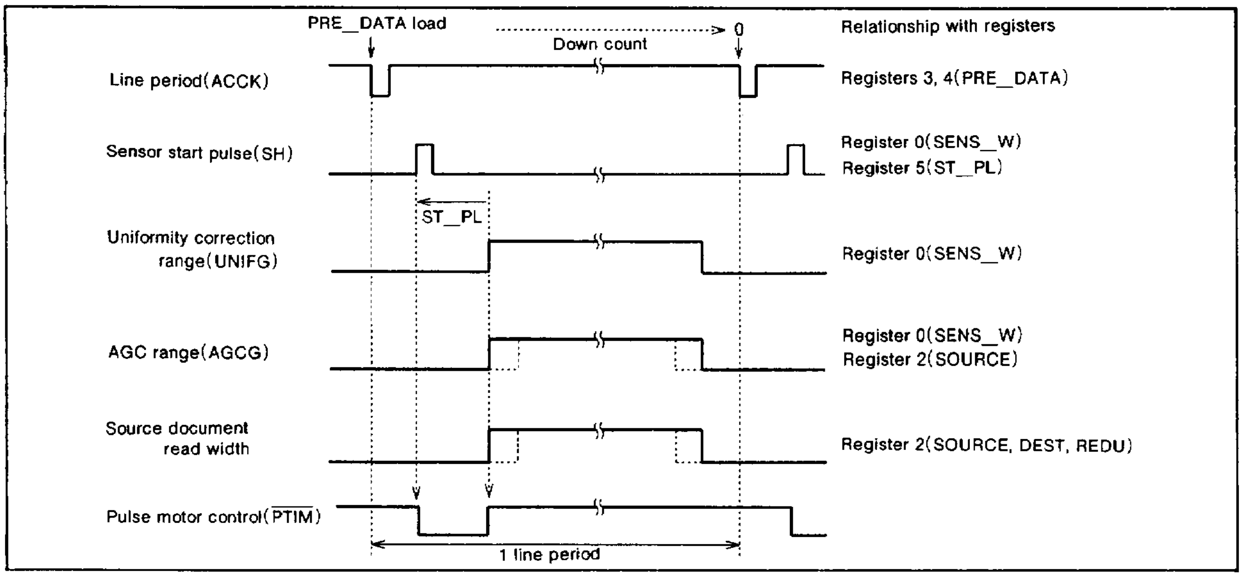


Fig. 1 Line period and read sequence

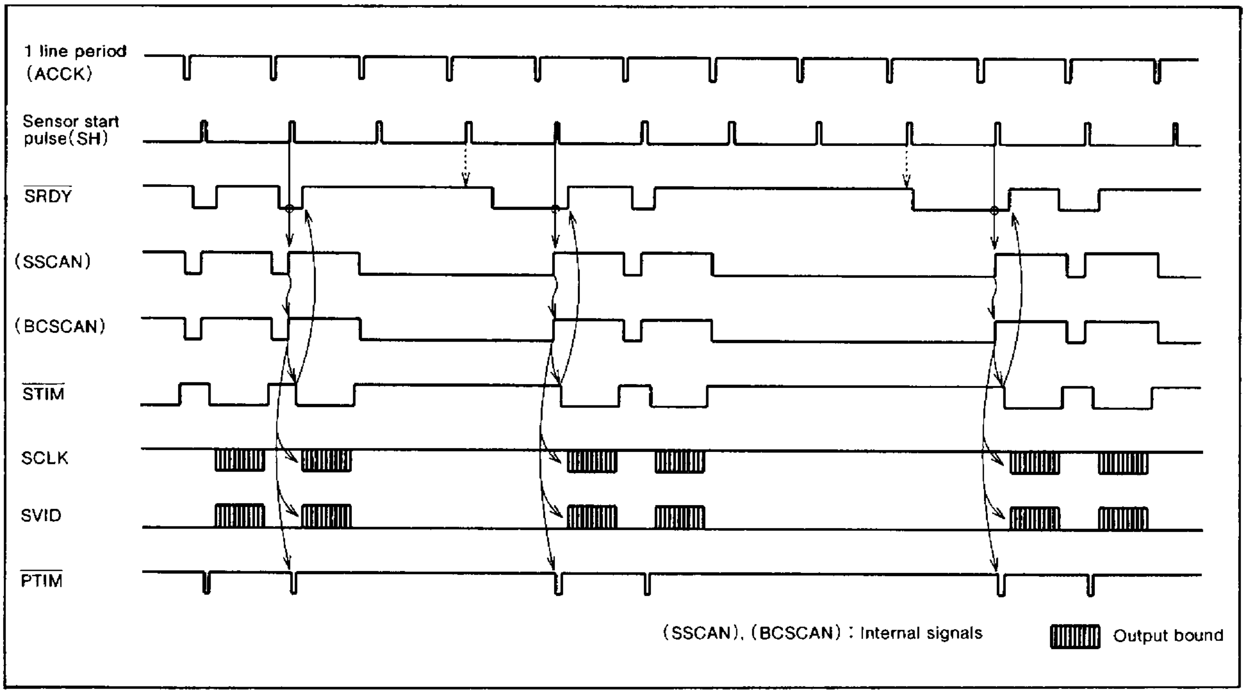


Fig. 2 CODEC Interface and read sequence

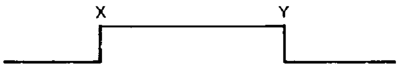
Table 2 Sensor width and gate signal range

Sensor width Gate signal		A3	B4	A4
Uniformity correction range (UNIFG)		2487/55	2279/231	2119/391
AGC range (AGCG)	AGC mode	2487/55	2279/231	2119/391
	SCAN mode	2370/162	2194/306	1760/740

Table 3 Source document read width according to sensor width and source document size

Sensor width Source document size	A3	B4	A4
A3	2487/55	—	—
B4	2278/230	2278/230	—
A4	2118/390	2118/390	2118/390

X/Y
X : Left end address
Y : Right end address



(3) Image processing function

The M66333 converts image signals from the image sensor to bi-level signals. Bi-level conversion can be either simple bi-level conversion or pseudo half-tone conversion which converts image shades into bi-levels.

The signal output from the image sensor must be corrected and compensated to reduce distortion and degradation before it can be converted to bi-level signals.

Furthermore, separation of image data area must be performed to reduce transmission time and perform optimum bi-level conversion.

The functions necessary for image processing are described below.

- Peak detection
- Uniformity correction
- γ correction
- MTF compensation
- Background and object level detection (simple bi-level conversion)
- Pseudo half-tone
  Dither method
  Error diffusion
- Separation of image data area
- Image scale down/area specification

● Peak detection

The A-D converter of the M66333 is used with its reference voltages (V_{WL}, V_{BL}) fixed. Normally, V_{WL} is set to Vcc and V_{BL} is set to 0V to keep the dynamic range of the A-D converter wide. Peak detection must be performed for analog signals to match them with the full scale value of the A-D converter before they are input to the A-D converter. Figures 19 to 22 show examples of analog signal processing circuits.

Peak detection is performed by reading white data in AGC mode (one of the three M66333 operating modes).

In AGC mode, 8 line period worth of DSCH signal to raise gain and 16 line period worth of AGC signal to lower gain are generated after AGC command start (register 0 : AGC) as shown in Figure 3.

This changes the gain as shown in Figure 4 .

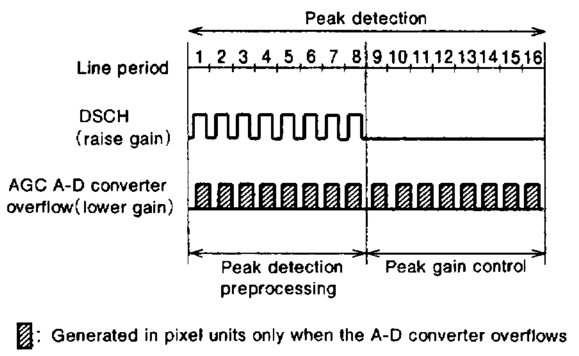


Fig. 3 Peak detection

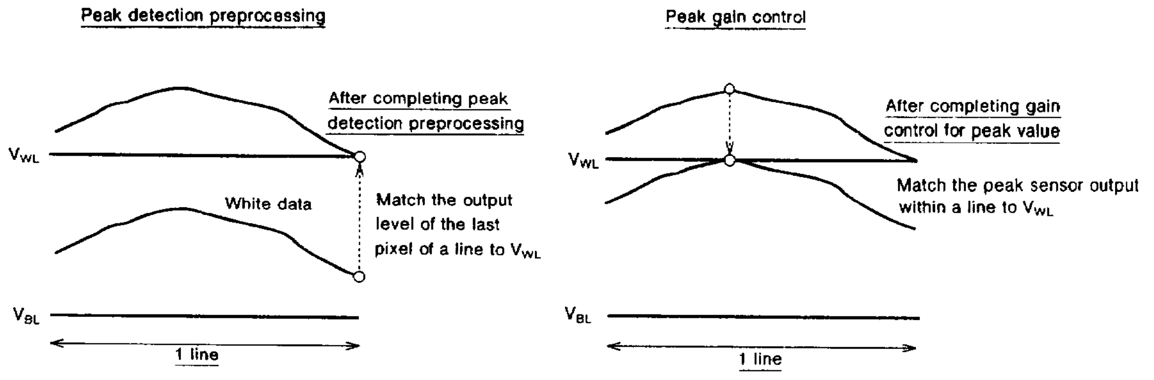


Fig. 4 Change in gain during peak detection

- **Uniformity correction**

Uniformity correction corrects the drop in lighting level at both ends of the light source, shading distortion due to drop in lighting level at the rim of the lens, and high frequency distortion caused by the scattering of pixel-unit image sensor characteristic (see Figure 5).

The M66333 creates uniformity correction data in UNIF mode (one of the three operating modes) and writes it to an external correction memory.

In SCAN mode, the correction data is read from the external correction memory to successively correct the input image data in pixel units.

As shown in Table 4, either white correction only, or both white correction and black correction can be selected.

This selection is made with register 0 (SENS, UMODE) and register 1 (UNIFM).

When performing both black correction and white correction, black correction must be performed first.

The M66333 performs entire pixel correction for 50% correction range as shown in Figure 6.

Correction is not possible if the white correction data exceeds the 50% correction range as shown in Figure 6. Therefore, be sure to keep the input signal within the correction range.

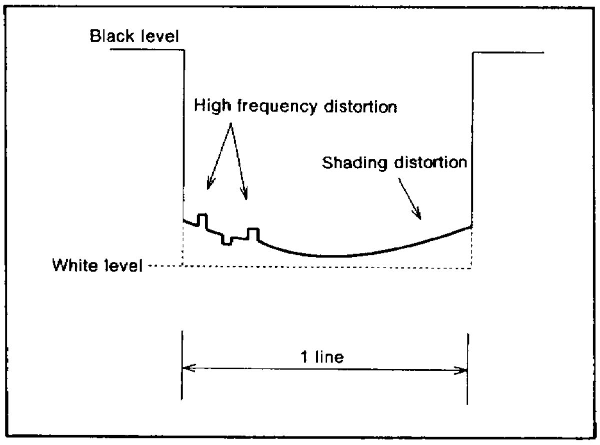


Fig. 5 Image sensor white data output waveform

Table 4 Image sensor uniformity correction

Image Sensor	Correction	Register		
		Sensor Type Register 0 (SENS)	Uniformity Correction Data Creation Register 0 (UMODE)	Correction Mode Selection During SCAN Register 1 (UNIFM)
CCD	White Correction	0	1	–
CIS	White Correction	1	1	0
	Black Correction White Correction	1	Black Correction : 1 White Correction : 0	1

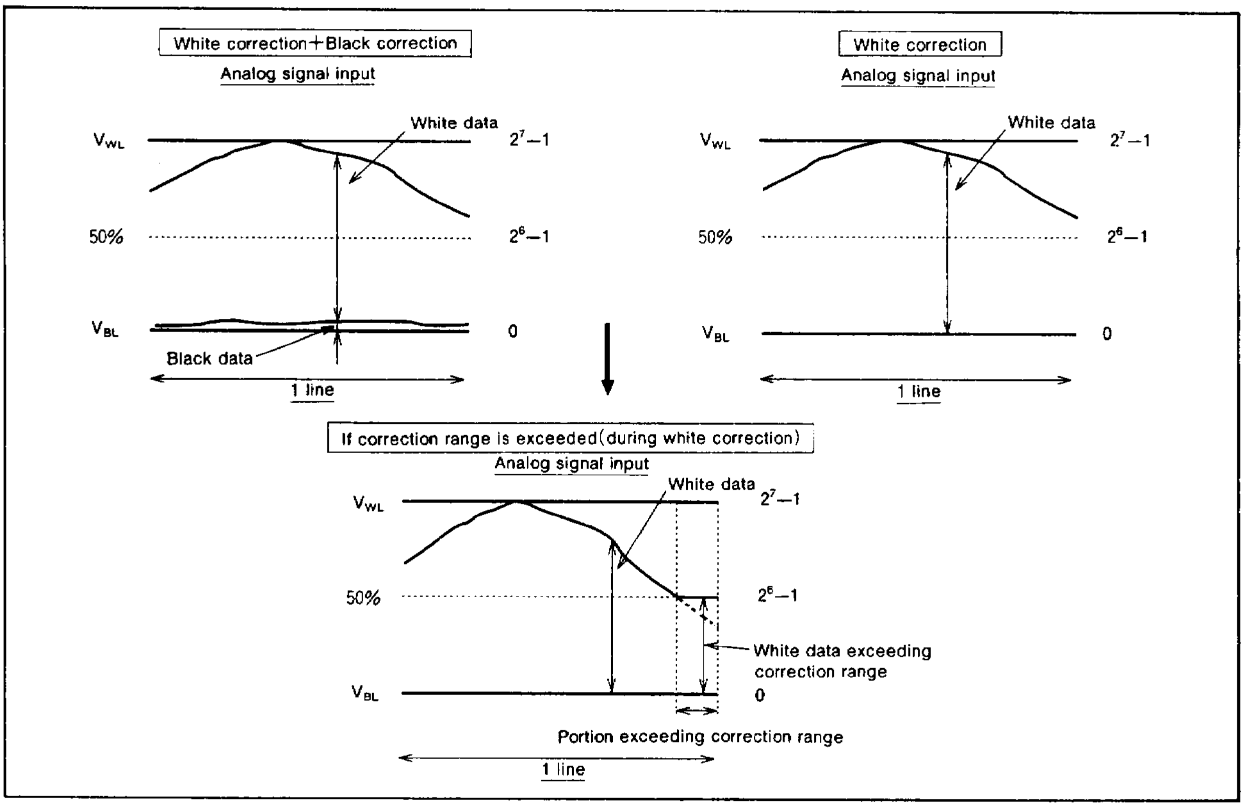


Fig. 6 Uniformity correction

- **γ correction**

γ correction is performed to simulate the sensitivity characteristics of the human eye in order to make the image data more similar to natural image.

The M66333 performs γ correction by externally applying voltage to the middle basic supply voltage pins (V_{ML1}, V_{ML2}, V_{ML3}) of the A-D converter.

γ =0.45 is said to be the optimum γ correction when using a thermal head printer. Figure 7 shows an example of the characteristic when γ =0.45. γ correction approximating γ = 0.45 can be realized by applying V_{ML1} = 0.31V, V_{ML2} = 1.25V, and V_{ML3}=2.50V to the middle basic supply voltage pins of the A-D converter.

γ correction using the middle basic supply voltage pins is performed during error diffusion. γ correction by dither method should be performed using the value to be written in the dither matrix. Refer to the section on dither method for details.

Figure 24 shows an example of a circuit to apply voltage to the middle basic supply voltage pins. This circuit can be used to choose whether to perform γ correction or not according to the operating mode and to perform repeatable bi-level conversion.

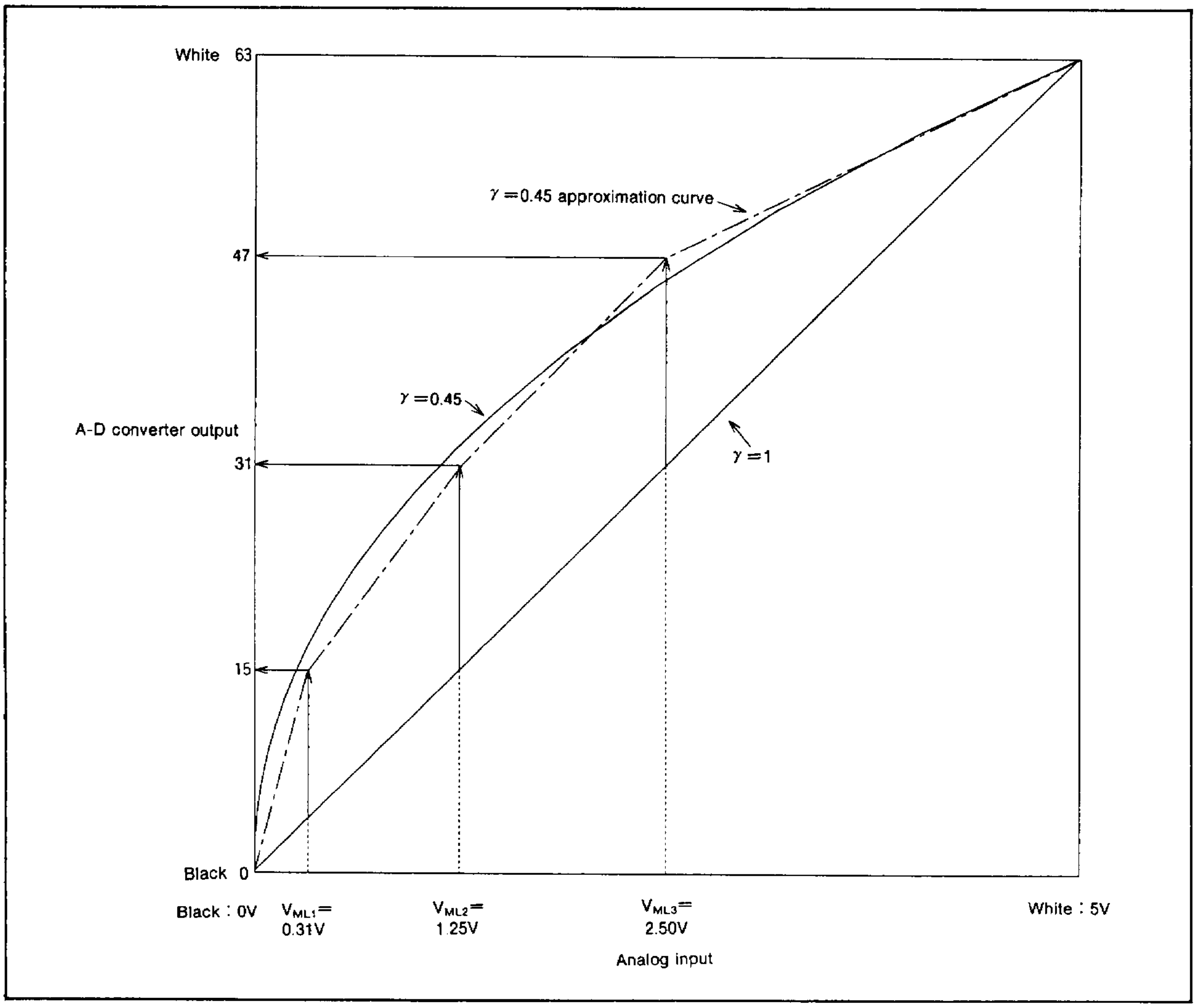
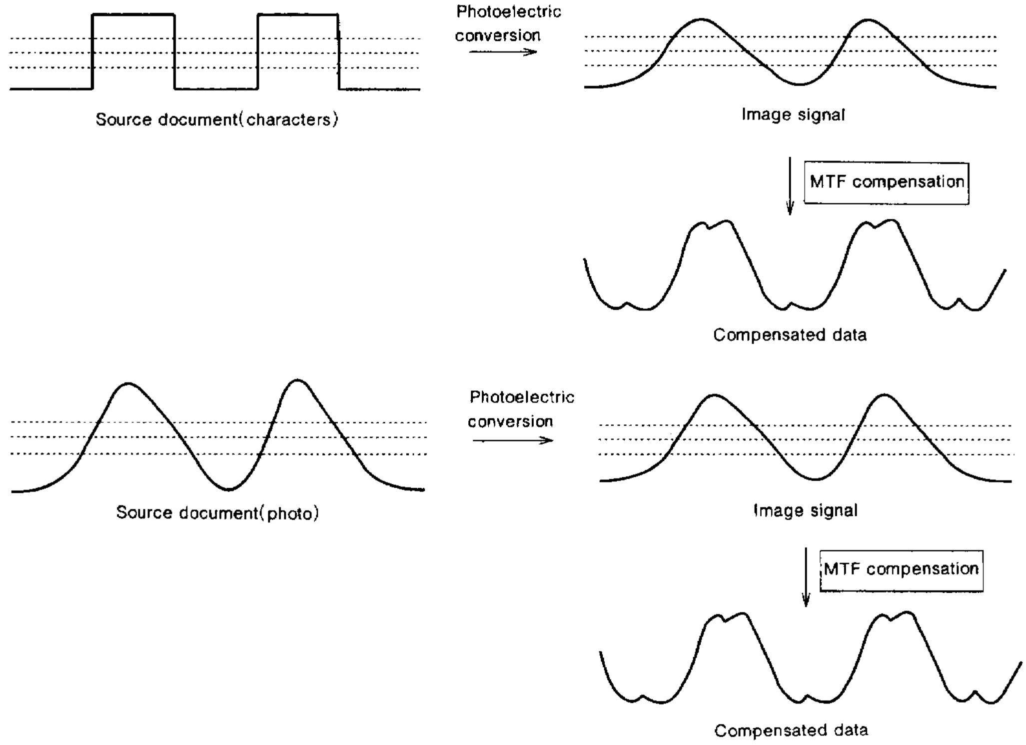


Fig. 7 Example of middle basic supply voltage during γ correction

- **MTF compensation**

As shown in Figure 8 , characters and photos that have been photoelectrically converted by the sensor unit are characterized by a drop in resolution. The MTF compensation performed by the M66333 enhances the high-frequency components with a Laplacian filter to maintain the resolution of the image data and creates a perception of increased dynamic range.

Photoelectric conversion



MTF compensation

$$X' = X + \alpha((X-B)+(X-D)) + \beta((X-A)+(X-C))$$

α : Primary scanning compensation coefficient register 6(MTF_M)
β : Secondary scanning compensation coefficient register 6(MTF_S)

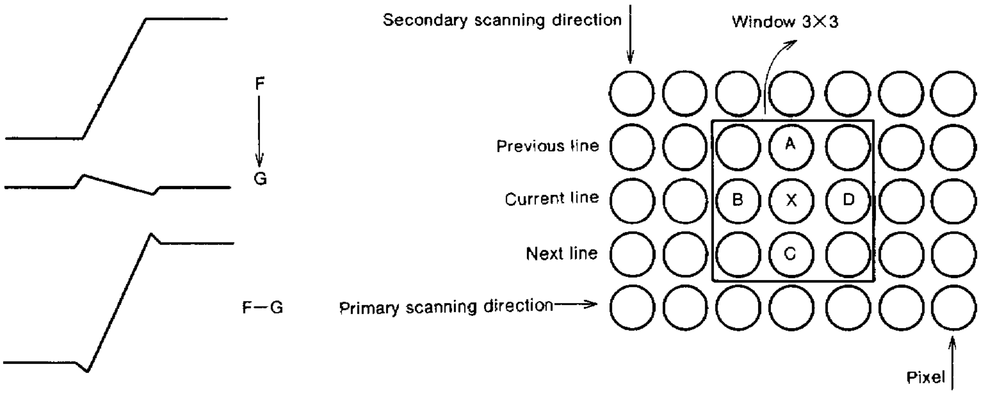


Fig. 8 MTF Compensation

- **Background and object level detection**

The M66333 uses the floating threshold method rather than the fixed threshold method. This method successively generates a threshold for optimum simple bi-level conversion of the target pixel.

Therefore, a threshold matching the picture data is generated without modifying the image data.

This value is used as the threshold of the bi-level area when simple bi-level conversion or image separation is selected as bi-level conversion mode.

: register 6 (MODE)

Background level counter

If an image data greater (brighter) than the current counter value is input, this counter is incremented to approach the image data.

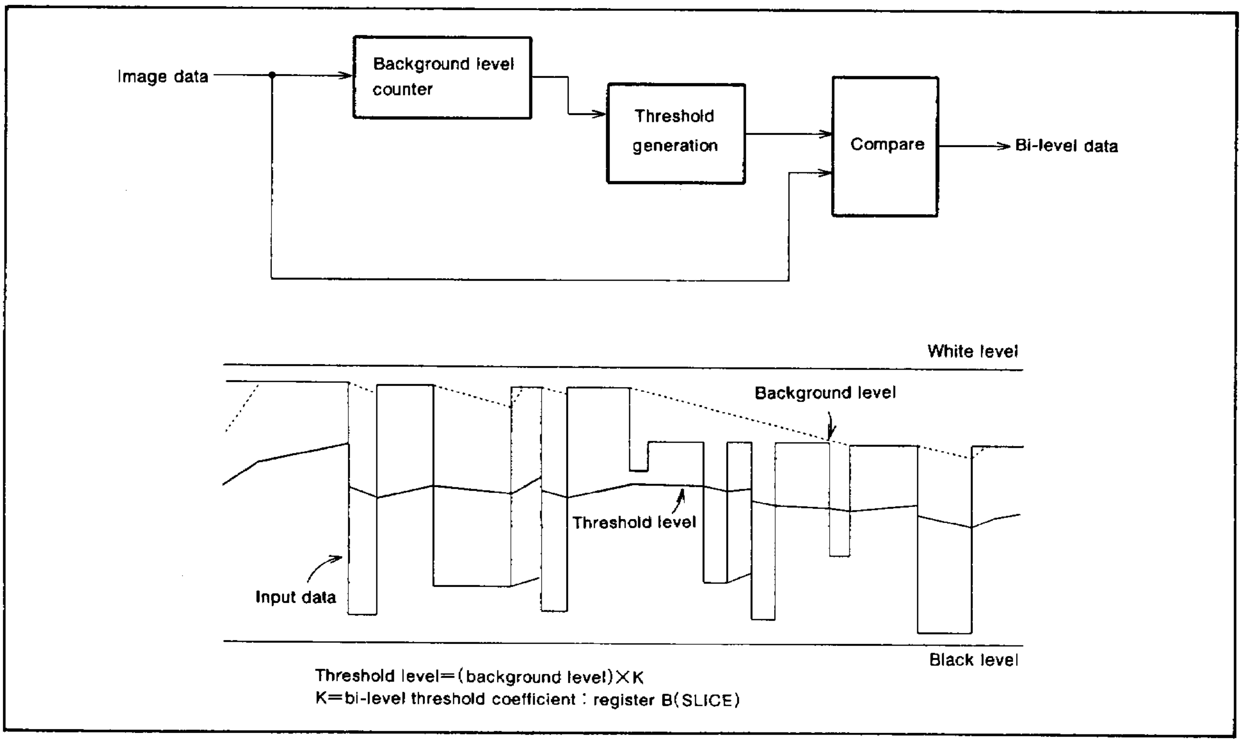
If an image data less (darker) than the current counter value is input, this counter is decremented to approach the image data.

The count up/down speed can be set with the following register.

: register B (MAX_UP, MAX_DOWN)

The lower limit of the background level can be set with the following register.

: register D (LL_MAX)



Threshold level=(background level)×K
K=bi-level threshold coefficient : register B(SLICE)

Fig. 9 Background-object level

- **Dither method**

The M66333 has a built-in 64 words×6 bit SRAM which is used as a collective dithering memory.

During initialization, the dither matrix size is set and then the threshold matching the desired dither pattern is written in the dither memory.

: register 6 (DITH)
: register E (DITH_D)

Figure 10 shows some examples of dither patterns.

Refer to the section on dither memory and uniformity correction memory write/read for details on how to write/read the dither memory.

This is used when dither method, image data area separation, or error diffusion (see section on error diffusion) is selected for bi-level conversion mode during read. : register 6 (MODE)

The matrix size shown in Table 5 is selected for the dither matrix depending on whether the scanning line density is fine or super fine. If the matrix size 8X8 is selected for super fine, the 4X8 dither pattern shown in Figure 11 is repeated.

4X4 matrix sequence (fine)

0	8	2	10
12	4	14	6
3	11	1	9
15	7	13	5

a) Diffused type

4	10	5	11
15	0	2	6
9	3	1	12
14	8	13	7

b) Concentrated type

11	4	6	9
12	0	2	14
7	8	10	5
3	15	13	1

c) Mesh type

4X8 matrix example (super fine)

0	16	4	20
24	8	28	12
6	22	2	18
30	14	26	10
1	17	5	21
25	9	29	13
7	23	3	19
31	15	27	11

a) Diffused type

8	20	10	22
30	0	4	12
18	6	2	24
28	16	26	14
9	21	11	23
31	1	5	13
19	7	3	25
29	17	27	15

b) Concentrated type

22	8	12	18
24	0	4	28
14	16	20	10
6	30	26	2
23	9	13	19
25	1	5	29
15	17	21	11
7	31	27	3

c) Mesh type

Fig. 10 Collective dithered pattern

Table 5 Scanning line density and dither matrix size

Scanning Line Density	Primary/Secondary Scanning Line (lines/mm)	Level	Matrix Size
Normal	8X3.85	—	—
Fine	8X7.7	16	4X4
Super Fine	8X15.4	32	4X8, 8X8

0	16	4	20	11	27	15	31
24	8	28	12	19	3	23	7
6	22	2	18	13	29	9	25
30	14	26	10	21	5	17	1
1	17	5	21	10	26	14	30
25	9	29	13	18	2	22	6
7	23	3	19	12	28	8	24
31	15	27	11	20	4	16	0

Fig. 11 8X8 Matrix dither pattern example (diffused type)

If dither method is used to perform pseudo half-tone, γ correction with the middle basic supply voltage pin of the A-D converter is not used. Instead, the γ characteristic is applied to the threshold value to be written in the dither matrix to perform γ correction. This method is shown in Figure 12.

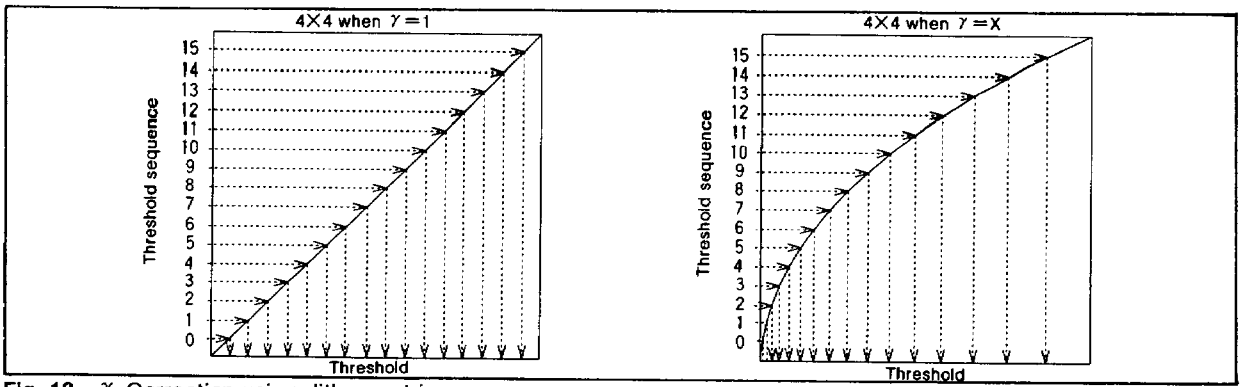


Fig. 12 γ Correction using dither matrix

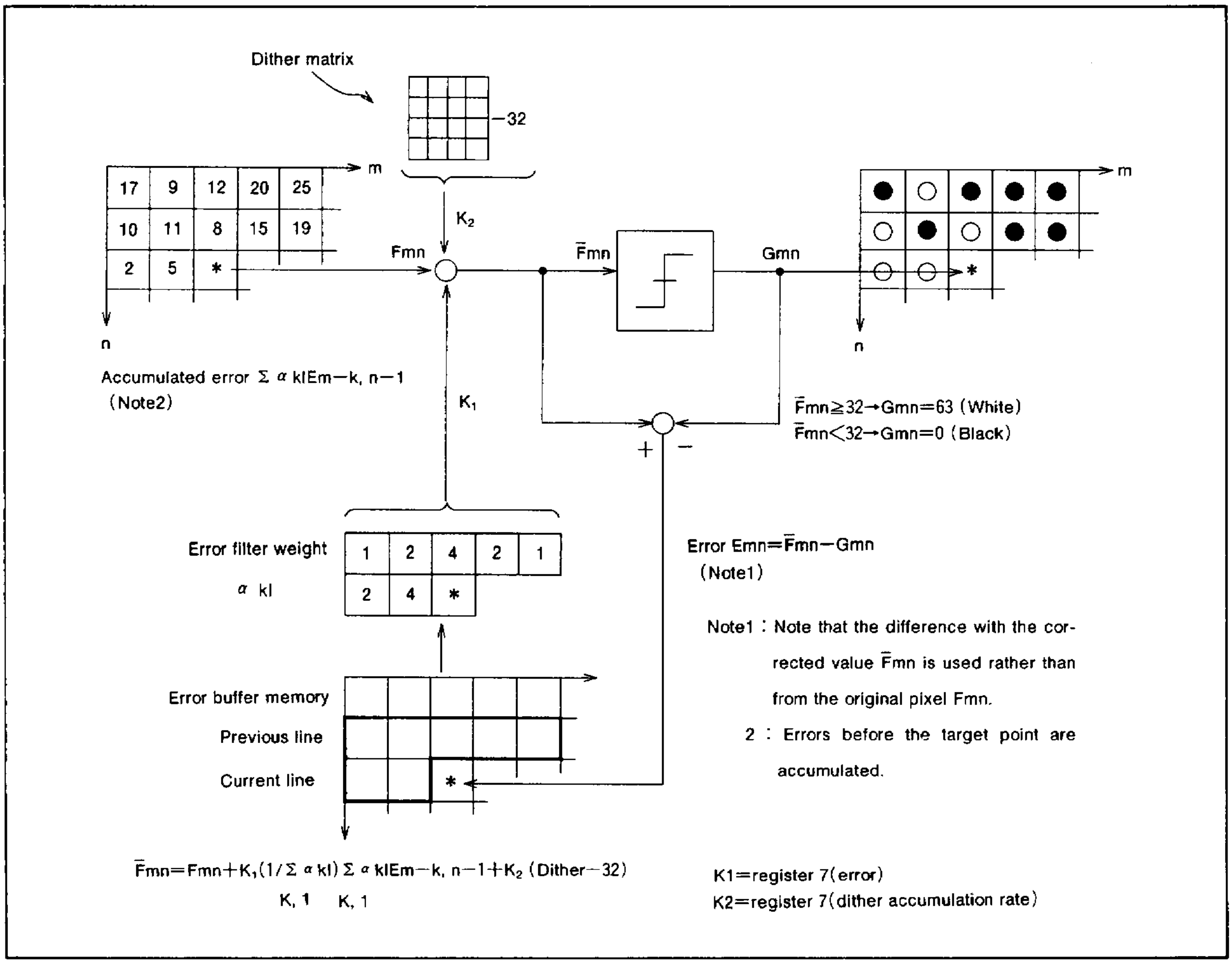
- **Error diffusion**

Error diffusion method, which is a type of conditional identification method, locally diffuses the density error between the source and the result to obtain a close approximation. This produces pictures with balanced gradation and resolution.

This is performed by selecting error diffusion during bi-level conversion mode selection. : register 6 (MODE)

Error diffusion adds dither in addition to image data density error. In this case, the dither matrix data is shared. : register 7 (ERROR)

γ correction must be performed when performing error diffusion.



Note1 : Note that the difference with the corrected value $\bar{F}mn$ is used rather than from the original pixel Fmn.

2 : Errors before the target point are accumulated.

$$\bar{F}mn=Fmn+K_1(1/\sum_{K,1}\alpha kl)\sum_{K,1}\alpha klEm-k,\,n-1+K_2\,(Dither-32)$$

K1=register 7(error)
K2=register 7(dither accumulation rate)

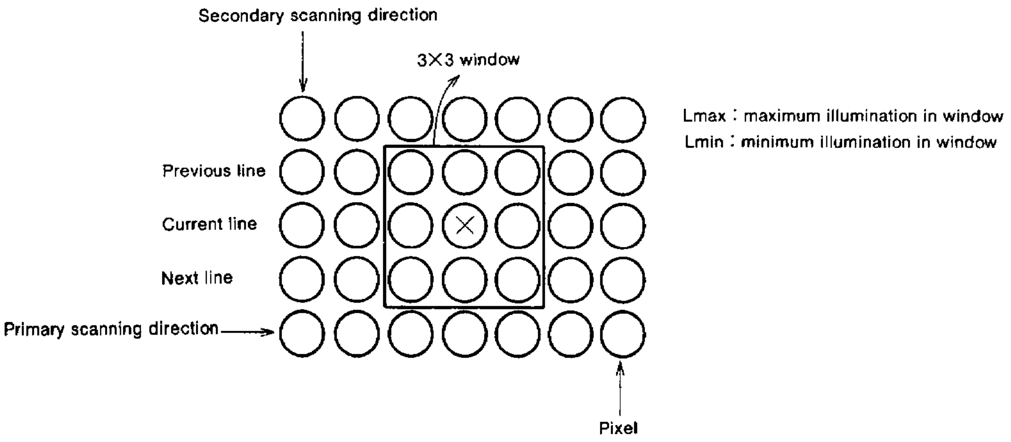
Fig. 13 Error diffusion method

- **Separation of image data area**

In order to perform bi-level conversion appropriate for the image, a black and white image is separated into bi-level conversion area and gradation conversion area. Simple bi-level conversion is applied to the bi-level conversion area and dither method is applied to the gradation area.
: register 2 (MODE)

	Area	Process	Example
Black and white image	Bi-level conversion area	Simple bi-level conversion	Character
	Gradation conversion area	Pseudo half-tone conversion	Photo

There is no significant change in illumination of the gradation conversion area (photo)when a black and white image is viewed through a 3X3 window. This characteristic is used to distinguish between gradation conversion area and bi-level conversion area.



Lmax : maximum illumination in window
Lmin : minimum illumination in window

Identification equation 1 Lmax-Lmin>A(illumination difference in bi-level conversion area) : register 8 difference(SEPA_A)

Identification equation 2 Lmin>B(area is entirely white) : register 9 minimum(SEPA_B)

Identification equation 3 Lmax<C(area is entirely black) : register A maximum(SEPA_C)

Simple bi-level conversion if identification equation 1, 2, or 3 is satisfied.

Pseudo half-tone conversion when none of the identification equations is satisfied.

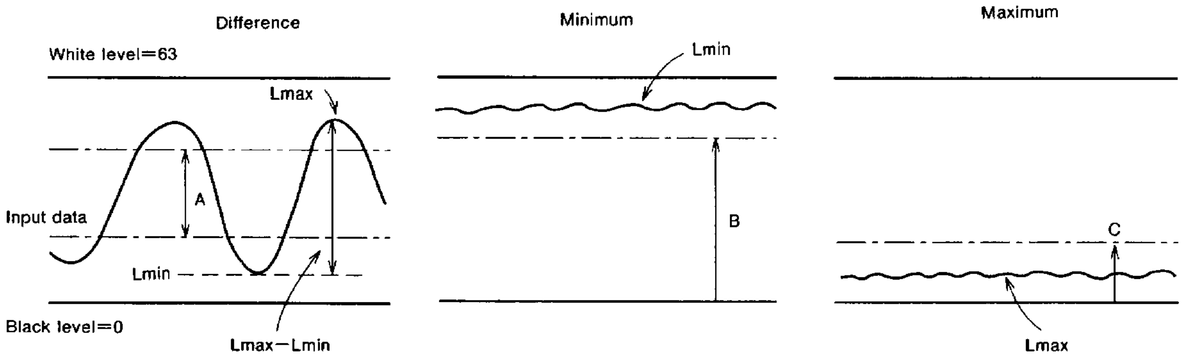


Fig. 14 Separation of image data area

- **Image scale down/area specification**

Scale down funcion

The image data input from the analog signal processing circuit can be scaled down (A3→B4, A3→A4, B4→A4) by leaving out pixels in the primary scanning direction for bi-level conversion. : register 2 (SOURCE, DEST, REDU)

Scale down in secondary scanning direction can be performed either by controlling the read roller pulse motor according to the $\overline{\text{PTIM}}$ signal (with scaling) or by leaving it up to the MPU (without scaling) . : register C (REDM)

With scaling in secondary scanning direction	: The image data to be left out is read by the M66333, but is not output.
Without scaling in secondary scanning direction	: No image data is left out in the secondary scanning direction. Leave the $\overline{\text{PTIM}}$ pin open.

Table 6 Scaling rate

IN / OUT	A3	B4	A4
B4	13/15	1	–
A4	12/17	9/11	1

Area specification function

When area specification is selected, bi-level conversion is performed only in the specified area from the center of the source document. : register 2 (SOURCE, DEST, REDU)

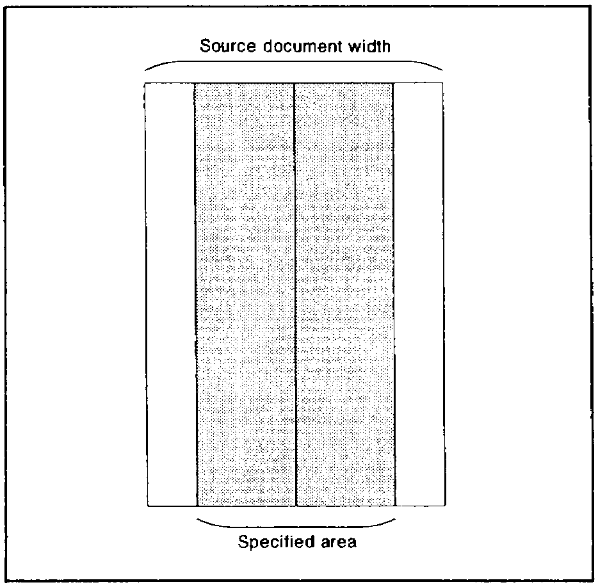
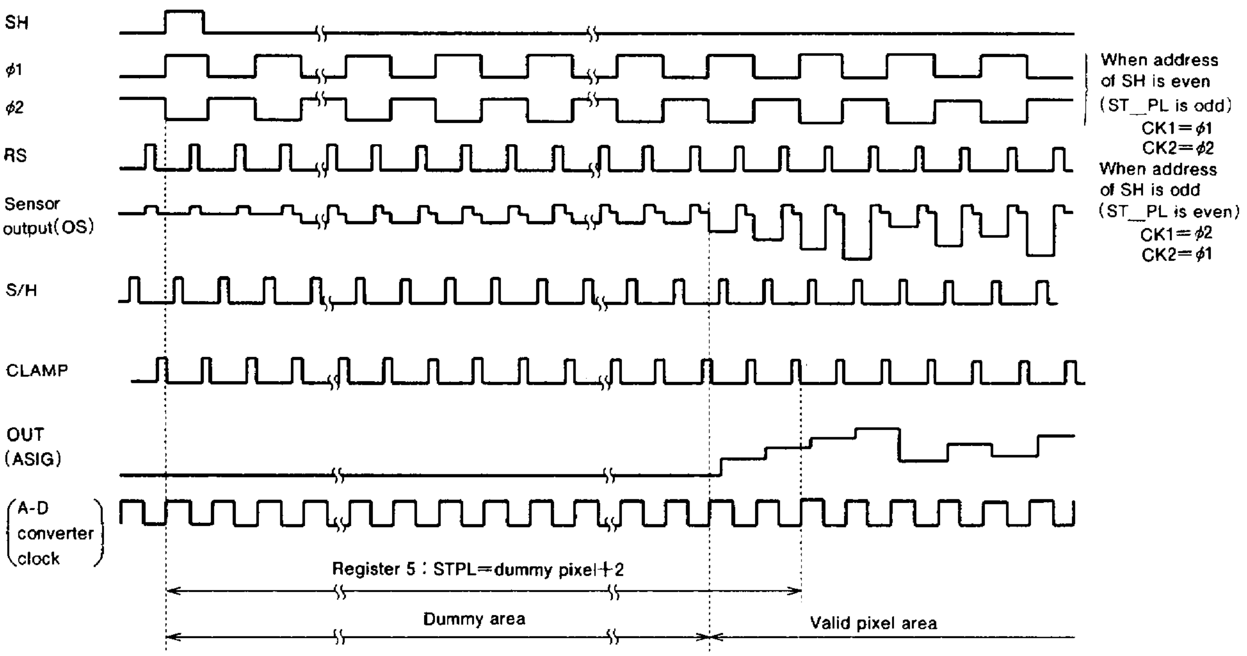
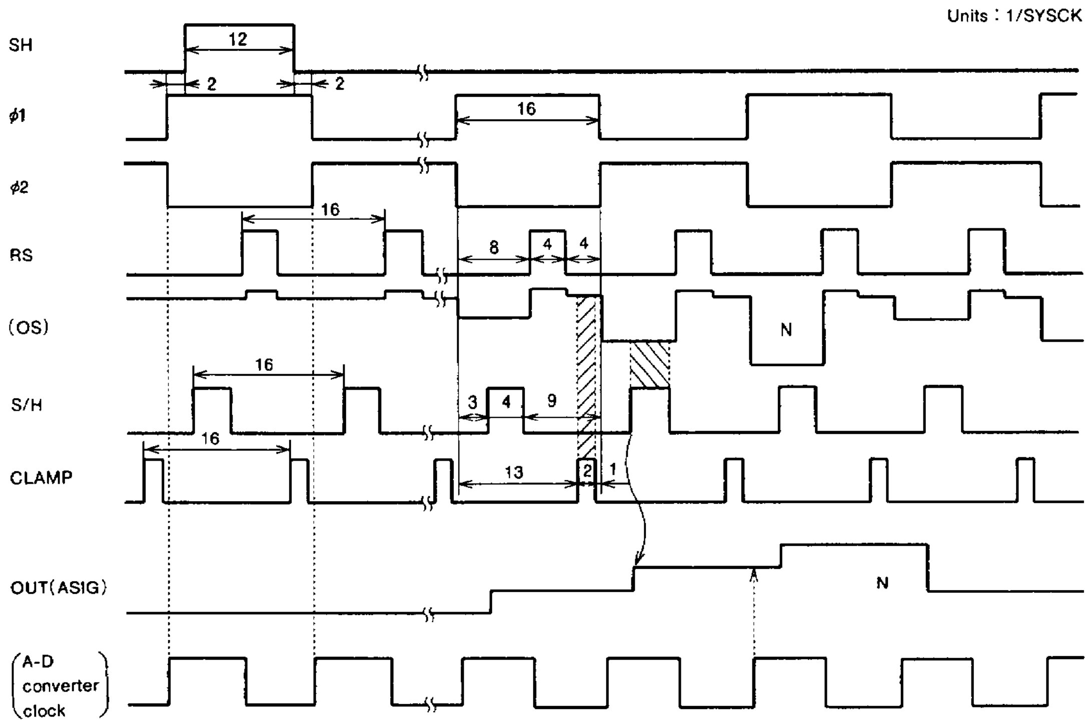


Fig. 15 Cut out function

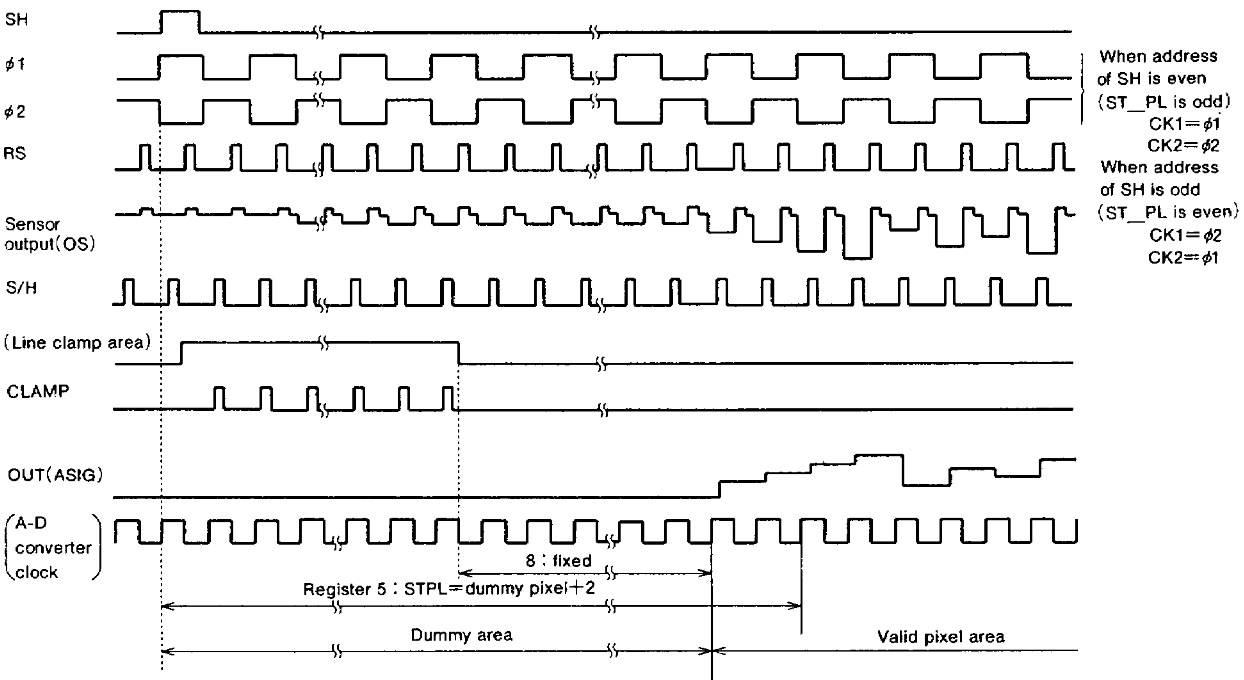
(4) Sensor unit/analog signal processing unit interface

CCD-bit clamp type

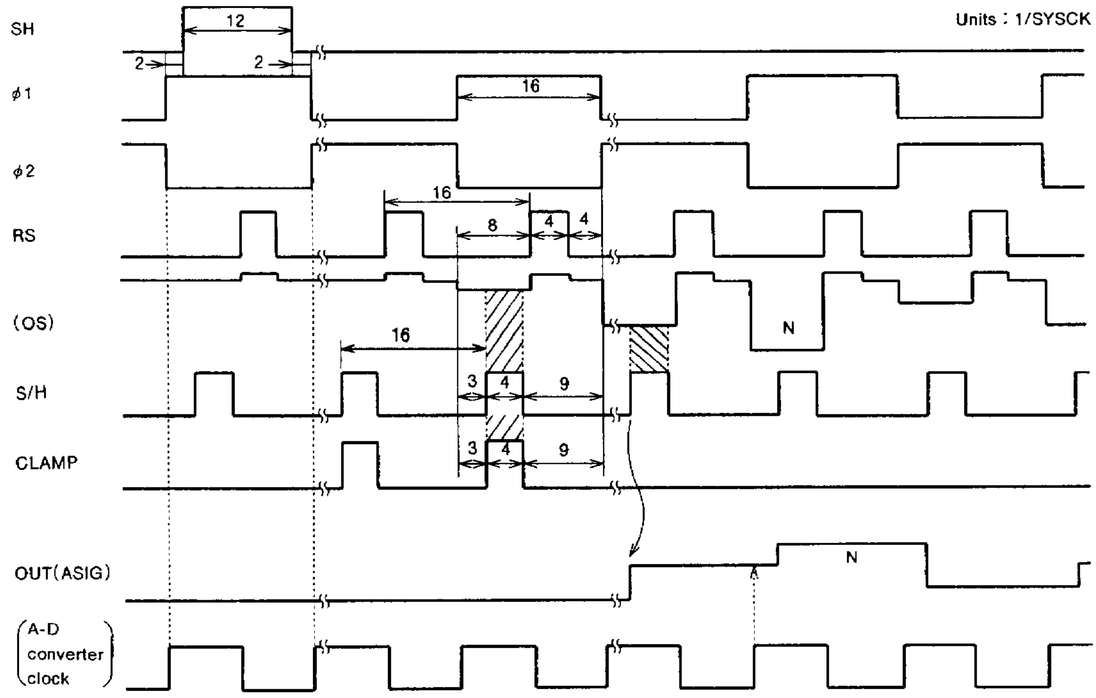




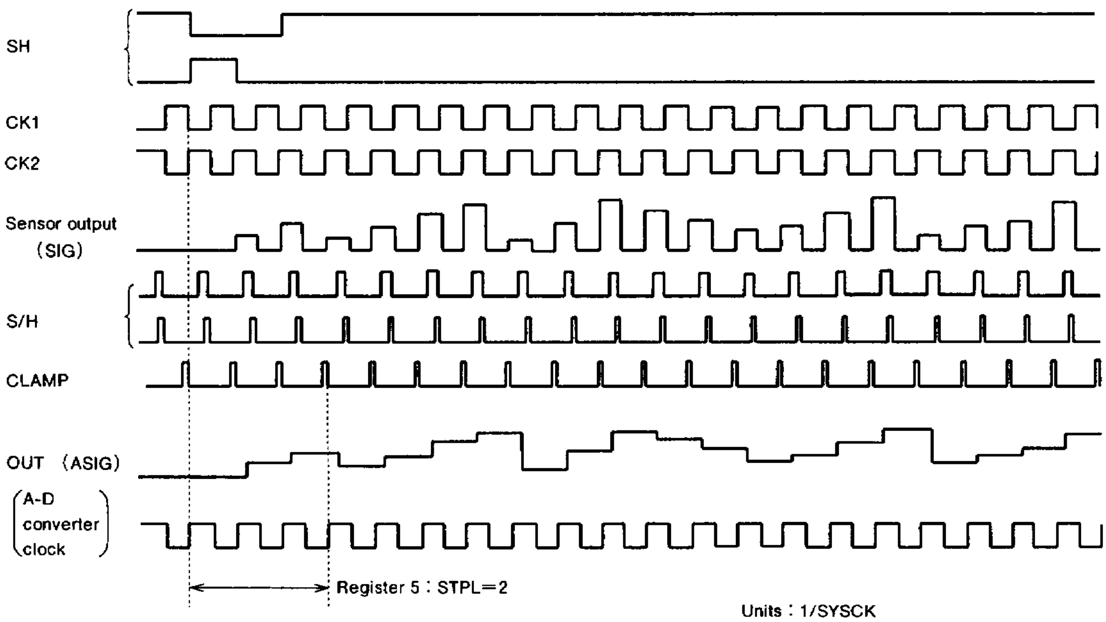
CCD-line clamp type



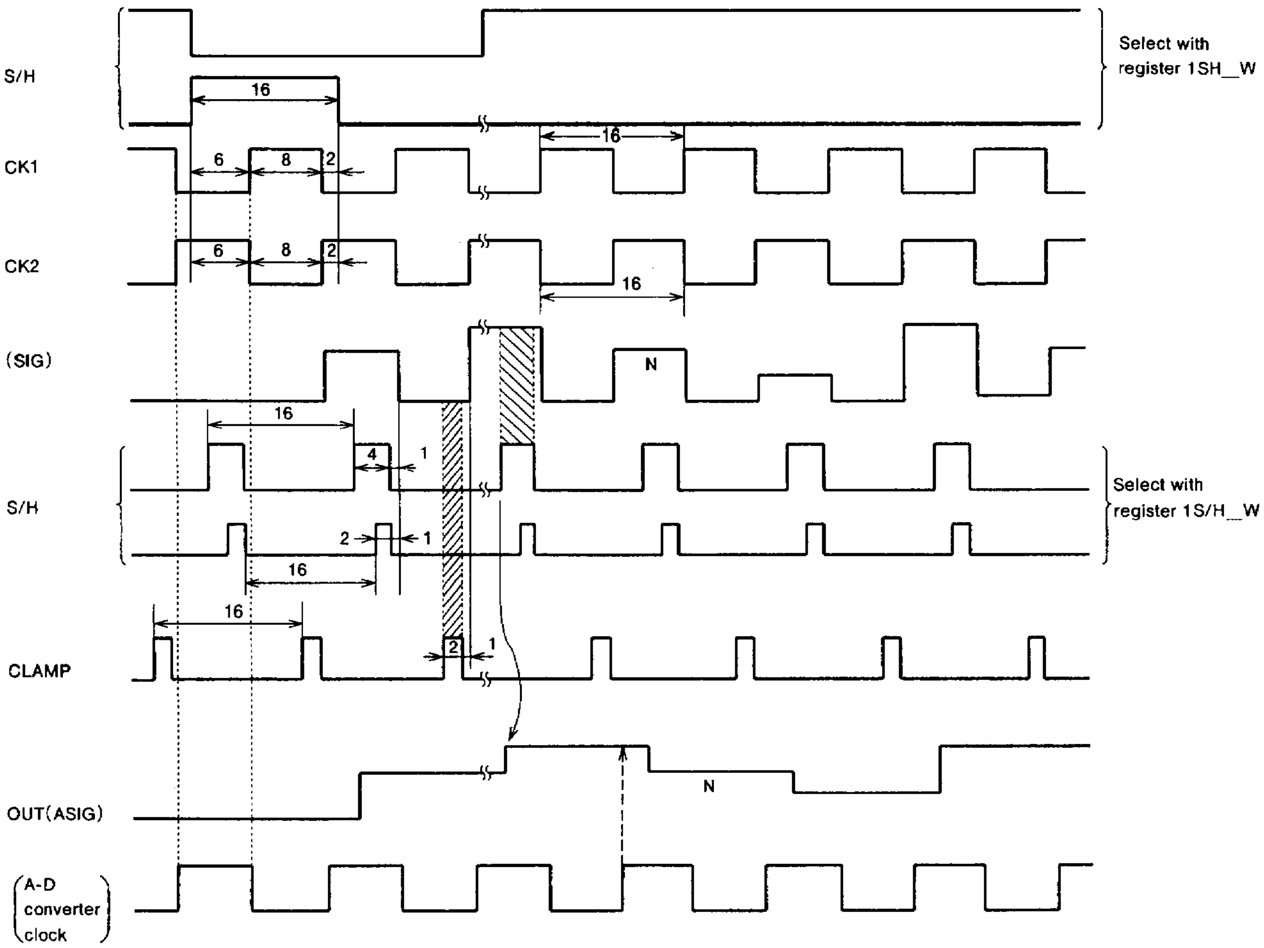
Note : Line clamp uses sensor output equivalent to (dummy area − 8) pixels from the first pixel after SH.



CIS type



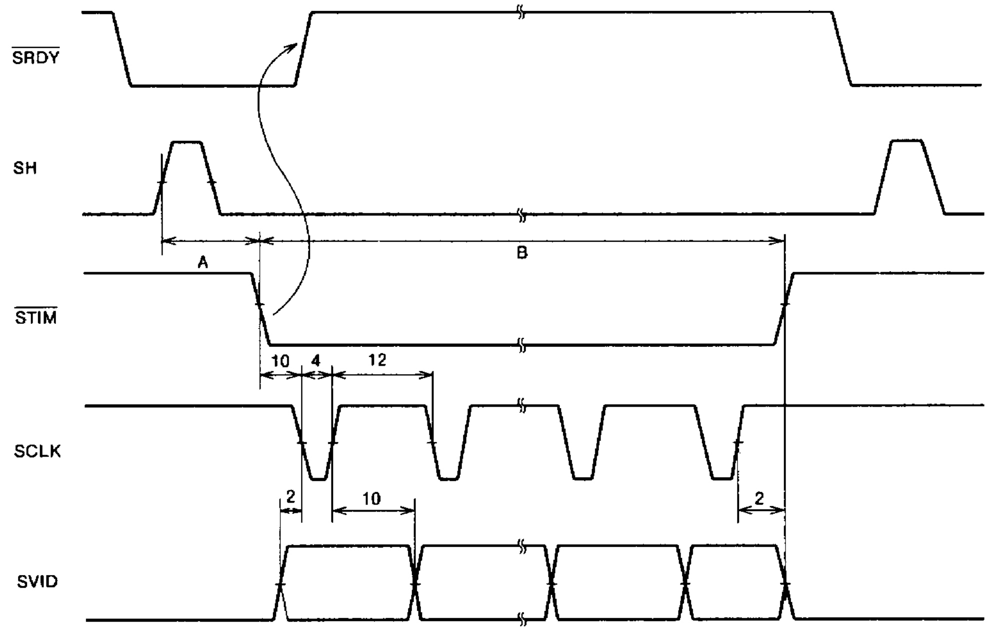
Units : 1/SYSCK



Note : CLAMP : In case of CIS, check with the sensor manufacturer for the use of CLAMP.
SH and CK1, CK2 : SH can be selected with register 1 and CK can be selected with CK1 and CK2(2 selections each)to provide interface to various types of CIS.

(5) CODEC interface

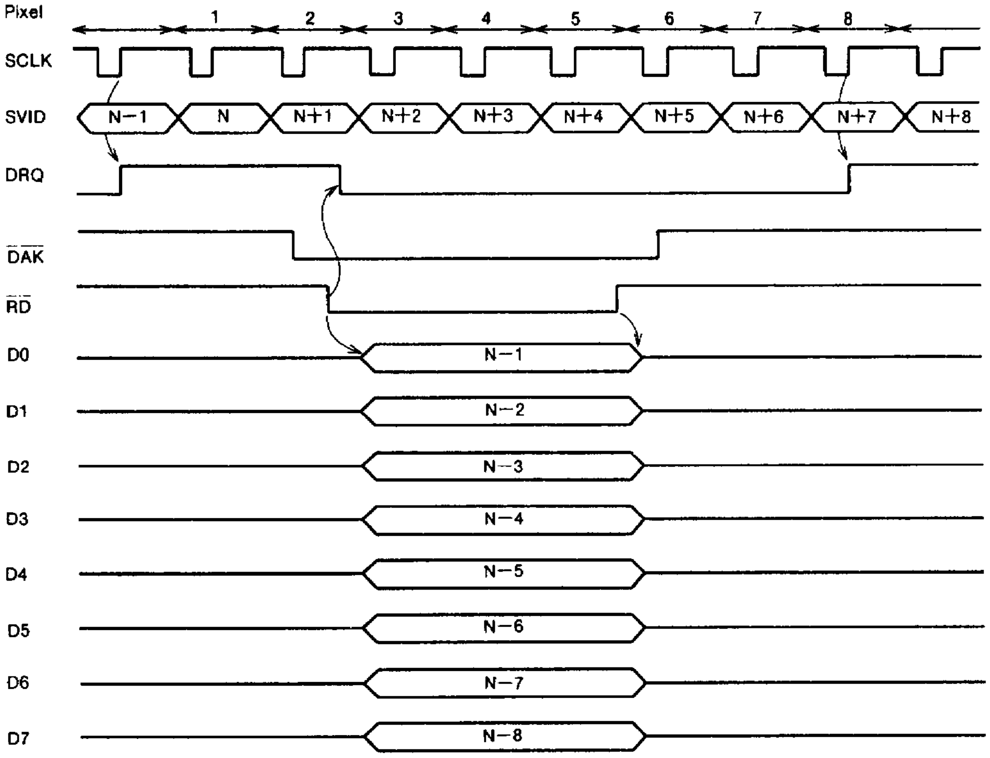
Serial output



Units : 1/SYSCK

Note : A is determined by register 5(ST__PL)and B is determined by register 2(SOURCE, DEST, REDU).

Parallel output



Note : Handshaking of three lines $\overline{\text{SRDY}}$, SH, and $\overline{\text{STIM}}$, which are interface to the CODEC, is the same as serial output.

(6) External memory interface

The pixel transmission period during operation is 16/ SYSCK.

In SCAN mode, 4 to 7 cycle write/read is performed to the external memory during one pixel transmission period in order to read the source document width and perform uniformity correction and error diffusion.

The memory address for each cycle is shown below.

Table 7 Read width in SCAN mode, Memory write/read cycle vs memory address map

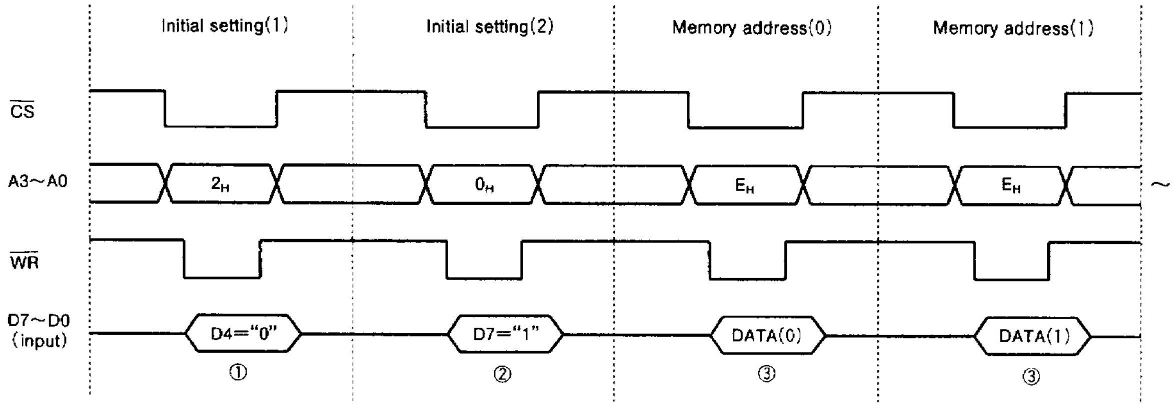
Source document read width			Memory R/W cycle	External memory capacity	Chip select	Uniformity correction memory area		MTF compensation memory area (shared with data image area separation memory area)		Error diffusion memory area
						Black correction	White correction	Current line	Previous line	Error buffer
A3	B4	A4				Address	Address	Address	Address	Address
○	○	○	4 cycles	64KS	$\overline{S2}$	—	$0_H \sim 097F_H$	$0A00_H \sim 137F_H$	$1400_H \sim 1D7F_H$	—
×	○	○	5 cycles	64KS	$\overline{S2}$	$0_H \sim 07FF_H$	$0800_H \sim 0FFF_H$	$1000_H \sim 17FF_H$	$1800_H \sim 1FFF_H$	—
×	○	○	6 cycles	64KS	$\overline{S2}$	—	$0800_H \sim 0FFF_H$	$1000_H \sim 17FF_H$	$1800_H \sim 1FFF_H$	$0_H \sim 07FF_H$
○	○	○		64KS	$\overline{S1}$	—	$0_H \sim 097F_H$	—	—	—
				64KS	$\overline{S2}$	—	—	$0A00_H \sim 137F_H$	$1400_H \sim 1D7F_H$	$0_H \sim 097F_H$
○	○	○		256KS	$\overline{S2}$	—	$0_H \sim 097F_H$	$2A00_H \sim 337F_H$	$3400_H \sim 3D7F_H$	$2000_H \sim 297F_H$
×	○	○	7 cycles	32KR	$\overline{S1}$	$0_H \sim 07FF_H$	$0800_H \sim 0FFF_H$	—	—	—
				64KS	$\overline{S2}$	—	—	$0A00_H \sim 11FF_H$	$1400_H \sim 1BFF_H$	$0_H \sim 07FF_H$
○	○	○		64KS, R	$\overline{S1}$	$0A00_H \sim 137F_H$	$0_H \sim 097F_H$	—	—	—
				64KS	$\overline{S2}$	—	—	$0A00_H \sim 137F_H$	$1400_H \sim 1D7F_H$	$0_H \sim 097F_H$
○	○	○		256KS	$\overline{S2}$	$0A00_H \sim 137F_H$	$0_H \sim 097F_H$	$2A00_H \sim 337F_H$	$3400_H \sim 3D7F_H$	$2000_H \sim 297F_H$

32KR : 32K EPROM
64KR : 64K EPROM
64KS : 64K SRAM
256KS : 256K SRAM

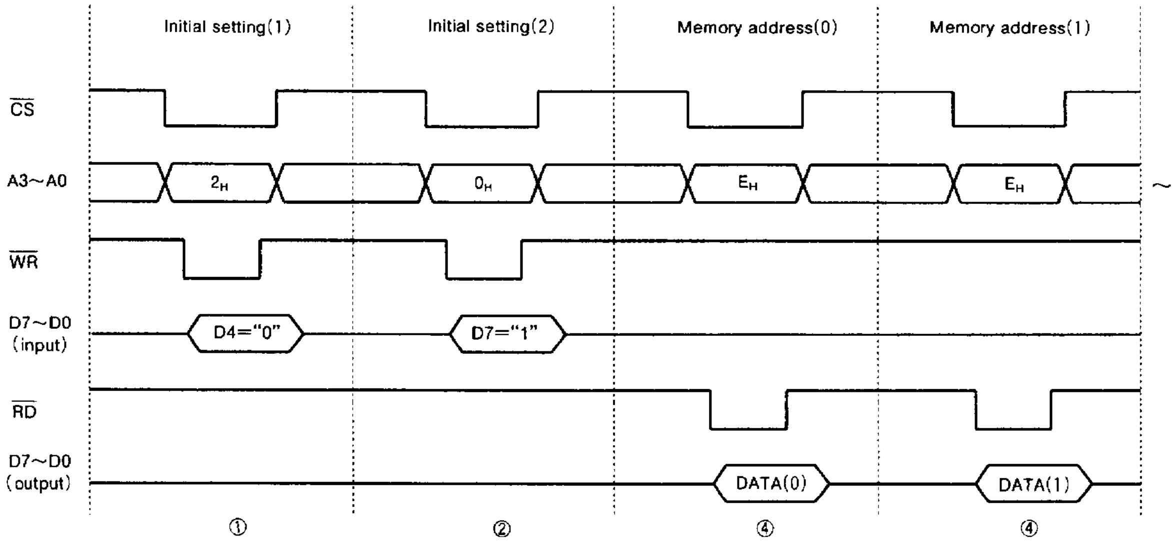
(7) Read/write to dither memory, uniformity correction memory

The following figures show the sequence for writing and reading dither patterns in the 64 words X 6 bit collective dithering SRAM built in the M66333.

Dither memory write (MPU→M66333)



Dither memory read (M66333→MPU)



① Clear D4(PO)in register 2 to "0" in order to set the MPU bus(D7-D0)to dither matrix memory data output mode.

② Set D7(RESET)in register 0 to "1" in order to reset the dither memory address counter.

③ Select DITH__D with register E and write DATA(0)on the MPU bus(D5-D0). Increment the address counter of the dither memory at the rising edge of WR. (during write)

④ Select DITH__D with register E and read DATA(0) in dither memory to the MPU bus(D5-D0). Increment the address counter of the dither memory at the rising edge of RD.(during read)

Dither matrix address

A0	A1	A2	A3
A4	A5	A6	A7
A8	A9	A10	A11
A12	A13	A14	A15

4X4 matrix

A0	A1	A2	A3
A4	A5	A6	A7
A8	A9	A10	A11
A12	A13	A14	A15
A16	A17	A18	A19
A20	A21	A22	A23
A24	A25	A26	A27
A28	A29	A30	A31

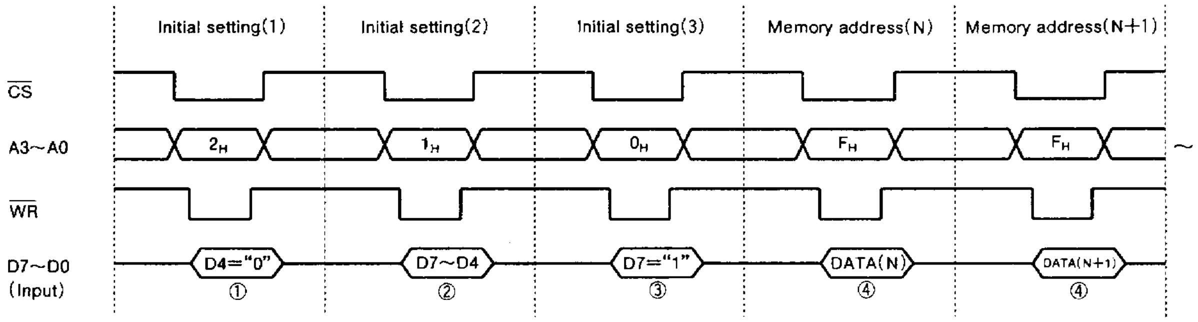
4X8 matrix

A0	A1	A2	A3	A4	A5	A6	A7
A8	A9	A10	A11	A12	A13	A14	A15
A16	A17	A18	A19	A20	A21	A22	A23
A24	A25	A26	A27	A28	A29	A30	A31
A32	A33	A34	A35	A36	A37	A38	A39
A40	A41	A42	A43	A44	A45	A46	A47
A48	A49	A50	A51	A52	A53	A54	A55
A56	A57	A58	A59	A60	A61	A62	A63

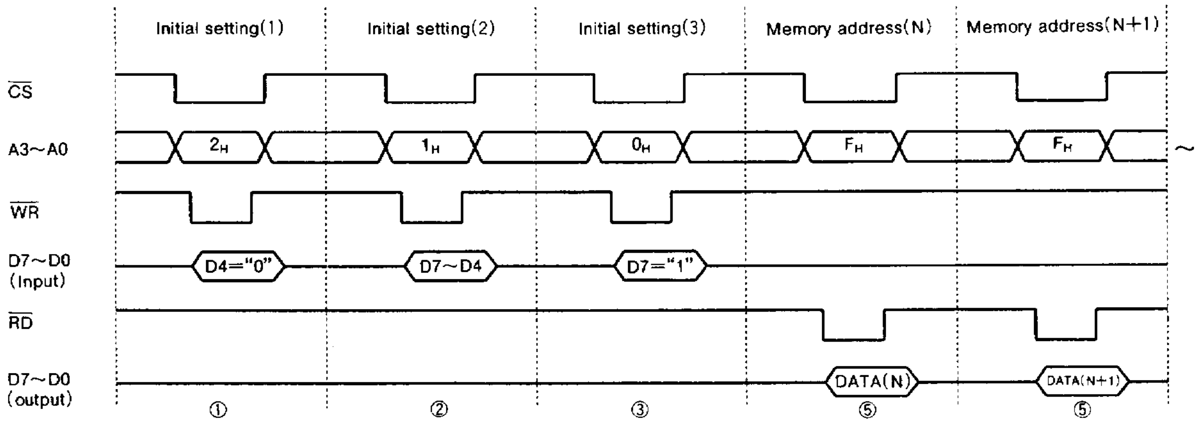
8X8 matrix

The M66333 can write/read uniformity correction data in the external correction SRAM through the MPU bus. This enables the uniformity correction data to be temporarily saved in backup memory during power off. The following figures shown the uniformity correction data write/read sequence.

Uniformity correcion memory write(MPU→M66333)



Uniformity correction memory read(M66333→MPU)



① Clear D4 (PO) in register 2 to "0" in order to set the MPU bus (D7-D0) to uniformity correction memory data output mode.

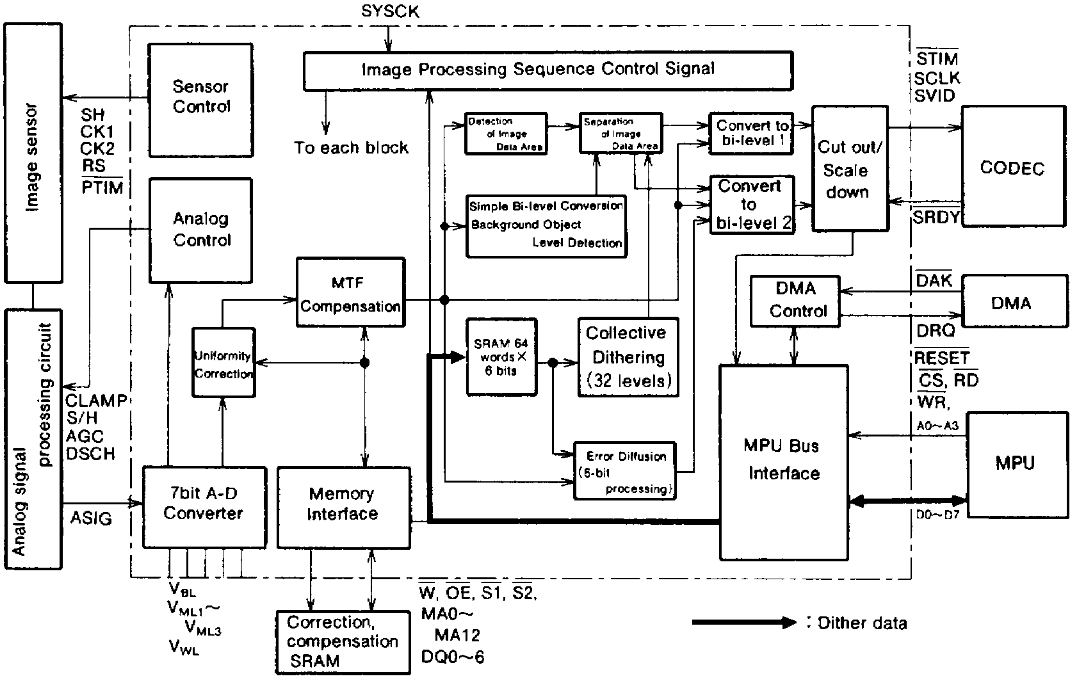
② Set D7D6 (M CLK) and D5D4 (MEMO) in register 1.

③ Set D7 (RESET) in register 0 to "1" in order to reset the uniformity correction memory address counter.

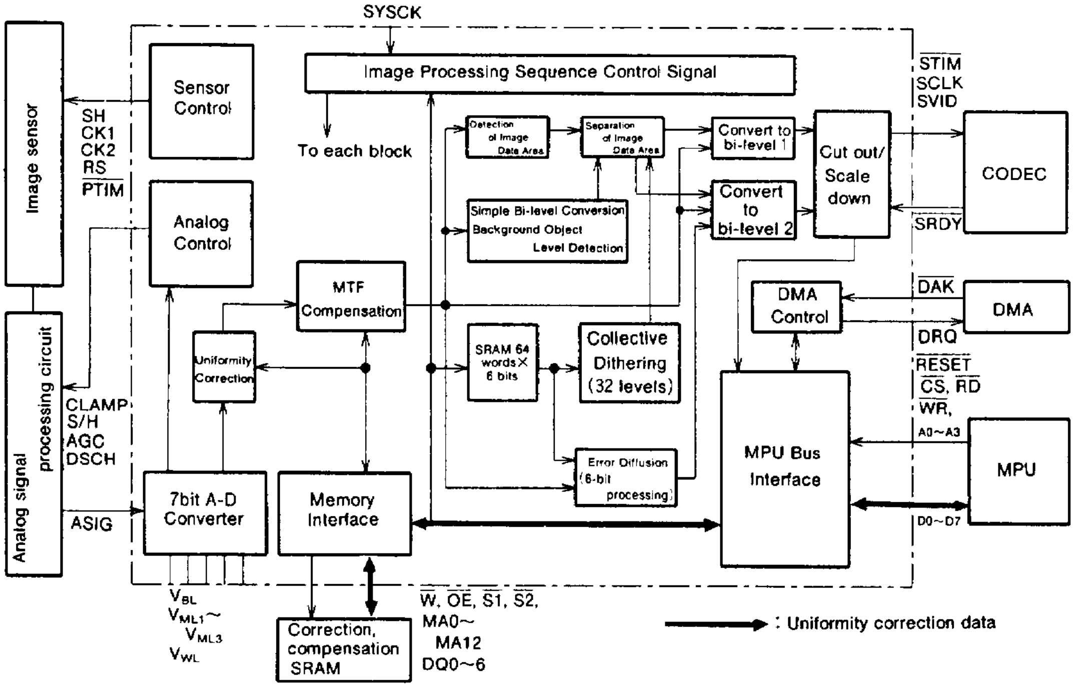
④ Select UNIF__D with register F and write DATA (N) on the MPU bus (D6-D0). Increment the address counter of the uniformity correction memory at the rising edge of WR. (during write)

⑤ Select UNIF__D with register F and read DATA (N) in uniformity correction memory to the MPU bus (D6-D0). Increment the address counter of the uniformity correction memory at the rising edge of RD. (during read)

Dither memory write/read



Uniformity correction memory write/read



(8) Image scale down and $\overline{\text{PTIM}}$ signal

Use the $\overline{\text{PTIM}}$ signal as the read roller pulse motor control signal. Figure 16 shows the sequence without scale down and Figure 17 shows the sequence with scale down (B4→A4, scaling rate : 9/11).

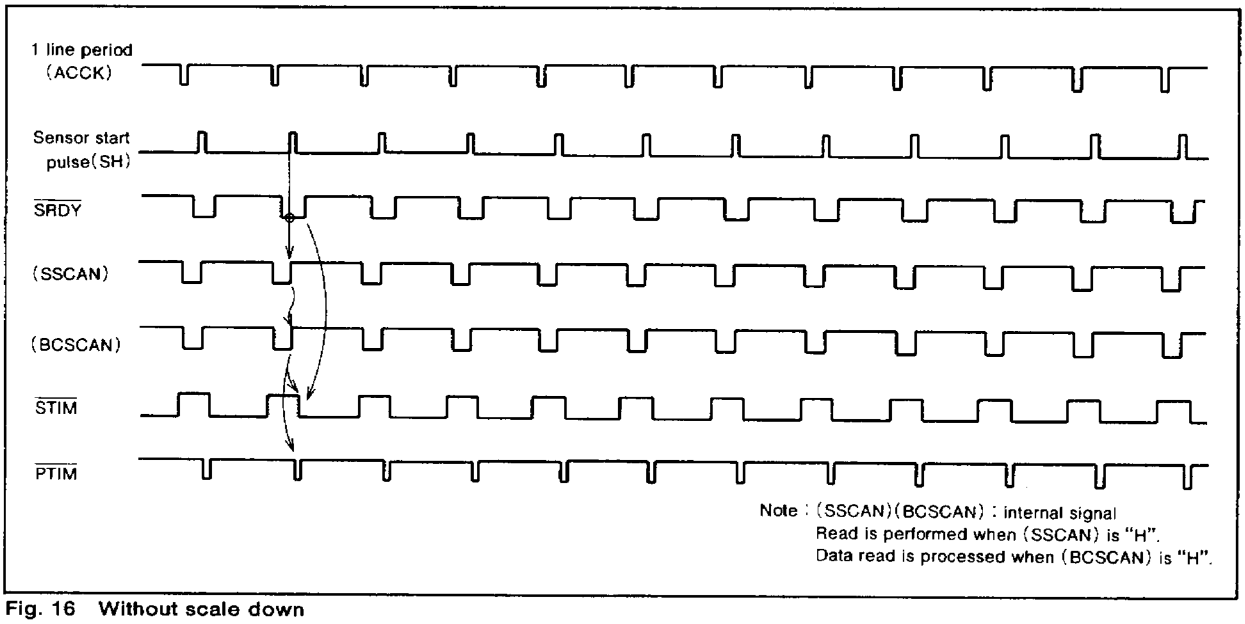


Fig. 16 Without scale down

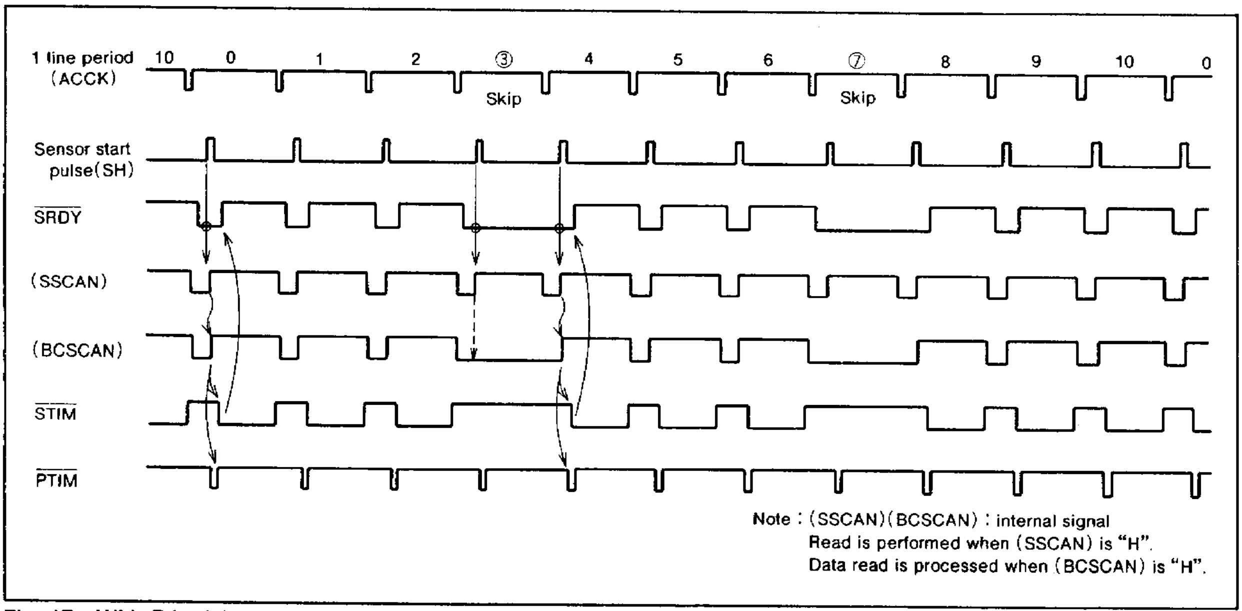


Fig. 17 With B4→A4 reduction

(9) Reset

The M66333 has three types of reset. Each reset function is described below.

Hard reset : Initializes the circuit. Hard reset also performs the following soft reset and standby reset.

Soft reset : Used when cancelling a line read operation in the middle during SCAN mode. Read operation is resumed starting from the next line. This is used during write/read of dither memory (register E) and uniformity correction memory (register F) .
Soft reset is used to reset the address counter before write/read.

Standby : Used as standby mode. The internal clock is stopped by stopping the clock generator which generates the internal clock from the system clock.
Therefore, the internal circuit is stopped and power is saved.
The period counter and register statuses are saved and the internal memory is placed in standby mode.

Table 8 Reset function

Function / Reset Types	Initialize Register	Initialize Internal F/F	Reset Period Counter	Reset Memory Interface Address Counter＊	Stop Clock Generator Operation	Stop Line Read
Hard Reset $\overline{\text{RESET}}$	○	○	○	○	○	
Soft Reset Register 0 (RESET)				○		○
Standby Register 2 (STNBY)		○		○	○	

＊ : Dither memory and uniformity correction memory address counter

(10) Image quality control using registers

- **MTF compensation**

If the sensor has high resolution, MTF compensation need not be performed for half-tone area.

MTF compensation should be performed for bi-level area regardless of the sensor resolution in order to achieve good object reproduction.

- **Simple bi-level conversion, background and object level detection**

Set the background level detection counter and object level detection counter as follows in order to obtain clear output of objects that do not have completely white background and objects that are not entirely black.

← fast
MAX_UP>MAX_DOWN>MIN_UP

The output becomes darker as bi-level conversion threshold coefficient(SLICE) is increased.

Select a large SLICE value for light source document.

- **Pseudo half-tone conversion, dither method**

Select 16 gradation using 4×4 dither matrix for fine mode and 32 gradation using 4×8 dither matrix for super fine mode. Refer to the section on image processing function for details on providing dither pattern threshold.

- **Error diffusion**

γ correction must be performed for error diffusion. This is performed by applying voltage to the middle basic supply voltage pin of the A-D converter as described in the section on image processing function.

If the printer has a thermal head, $\gamma = 0.45$ is said to be the optimum γ characteristic for the human eye.

- **Separation of image data area**

The optimum parameter is selected to perform the best bi-level conversion for each area : simple bi-level conversion for the object and pseudo half-tone conversion for half-tone.

Table 9 shows the recommended values for parameters related to picture quality.

Use these values as reference to determine the optimum parameter.

Table 9 Recommended parameter values

Image	Uniformity Correction	MTF Compensation MTF_M MTF_S	Background and Object Level						γ Correction	Dither Pattern	ERROR		Separation of Image Data Area*		
			SLICE	MAX UP	MAX DOWN	MIN UP	UL MIN	LL MAX			Error	Dither	SEP A A	SEP A B	SEP A C
Simple Bi-level Conversion	Yes	1/2	5/8	Normal	Normal	Normal	$1F_H$	20_H	No	—	—	—	—	—	—
Dithering	Yes	1/4	—	—	—	—	—	—	No	4X4 diffusion (pattern 1)	—	—	—	—	—
Error Diffusion	Yes	NON	5/8	—	—	—	—	—	$\gamma=0.45$ $V_{ML1}=0.31V$ $V_{ML2}=1.25V$ $V_{ML3}=2.50V$	4X4 diffusion (pattern 2)	7/8	1/8	$3F_H$	$3A_H$	00_H
Separation of Image Data Area	Yes	1/4	5/8	Normal	Normal	Normal	$1F_H$	20_H	No	4X4 diffusion (pattern 1)	—	—	18_H	34_H	00_H

Dither pattern 1 ($\gamma=0.6$)

0 02	8 14	2 04	10 1C
12 25	4 07	14 2F	6 0D
3 05	11 20	1 03	9 17
15 35	7 10	13 2A	5 09

Dither pattern 2

0 02	8 22	2 0A	10 2A
12 32	4 12	14 3A	6 1A
3 0E	11 2E	1 06	9 26
15 3E	7 1E	13 36	5 16

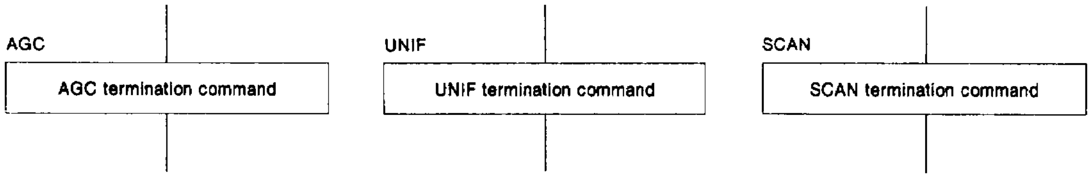
* : The value in the error diffusion column is the background processing value.

USAGE PRECAUTIONS

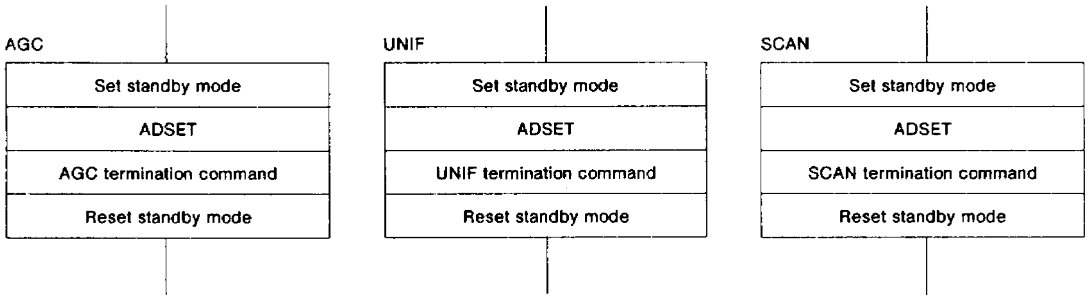
- **Operating mode termination command**

When accessing the M66333 after terminating the AGC, UNIF, or SCAN command, wait at least 1 line period after terminating the AGC, UNIF, or SCAN command. Furthermore, the ADSET processing described below is required when accessing immediately after terminating the command.

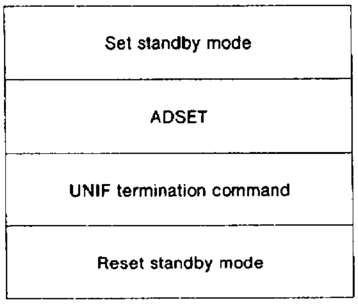
General termination commands

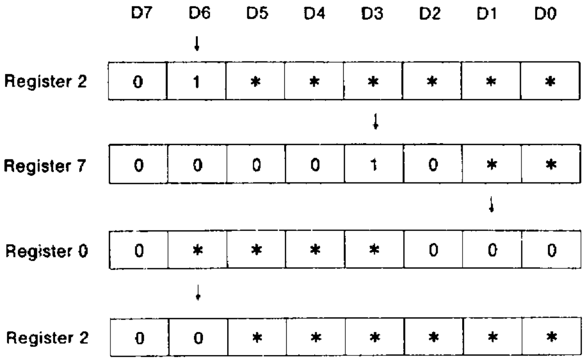


Termination command with ADSET processing



Example of UNIF termination with ADSET processing





	D7	D6	D5	D4	D3	D2	D1	D0
Register 2	0	1	*	*	*	*	*	*
Register 7	0	0	0	0	1	0	*	*
Register 0	0	*	*	*	*	0	0	0
Register 2	0	0	*	*	*	*	*	*

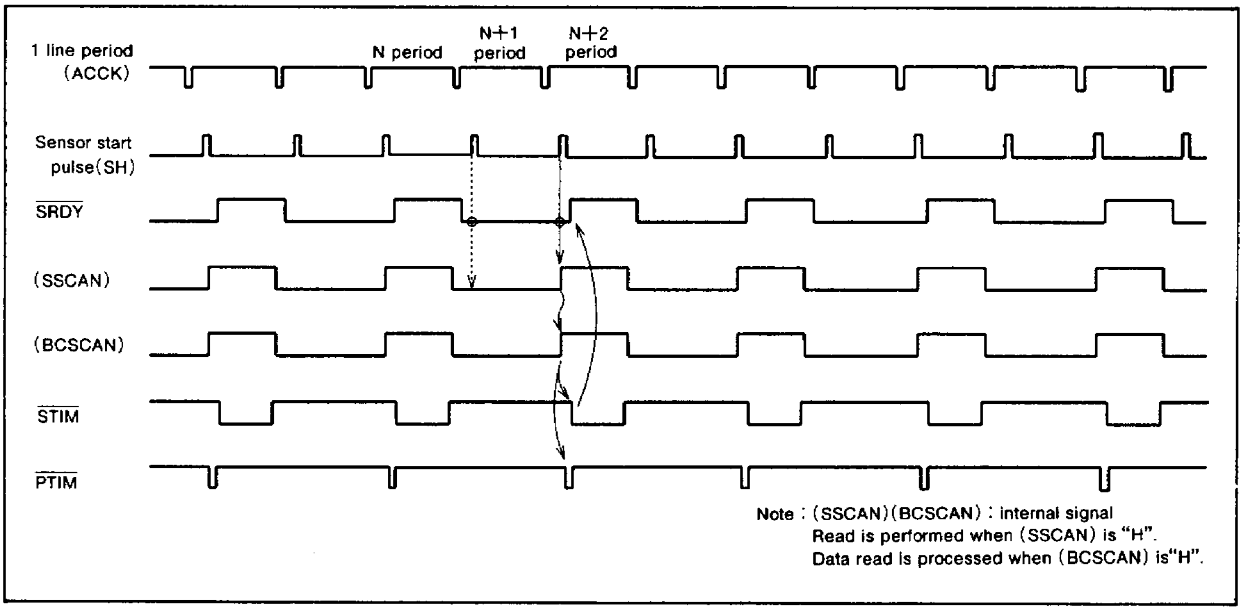
* : Set same as operating mode.

- **TIME function**

When TIME = "1" is set in register 2, the processing time per line is doubled to 2 line periods.

Data is read once every two line periods and processed.

When the read and write motors operate simultaneously during copy operation, this command can be used to reduce the processing speed to 1/2 in order to reduce the power load.



Note : (SSCAN)(BCSCAN) : internal signal
Read is performed when (SSCAN) is "H".
Data read is processed when (BCSCAN) is"H".

Fig. 18 When processing speed is 1/2

- **Peak detection in SCAN mode**

In SCAN mode, successive peak detection is performed for the image data being read as shown for the AGC range (dotted line) in Figure 1.

This enables better picture reproduction when picture data brighter than the white reference used during peak detection is input in SCAN mode.

This is especially effective for sensor units such as CIS which do not have a built-in white reference.

Register Structure

<table>
<tr><th>Address</th><th>R/W</th><th>Explanation</th></tr>
<tr><td>0_H</td><td>W</td><td>
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td>RESET</td><td>SENS</td><td colspan="2">SENS_W</td><td>UMODE</td><td>AGC</td><td>UNIF</td><td>SCAN</td><td>(Default is 00_H)</td></tr>
</table>
<table>
<tr><th>D7</th><th>RESET System Reset</th></tr>
<tr><td>0</td><td>Normal Mode</td></tr>
<tr><td>1</td><td>Reset Mode</td></tr>
</table>
• Reset while write pulse is "L" when D7="1".
<table>
<tr><th>D6</th><th>SENS Sensor Type</th></tr>
<tr><td>0</td><td>CCD</td></tr>
<tr><td>1</td><td>CIS</td></tr>
</table>
<table>
<tr><th>D5</th><th>D4</th><th>SENS_W Sensor Width</th></tr>
<tr><td>0</td><td>0</td><td>A4</td></tr>
<tr><td>0</td><td>1</td><td>B4</td></tr>
<tr><td>1</td><td>0</td><td>A3</td></tr>
<tr><td>1</td><td>1</td><td>—</td></tr>
</table>
<table>
<tr><th rowspan="2">D3</th><th colspan="2">UMODE Uniformity Correction Mode</th></tr>
<tr><th>White & Black Correction</th><th>White Correction only</th></tr>
<tr><td>0</td><td>White Correction</td><td>—</td></tr>
<tr><td>1</td><td>Black Correction</td><td>White Correction</td></tr>
</table>
• For selecting correction mode in UNIF mode. Refer to Table 4.
<table>
<tr><th>D2</th><th>AGC Auto Gain Control</th></tr>
<tr><td>0</td><td>Stop</td></tr>
<tr><td>1</td><td>Start</td></tr>
</table>
• Controls AGC mode start/stop.
<table>
<tr><th>D1</th><th>UNIF Uniformity Correction</th></tr>
<tr><td>0</td><td>Stop</td></tr>
<tr><td>1</td><td>Start</td></tr>
</table>
• Controls UNIF mode start/stop.
<table>
<tr><th>D0</th><th>SCAN Source Scanning</th></tr>
<tr><td>0</td><td>Stop</td></tr>
<tr><td>1</td><td>Start</td></tr>
</table>
• Controls SCAN mode start/stop.
</td></tr>
<tr><td>1_H</td><td>W</td><td>
<table>
<tr><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td colspan="2">M_CLK</td><td colspan="2">MEMO</td><td>UNIFM</td><td>S/H_W</td><td>SH_W</td><td>CLAMP</td><td>(Default is 00_H)</td></tr>
</table>
<table>
<tr><th>D7</th><th>D6</th><th>M_CLK Memory Read/Write Cycle</th><th>Correction</th><th>Compensation</th><th>Error</th></tr>
<tr><td>0</td><td>0</td><td>7 Cycle</td><td>Black, White</td><td>Now, Pre, Next</td><td>R, W</td></tr>
<tr><td>0</td><td>1</td><td>4 Cycle</td><td>White</td><td>Now, Pre, Next</td><td>—</td></tr>
<tr><td>1</td><td>0</td><td>5 Cycle</td><td>Black, White</td><td>Now, Pre, Next</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>6 Cycle</td><td>White</td><td>Now, Pre, Next</td><td>R, W</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Explanation</th></tr>
<tr><td>1_H</td><td>W</td><td>
<table>
<tr><th>D5</th><th>D4</th><th>MEMO Memory Map</th></tr>
<tr><td>0</td><td>0</td><td>SRAM (64K)</td></tr>
<tr><td>0</td><td>1</td><td>SRAM (64K)+EPROM (32K)</td></tr>
<tr><td>1</td><td>0</td><td>SRAM (64K)×2 or SRAM (64K)+EPROM (64K)</td></tr>
<tr><td>1</td><td>1</td><td>SRAM (256K)</td></tr>
</table>
• Refer to Table 7 for the relationship between the external memory types and MCLK.
<table>
<tr><th>D3</th><th>UNIFM Uniformity Correction of CIS</th></tr>
<tr><td>0</td><td>White Correction only</td></tr>
<tr><td>1</td><td>White and black Correction</td></tr>
</table>
• For selecting correction mode in SCAN mode. Also use the same settings in UNIF mode. See Table 4.
<table>
<tr><th>D2</th><th>S/H_W Pulse Width of S/H</th></tr>
<tr><td>0</td><td>Normal (Sysclk period×4)</td></tr>
<tr><td>1</td><td>Normol×0. 5</td></tr>
</table>
<table>
<tr><th>D1</th><th>SH_W Pulse Width of SH</th></tr>
<tr><td>0</td><td>Normal (Sysclk period×16)</td></tr>
<tr><td>1</td><td>Reverse of (Normal×2)</td></tr>
</table>
• In case of CCD, there is only one SH pulse width and this register is ignored.
<table>
<tr><th>D0</th><th>CLAMP Clamp Method of Analog Circuit</th></tr>
<tr><td>0</td><td>Bit Clamp</td></tr>
<tr><td>1</td><td>Line Clamp</td></tr>
</table>
• Line clamp dose not apply to CIS.
</td></tr>
<tr><td>2_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>ER_S</td><td>STNBY</td><td>TIME</td><td>P_O</td><td colspan="2">SOURCE</td><td>DEST</td><td>REDU</td></tr>
</table>
(Default is 00_H)
<table>
<tr><th>D7</th><th>ER_S Error Diffusion Background Processing</th></tr>
<tr><td>0</td><td>Yes</td></tr>
<tr><td>1</td><td>No</td></tr>
</table>
<table>
<tr><th>D6</th><th>STNBY Standby Mode</th></tr>
<tr><td>0</td><td>Normal</td></tr>
<tr><td>1</td><td>Standby Mode</td></tr>
</table>
• Standby mode stops the clock generation circuit. The period counter and register status are saved and the internal memory is placed in standby mode.
<table>
<tr><th>D5</th><th>TIME Line Time</th></tr>
<tr><td>0</td><td>1 Line Period</td></tr>
<tr><td>1</td><td>2 Line Period</td></tr>
</table>
• When read and write operations are performed together as in copy operation, the power load can be reduced by selecting 2 line period. The processing speed drops to 1/2 when 2 line period is selected.
<table>
<tr><th>D4</th><th>P_O Parallel Output</th></tr>
<tr><td>0</td><td>Without Parallel Output</td></tr>
<tr><td>1</td><td>Parallel Output</td></tr>
</table>
• D0 is output in LSB format and D7 is output in MSB format. When SCAN data is output in SCAN mode, D7 is output in LSB format and Dφ is output in MSB format
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Explanation</th></tr>
<tr><td>2_H</td><td>W</td><td>
<table>
<tr><th>D3</th><th>D2</th><th>SOURCE Source Width</th></tr>
<tr><td>0</td><td>0</td><td>A4</td></tr>
<tr><td>0</td><td>1</td><td>B4</td></tr>
<tr><td>1</td><td>0</td><td>A3</td></tr>
<tr><td>1</td><td>1</td><td>—</td></tr>
</table>
<table>
<tr><th>D1</th><th>DEST Destination Width</th></tr>
<tr><td>0</td><td>A4</td></tr>
<tr><td>1</td><td>B4</td></tr>
</table>
<table>
<tr><th>D0</th><th>REDU Scale down/Cut out</th></tr>
<tr><td>0</td><td>Cut out</td></tr>
<tr><td>1</td><td>Scale down</td></tr>
</table>
<table>
<tr><th colspan="2">Scaling Rate</th></tr>
<tr><td>A3→B4</td><td>13/15</td></tr>
<tr><td>B4→A4</td><td>9/11</td></tr>
<tr><td>A3→A4</td><td>12/17</td></tr>
</table>
• Refer to image scale down/area specification for scale down/ cut out.
</td></tr>
<tr><td>3_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">PRE_DATA 〈7 : 0〉</td></tr>
</table>
(Default is 00_H)
D7～D0 : PRE_DATA 〈7 : 0〉 Pre Data of Line period Counter (Lower part)
</td></tr>
<tr><td>4_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="3"></td><td colspan="5">PRE_DATA 〈12 : 8〉</td></tr>
</table>
(Default is 00_H)
D4～D0 : PRE_DATA 〈12 : 8〉 Pre Data of Line period Counter (Upper part)
• 1 line period is determined from PRE_DATA and pixel transmission clock frequency (ADCK).
ADCK is 1/16 of system clock.
Refer to line period and read sequence section.
</td></tr>
<tr><td>5_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td></td><td colspan="7">ST_PL 〈6 : 0〉</td></tr>
</table>
(Default is 00_H)
D6～D0 : ST_PL 〈6 : 0〉 Start Pulse of Line Sensor
• Set ST_PL=(sensor dummy pixel+2)
Refer to line period and read sequence section.
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Explanation</th></tr>
<tr><td>6_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td colspan="2">DITH</td><td colspan="2">MODE</td><td colspan="2">MTF_M</td><td colspan="2">MTF_S</td><td>(Default is 00_H)</td></tr>
</table>
<table>
<tr><th>D7</th><th>D6</th><th>DITH Dither Matrix Size</th></tr>
<tr><td>0</td><td>0</td><td>4×4</td></tr>
<tr><td>0</td><td>1</td><td>4×8</td></tr>
<tr><td>1</td><td>0</td><td>8×8</td></tr>
<tr><td>1</td><td>1</td><td>—</td></tr>
</table>
<table>
<tr><th>D5</th><th>D4</th><th>MODE Bi-level Mode</th></tr>
<tr><td>0</td><td>0</td><td>Simple Bi-level</td></tr>
<tr><td>0</td><td>1</td><td>Dither</td></tr>
<tr><td>1</td><td>0</td><td>Separation (Simple Bi-level+Dither)</td></tr>
<tr><td>1</td><td>1</td><td>Error Diffusion</td></tr>
</table>
<table>
<tr><th>D3</th><th>D2</th><th>MTF_M Main Coefficient of MTF Compensation</th></tr>
<tr><td>0</td><td>0</td><td>NON (0)</td></tr>
<tr><td>0</td><td>1</td><td>A little less (1/4)</td></tr>
<tr><td>1</td><td>0</td><td>Middle (1/2)</td></tr>
<tr><td>1</td><td>1</td><td>A little over (1)</td></tr>
</table>
<table>
<tr><th>D1</th><th>D0</th><th>MTF_S Sub Coefficient of MTF Compensation</th></tr>
<tr><td>0</td><td>0</td><td>NON (0)</td></tr>
<tr><td>0</td><td>1</td><td>A little less (1/4)</td></tr>
<tr><td>1</td><td>0</td><td>Middle (1/2)</td></tr>
<tr><td>1</td><td>1</td><td>A little over (1)</td></tr>
</table>
</td></tr>
<tr><td>7_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td>0</td><td colspan="3"></td><td>ADSET</td><td>0</td><td colspan="2">ERROR</td><td>(Default is 00_H)</td></tr>
</table>
<table>
<tr><th>D3</th><th>ADSET ADSET processing</th></tr>
<tr><td>0</td><td>No</td></tr>
<tr><td>1</td><td>Yes</td></tr>
</table>
• Refer to usage precautions.
<table>
<tr><th rowspan="2">D1</th><th rowspan="2">D0</th><th colspan="2">ERROR</th></tr>
<tr><th>Error (basic)</th><th>Dither addition rate for error</th></tr>
<tr><td>0</td><td>0</td><td>Strong(7/8)</td><td>Weak(1/8)</td></tr>
<tr><td>0</td><td>1</td><td>Strong(7/8)</td><td>Strong(1/4)</td></tr>
<tr><td>1</td><td>0</td><td>Weak(3/4)</td><td>Weak(1/8)</td></tr>
<tr><td>1</td><td>1</td><td>Weak(3/4)</td><td>Strong(1/4)</td></tr>
</table>
• Fix at D7=D2=0.
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Explanation</th></tr>
<tr><td>8_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td colspan="2"></td><td colspan="6">SEPA_A</td><td>(Default is 00_H)</td></tr>
</table>
D5~D0 : SEPA_A Separation of Image Data Area (Difference)
</td></tr>
<tr><td>9_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td colspan="2"></td><td colspan="6">SEPA_B</td><td>(Default is 00_H)</td></tr>
</table>
D5~D0 : SEPA_B Separation of Image Data Area (MIN)
</td></tr>
<tr><td>A_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td colspan="2"></td><td colspan="6">SEPA_C</td><td>(Default is 00_H)</td></tr>
</table>
D5~D0 : SEPA_C Separation of Image Data Area (MAX)
</td></tr>
<tr><td>B_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td colspan="2">SLICE</td><td colspan="2">MAX_UP</td><td colspan="2">MAX_DOWN</td><td colspan="2">0_0</td><td>(Default is 00_H)</td></tr>
</table>
<table>
<tr><th>D7</th><th>D6</th><th>SLICE Detector of Background and Object level (SLICE)</th></tr>
<tr><td>0</td><td>0</td><td>Normal (4/8)</td></tr>
<tr><td>0</td><td>1</td><td>light (3/8)</td></tr>
<tr><td>1</td><td>0</td><td>Dark (5/8)</td></tr>
<tr><td>1</td><td>1</td><td>More Dark (6/8)</td></tr>
</table>
<table>
<tr><th>D5</th><th>D4</th><th>MAX_UP Detector of Background level (Up Counter CLK)</th></tr>
<tr><td>0</td><td>0</td><td>Normal (T=(1 pixel period)×32)</td></tr>
<tr><td>0</td><td>1</td><td>Slow (T=(1 pixel period)×64)</td></tr>
<tr><td>1</td><td>0</td><td>Fast (T=(1 pixel period)×16)</td></tr>
<tr><td>1</td><td>1</td><td>More fast (T=(1 pixel period)×8)</td></tr>
</table>
<table>
<tr><th>D3</th><th>D2</th><th>MAX_DOWN Detector of Background level (Down Counter CLK)</th></tr>
<tr><td>0</td><td>0</td><td>Normal (T=(1 pixel period)×128)</td></tr>
<tr><td>0</td><td>1</td><td>Slow (T=(1 pixel period)×256)</td></tr>
<tr><td>1</td><td>0</td><td>Fast (T=(1 pixel period)×64)</td></tr>
<tr><td>1</td><td>1</td><td>More fast (T=(1 pixel period)×32)</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Address</th><th>R/W</th><th>Explanation</th></tr>
<tr><td>C_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td>REDM</td><td></td><td colspan="6">UL__MIN</td><td>(Default is 31_H)</td></tr>
</table>
<table>
<tr><th>D7</th><th>REDM Scaling Factor in Secondary Scanning Direction</th><th>Remarks</th></tr>
<tr><td>0</td><td>No</td><td>Scaling factor in secondary scanning direction is not supported. It must be supported by the system.</td></tr>
<tr><td>1</td><td>Yes</td><td>Control the read roller pulse motor according to $\overline{\text{PTIM}}$.</td></tr>
</table>
D5~D0 : UL__MIN Detector of Object level (Upper Limit)
</td></tr>
<tr><td>D_H</td><td>W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td colspan="2"></td><td colspan="6">LL__MAX</td><td>(Default is 32_H)</td></tr>
</table>
D5~D0 : LL__MAX Detector of Background level (Lower Limit)
</td></tr>
<tr><td>E_H</td><td>R/W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="2"></td><td colspan="6">DITH__D</td></tr>
</table>
D5~D0 : DITH__D Internal dither memory data
• Refer to the section on dither memory, uniformity correction memory read/write for information concerning write/read method.
</td></tr>
<tr><td>F_H</td><td>R/W</td><td>
<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td colspan="8">UNIF__D</td></tr>
</table>
D7~D0 : UNIF__D External memory uniformity correction data
• Refer to the section on dither memory, uniformity correction memory read/write for information concerning write/read method.
</td></tr>
</table>

ABSOLUTE MAXIMUM RATING (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3~+7.0	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
AV_{CC}	Analog supply voltage		V_{CC}−0.3~V_{CC}+0.3	V
V_{WL}	Reference voltage (White)		−0.3~AV_{CC}+0.3	V
V_{BL}	Reference voltage (Black)		−0.3~AV_{CC}+0.3	V
V_{ML}	Reference voltage (Middle)		−0.3~AV_{CC}+0.3	V
V_{AIN}	Analog input voltage		−0.3~AV_{CC}+0.3	V
Tstg	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
GND	Ground			0		V
V_I	Input voltage		0		V_{CC}	V
AV_{CC}	Analog supply voltage		4.5	5.0	5.5	V
A_{GND}	Analog ground (Note)			0		V
V_{WL}	Reference voltage (White)		3		AV_{CC}	V
V_{BL}	Reference voltage (Black)		0.0	0.0	1.0	V
V_{AIN}	Analog input voltage	ASIG	V_{BL}		V_{WL}	V
Topr	Operating temperature range		−20		75	℃

Note : Please connect AGND with GND.

ELECTRICAL CHARACTERISTICS ($T_a=-20\sim75$℃, $V_{CC}=5V\pm10\%$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	"H" Input voltage	SYSCK, DQ0~DQ6, $\overline{SRDY}$, $\overline{DAK}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0~A3, D0~D7		2.0			V
V_{IL}	"L" Input voltage					0.8	V
V_{T+}	Positive-going threshold voltage	$\overline{RESET}$				2.4	V
V_{T-}	Negative-going threshold voltage			0.6			V
V_H	Hysteresis voltage				0.2		V
V_{OH}	High-level output voltage	D0~D7	$I_{OH}=-12mA$	$V_{CC}-0.8$			V
V_{OL}	Low-level output voltage		$I_{OL}=12mA$			0.55	V
V_{OH}	High-level output voltage	SH, CK1, CK2, RS $\overline{PTIM}$, CLAMP, S/H, AGC, DSCH $\overline{STIM}$, SCLK, SVID $\overline{W}$, $\overline{OE}$, $\overline{S1}$, $\overline{S2}$, DQ0~DQ6 MA0~MA12, DRQ	$I_{OH}=-4mA$	$V_{CC}-0.8$			V
V_{OL}	Low-level output voltage		$I_{OL}=4mA$			0.55	V
I_{IH}	High-level input current	$\overline{SRDY}$, $\overline{DAK}$ $\overline{RESET}$, $\overline{CS}$ $\overline{RD}$, $\overline{WR}$, A0~A3	$V_{CC}=5.5V$ $V_I=5.5V$			1.0	μA
I_{IL}	Low-level input current		$V_{CC}=5.5V$ $V_I=0V$			−1.0	μA
I_{OZH}	Off-state high-level output current	D0~D7 DQ0~DQ6	$V_{CC}=5.5V$ $V_O=5.5V$			5.0	μA
I_{OZL}	Off-state low-level output current		$V_{CC}=5.5V$ $V_O=0V$			−5.0	μA
I_{AIN}	Analog input current	ASIG				±10	μA
R_L	Reference resistance				1.3		KΩ
S_{INL}	A-D converter Non-linear error (Note 1)		$V_{CC}=5.0V$		±0.5	±1.5	LSB
I_{CCS}	Quiescent supply current (Standby) (Note 2)		$V_{CC}=5.5V$ $V_I=V_{CC}$, GND		20	40	mA
I_{CCA}	Quiescent supply current (Active state) (Note 2)		$V_{CC}=5.5V$ $V_I=V_{CC}$, GND		30	60	mA
I_{CC}	Dynamic supply current	SYSCK=8MHz	$V_{CC}=5.5V$ $V_I=V_{CC}$, GND		45		mA

Note 1 : The A-D converter has a 7-bit resolution.
2 : Current flowing in the reference resistor in the A-D converter is not included.

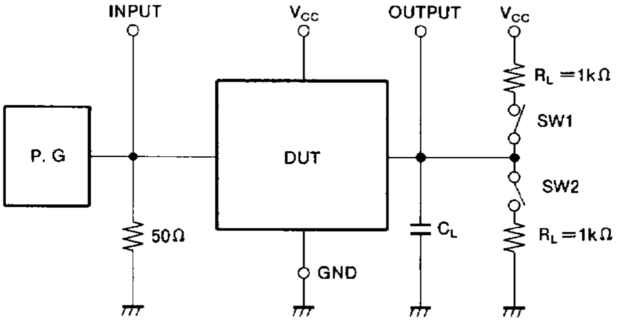
TIMING REQUIREMENT (T$_a$=−20~75℃, V$_{CC}$=5V±10%, unless otherwise noted)

Symbol	Parameter			Test conditions	Limits			Unit
					Min.	Typ.	Max.	
$t_{c(SYS)}$	System clock	Period				125		ns
$t_{w+(SYS)}$		High-level pulse width				62.5		ns
$t_{w-(SYS)}$		Low-level pulse width				62.5		ns
$t_{r(SYS)}$		Rise time					20	ns
$t_{f(SYS)}$		Fall time					20	ns
$t_{w(\overline{RD})}$	Read pulse	Pulse width			100			ns
$t_{su(\overline{CS}-\overline{RD})}$		Setup time	$\overline{CS}$		20			ns
$t_{su(A-\overline{RD})}$		Setup time	A0~A3		20			ns
$t_{su(\overline{DAK}-\overline{RD})}$		Setup time	$\overline{DAK}$		20			ns
$t_{h(\overline{RD}-\overline{CS})}$		Hold time	$\overline{CS}$		10			ns
$t_{h(\overline{RD}-A)}$		Hold time	A0~A3		10			ns
$t_{h(\overline{RD}-\overline{DAK})}$		Hold time	$\overline{DAK}$		10			ns
$t_{w(\overline{WR})}$	Write pulse	Pulse width			100			ns
$t_{su(\overline{CS}-\overline{WR})}$		Setup time	$\overline{CS}$		20			ns
$t_{su(A-\overline{WR})}$		Setup time	A0~A3		20			ns
$t_{su(D-\overline{WR})}$		Setup time	D0~D7		50			ns
$t_{h(\overline{WR}-\overline{CS})}$		Hold time	$\overline{CS}$		20			ns
$t_{h(\overline{WR}-A)}$		Hold time	A0~A3		10			ns
$t_{h(\overline{WR}-D)}$		Hold time	D0~D7		0			ns
$t_{h(\overline{STIM}-\overline{SRDY})}$	$\overline{STIM}$	Hold time	$\overline{SRDY}$		0			ns

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{PZL}($\overline{RD}$−D) t_{PZH}($\overline{RD}$−D)	Output enable time to low-level and high-level (RD-D)	C_L=150pF			75	ns
t_{PLZ}($\overline{RD}$−D) t_{PHZ}($\overline{RD}$−D)	Output disable time from low-level and high-level (RD-D)		10		50	ns
t_{PHL}($\overline{RD}$−DRQ)	High-level to low-level output propagation time (RD-DRQ)	C_L=50pF			50	ns

Test Circuit

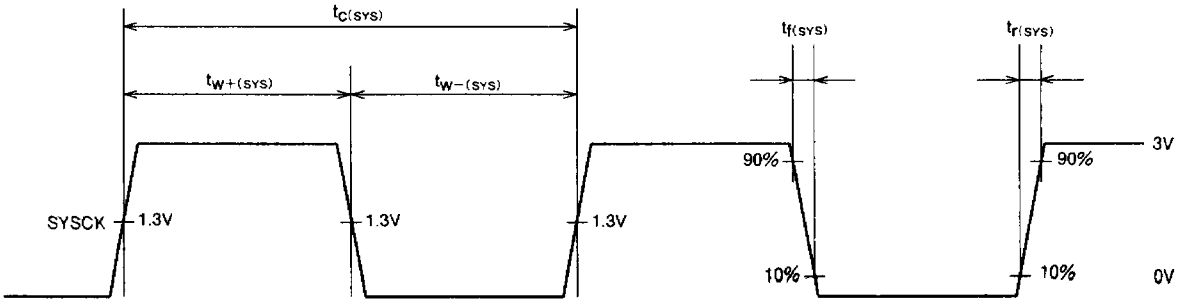


Parameter	SW1	SW2
t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%) : tr = 3ns, tf = 3ns

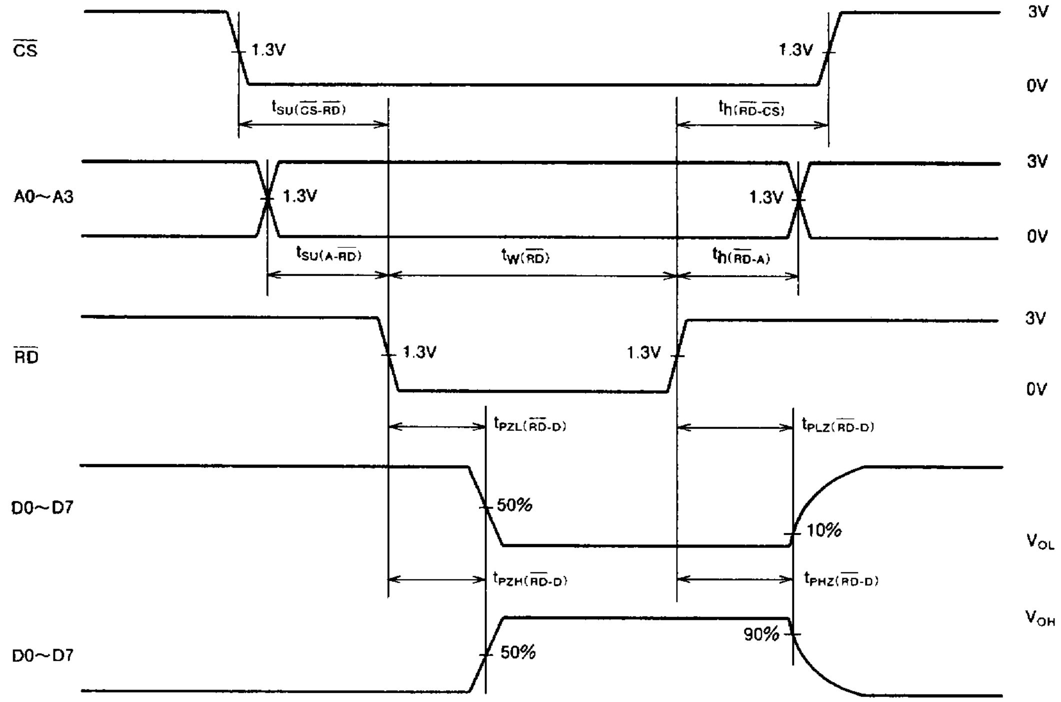
(2) The capacitance C_L = 150pF includes stray wiring capacitance and the probe input capacitance.

System clock

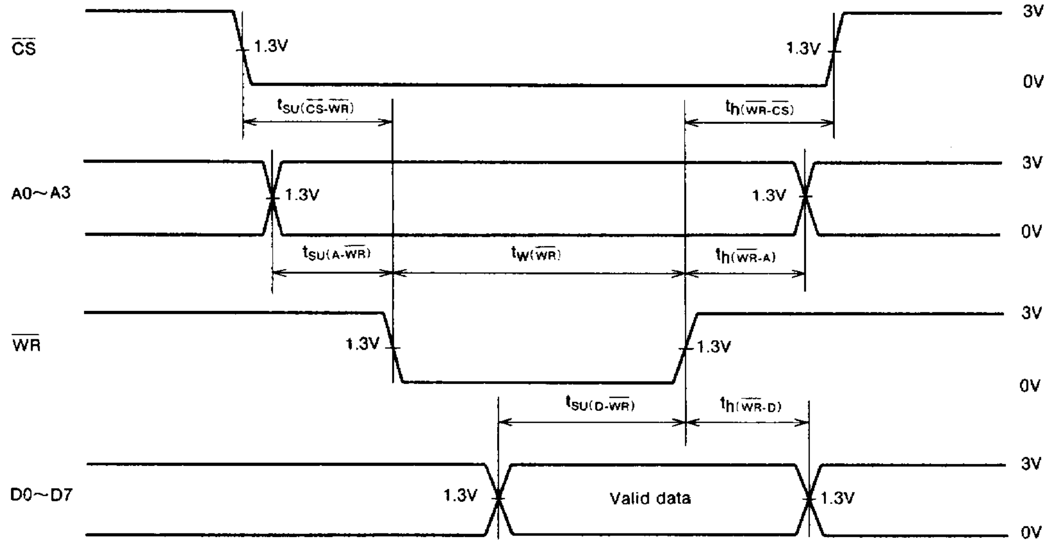


MPU Interface

1)Read timing (M66333→MPU)

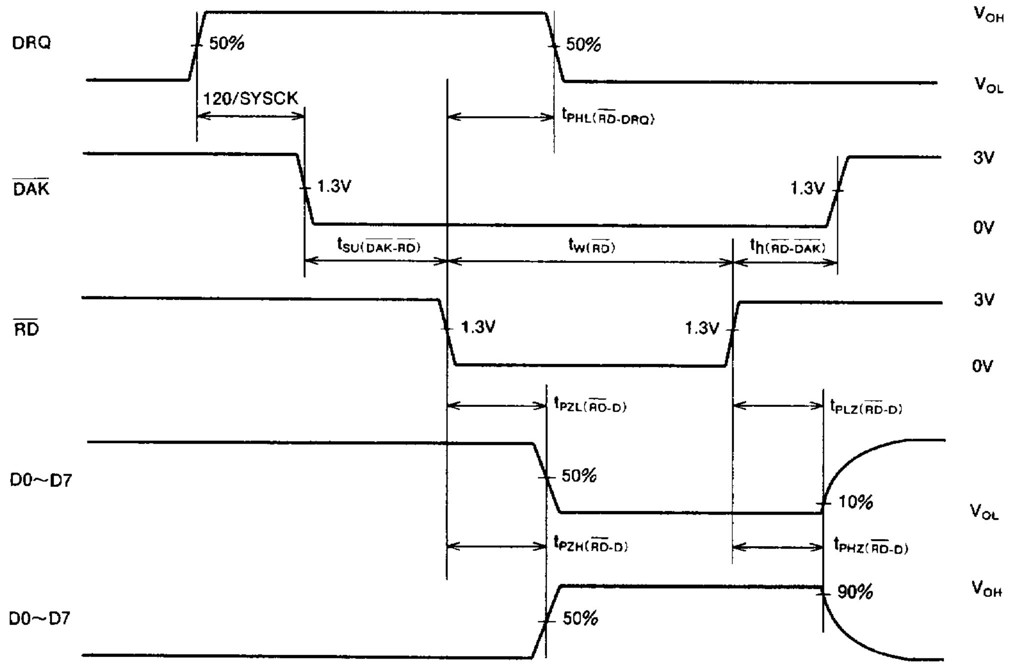


2)Write timing (MPU→M66333)

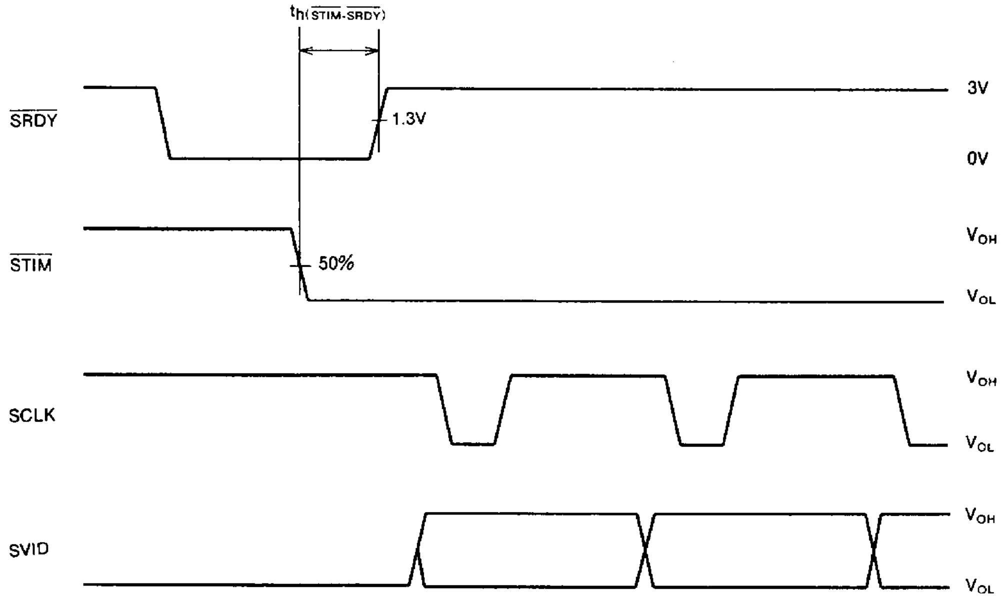


DMA timing

Read timing (M66333→System bus)



CODEC interface

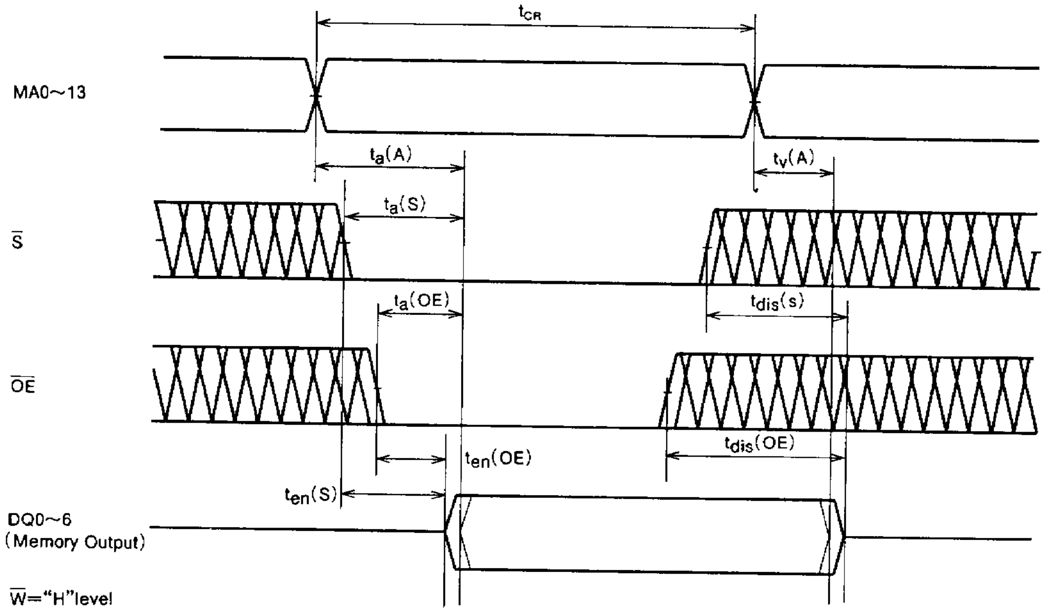


TIMING REQUIREMENT OF EXTERNAL MEMORY

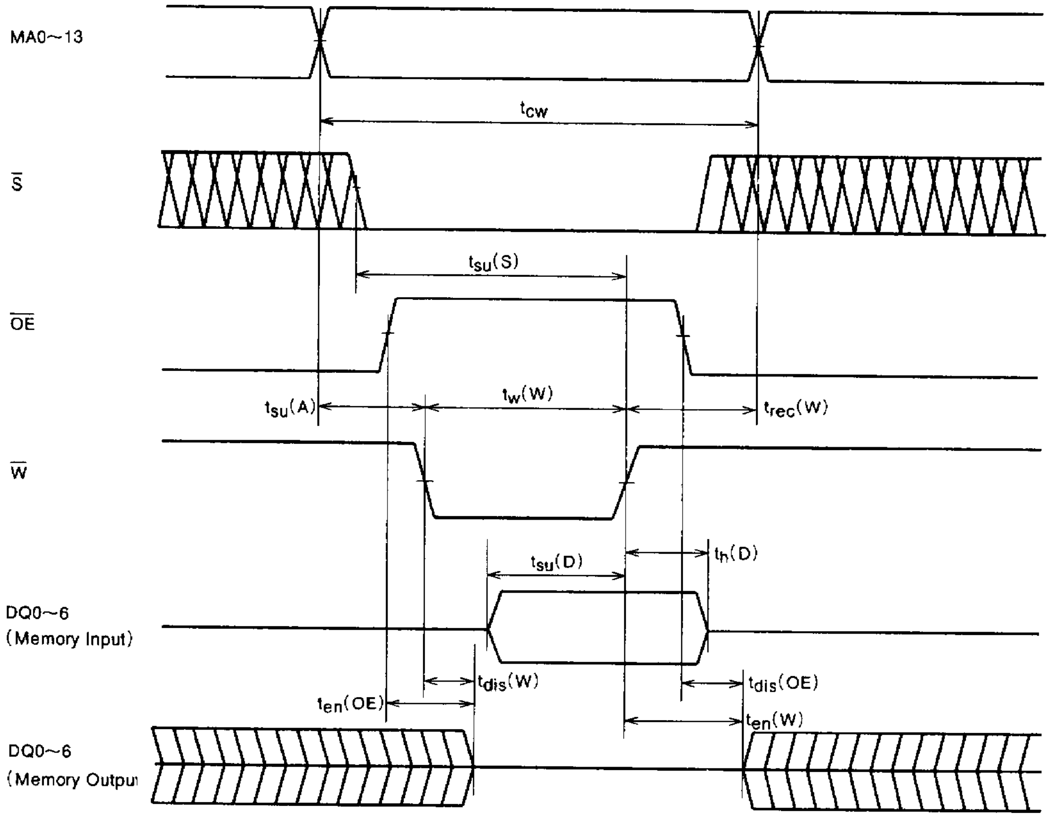
Symbol	Parameter			Test Condition	Limits			Unit
					Min.	Typ.	Max.	
t_{CR}	Read cycle time				100			ns
$t_{a(A)}$	Access time	Address	MA0～13				100	ns
$t_{a(S)}$		Chip select	$\overline{S}$				100	ns
$t_{a(OE)}$		Output enable	$\overline{OE}$				50	ns
$t_{dis(S)}$	Disable time	Chip select	S				35	ns
$t_{dis(OE)}$		Output enable	$\overline{OE}$				35	ns
$t_{en(S)}$	Enable time	Chip select	$\overline{S}$		10			ns
$t_{en(OE)}$		Output enable	$\overline{OE}$		10			ns
$t_{V(A)}$	Data effective time after Address				10			ns
t_{CW}	Write cycle				100			ns
$t_{W(W)}$	Write pulse				60			ns
$t_{SU(A)}$	Setup time	Address	MA0～13		0			ns
$t_{SU(S)}$		Chip select	$\overline{S}$		80			ns
$t_{SU(D)}$		Data	DQ0～6		35			ns
$t_{h(D)}$	Data hold time				0			ns
$t_{rec(W)}$	Write recovery time				0			ns
$t_{dis(W)}$	Output disable time after write enable						35	ns
$t_{en(W)}$	Output enable time after write enable				10			ns

Memory Interface

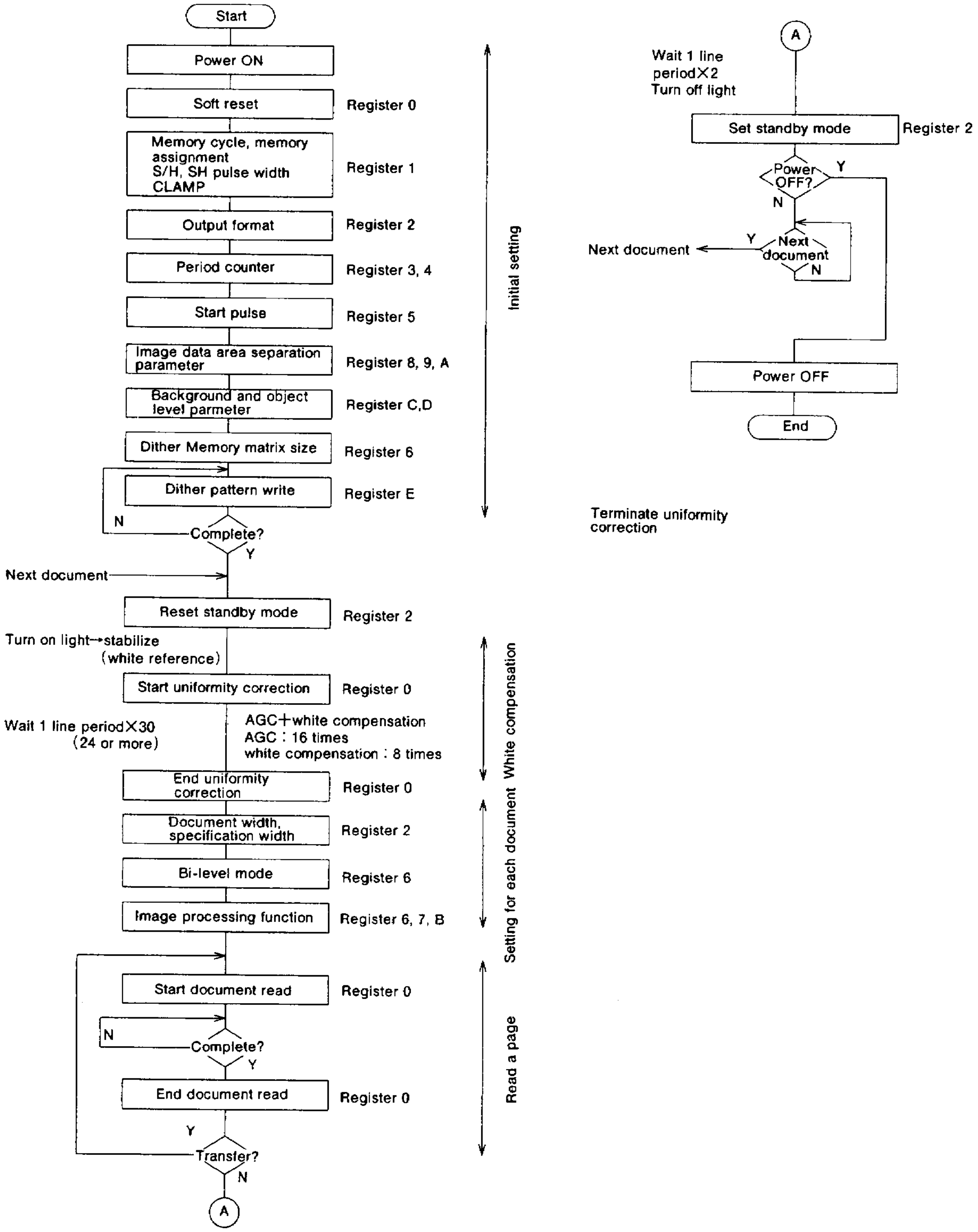
a)Read cycle



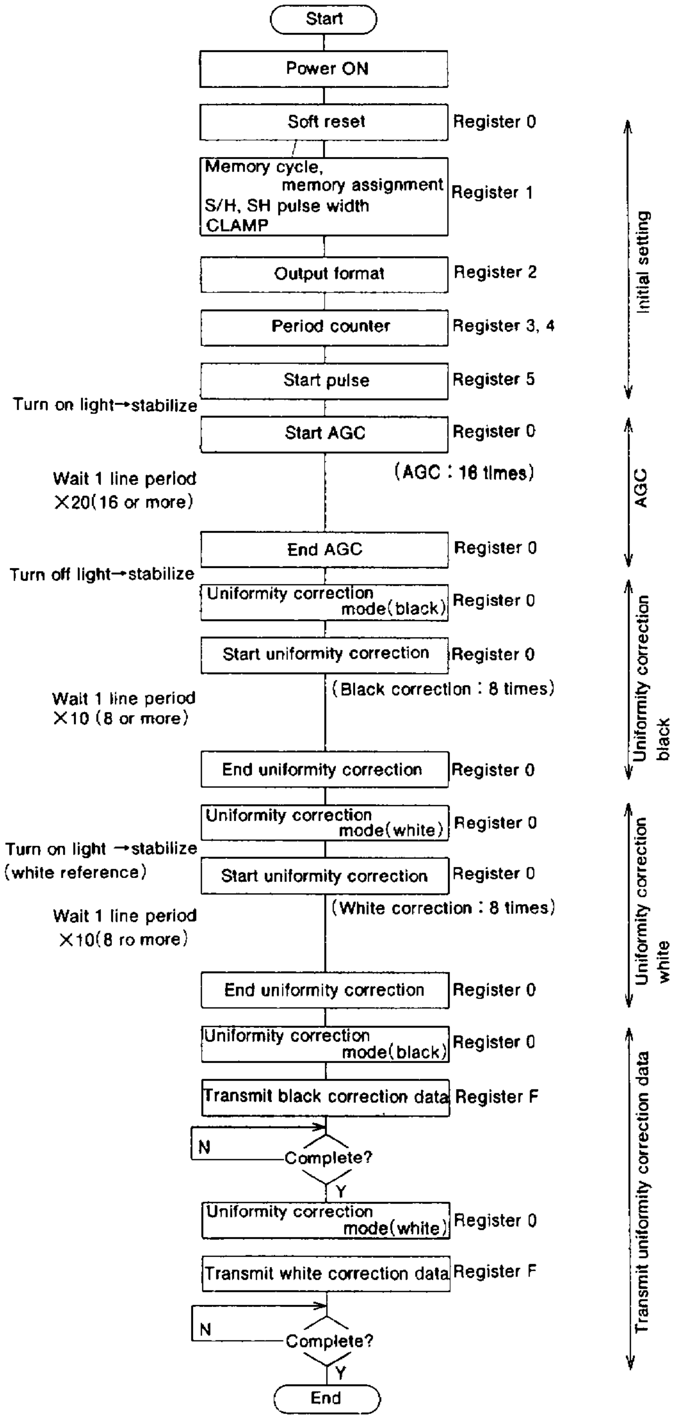
b)Write cycle(Write control Mode)



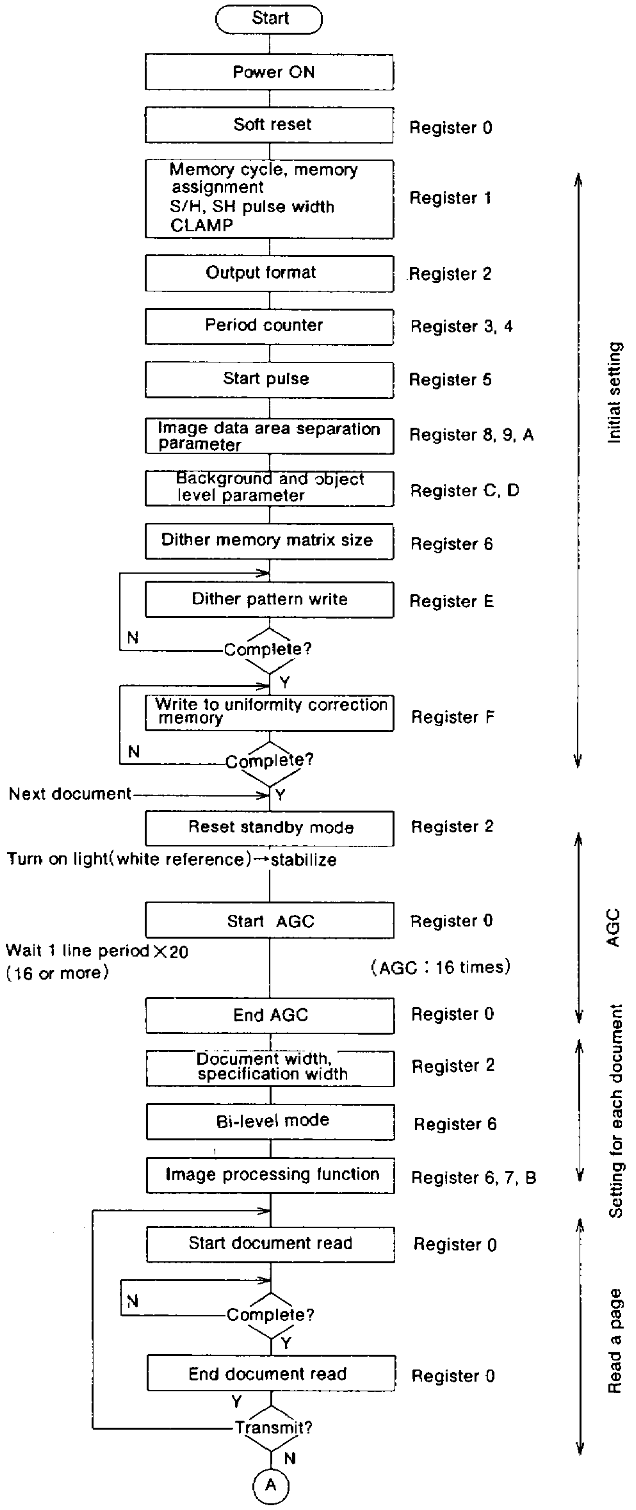
Flowchart
Read Operation(Sensor : CCD)

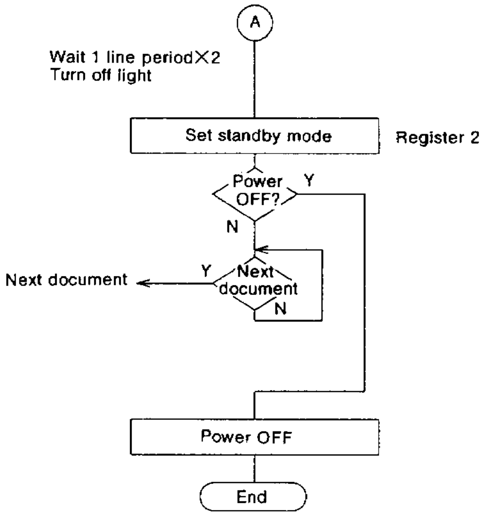


Uniformity correction data creation, transmission(sensor : CIS)



Read operation(sensor : CIS)





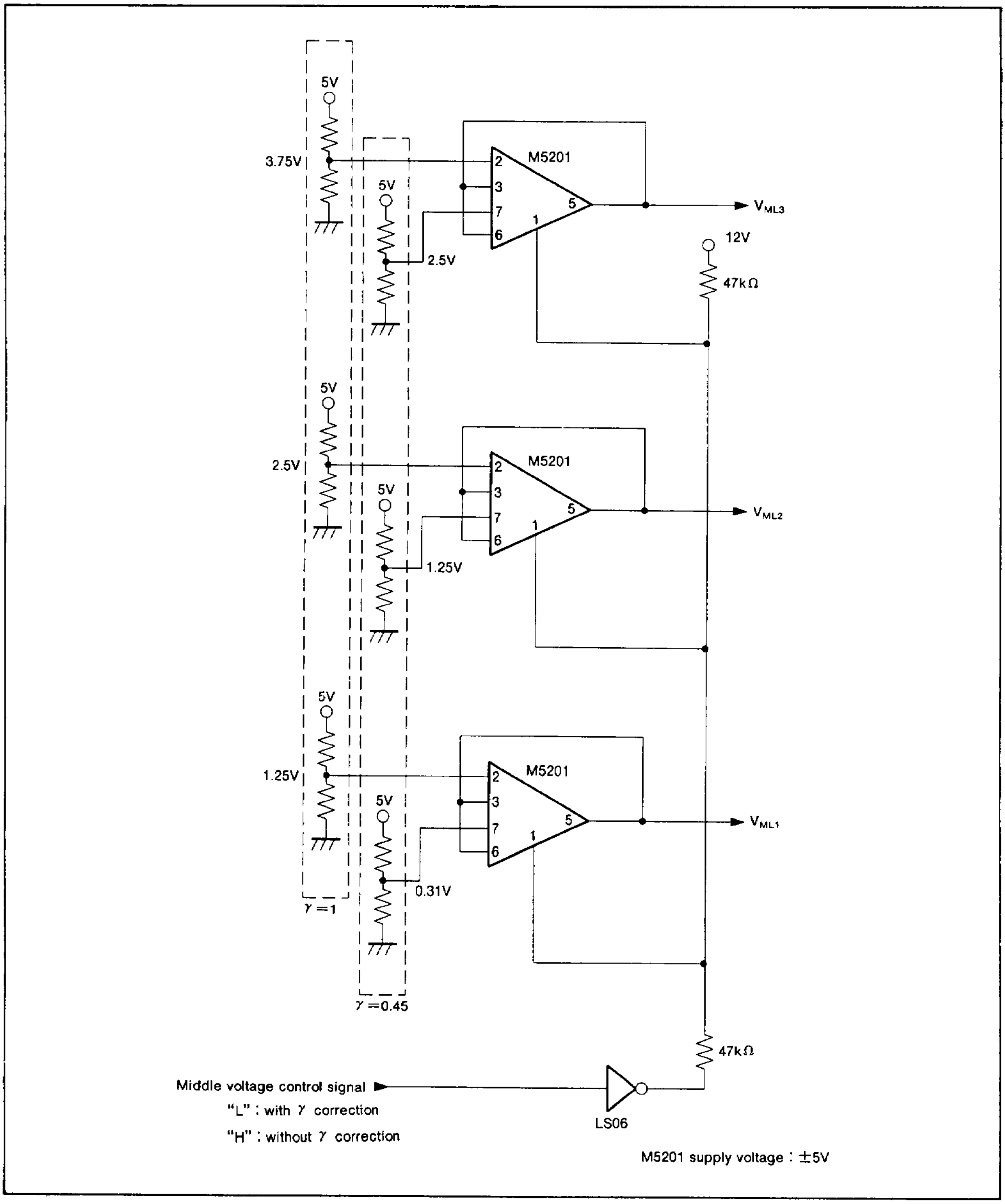


Fig. 19 Middle voltage control circuit example

System Formation